Rockchip RK3399 TRM

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Chapter 1 Introduction

RK3399 is a low power, high performance processor for mobile phones, personal mobile internet device and other digital multimedia applications, and integrates dual-core Cortex-A72 and quad-core Cortex-A53 with separately NEON coprocessor.

Many embedded powerful hardware engines provide optimized performance for high-end application. RK3399 supports almost full-format H.264 decoder by 2160p@30fps, H.265 decoder by 2160p@60fps, VP9 decoder by 2160p@30fps, also support H.264/MVC/VP8 encoder by 1080p@30fps, high-quality JPEG encoder/decoder, special image preprocessor and postprocessor.

Embedded 3D GPU makes RK3399 completely compatible with OpenGL ES1.1/2.0/3.0, OpenCL 1.2 and DirectX 11.1. Special 2D hardware engine with MMU will maximize display performance and provide very smoothly operation.

RK3399 has high-performance dual channel external memory interface (DDR3/DDR3L /LPDDR3/LPDDR4) capable of sustaining demanding memory bandwidths, also provides a complete set of peripheral interface to support very flexible applications.

1.1 Features

The features listed below which may or may not be present in actual product, may be subject to the third party licensing requirements. Please contact Rockchip for actual product feature configurations and licensing requirements.

1.1.1 Microprocessor

- Dual-core ARM Cortex-A72 MPCore processor and quad-core ARM Cortex-A53 MPCore processor, both are high-performance, low-power and cached application processor
- Two CPU clusters, Big cluster with dual-core Cortex-A72 is optimized for high-performance and Little cluster with quad-core Cortex-A53 is optimized for low power
- Full implementation of the ARM architecture v8-A instruction set, ARM Neon Advanced SIMD (single instruction, multiple data) support for accelerating media and signal processing
- ARMv8 Cryptography Extensions
- SCU ensures memory coherency between the MPCore for each clusters
- CCI500 ensures the memory coherency between the two clusters
- Integrated 48KB L1 instruction cache, 32KB L1 data cache for each Cortex-A72
- Integrated 32KB L1 instruction cache, 32KB L1 data cache for each Cortex-A53
- 1024KB unified L2 Cache for big cluster, 512KB unified L2 Cache for little cluster
- Trustzone technology support
- Full coresight debug solution
  - Debug and trace visibility of whole systems
  - ETM trace support
  - Invasive and non-invasive debug
- Eight separate power domains for CPU core system to support internal power switch and externally turn on/off based on different application scenario
  - PD_A72_B0: 1st Cortex-A72 + Neon + FPU + L1 I/D Cache of big cluster
  - PD_A72_B1: 2nd Cortex-A72 + Neon + FPU + L1 I/D Cache of big cluster
  - PD_SCU_B: SCU + L2 Cache controller, and including PD_A72_B0, PD_A72_B1, debug logic of big cluster
  - PD_A53_L0: 1st Cortex-A53 + Neon + FPU + L1 I/D Cache of little cluster
  - PD_A53_L1: 2nd Cortex-A53 + Neon + FPU + L1 I/D Cache of little cluster
  - PD_A53_L2: 3rd Cortex-A53 + Neon + FPU + L1 I/D Cache of little cluster
  - PD_A53_L3: 4th Cortex-A53 + Neon + FPU + L1 I/D Cache of little cluster
  - PD_SCU_L: SCU + L2 Cache controller, and including PD_A53_L0, PD_A53_L1, PD_A53_L2, PD_A53_L3, debug logic of little cluster
- Two isolated voltage domains to support DVFS, one for big cluster, the other for little cluster

1.1.2 Memory Organization

- Internal on-chip memory

- BootRom
- Internal SRAM

- External off-chip memory①
  - DDR3/DDR3L/LPDDR3/LPDDR4
  - SPI NOR/NAND Flash
  - eMMC5.1
  - SD3.0/MMC4.51

1.1.3 Internal Memory

- Internal BootRom
  - Size : 32KB
  - Support system boot from the following device:
    - SPI interface
    - eMMC interface
    - SD/MMC interface
  - Support system code download by the following interface:
    - USB OTG interface
- Internal SRAM
  - Size : 200KB
  - Support security and non-security access
  - Security or non-security space is software programmable
  - Security space can be 0KB,4KB,8KB,12KB,16KB, … up to 192KB by 4KB step

1.1.4 External Memory or Storage device

- Dynamic Memory Interface
  - Compatible with JEDEC standard DDR3/DDR3L/LPDDR3/LPDDR4 SDRAM
  - Support two channels, each channel 16 or 32bits data widths
  - Support up to 2 ranks (chip selects) for each channel
  - Totally 4GB(max) address space for two channels, maximum address space for one channel or one rank of each channel are also 4GB, which is software-configurable
  - 16bits/32bits data width is software programmable
  - 7 host ports with 64bits/128bits AXI bus interface for system access, AXI bus clock is asynchronous with DDR clock
  - Programmable timing parameters to support DDR3/DDR3L/LPDDR3/LPDDR4 SDRAM from various vendor
  - Advanced command reordering and scheduling to maximize bus utilization
  - Programmable output and ODT impedance with dynamic PVT compensation
  - Low power modes, such as power-down and self-refresh for DDR3/DDR3L/LPDDR3/ LPDDR4 SDRAM
  - Support standby mode to auto-gating DDR controller clock for power save
  - Support power down DDR controller and DDR PHY, just keep resetn DDR IO at high status and cke DDR IO at low status to make SDRAM still in self-refresh state to prevent data missing
  - Support hardware-based DDR frequency scaling

- eMMC Interface
  - Fully compliant with JEDEC eMMC 5.1 and eMMC 5.0 specification
  - It is backward compliant with eMMC 4.51 and earlier versions specification.
  - Support HS400, HS200, DDR50 and legacy operating modes
  - Provide eMMC boot sequence to receive boot data from external eMMC device
  - Configurable (Minimum 1 Block Size) FIFO used to aid data transfer between the CPU and the controller
  - Handle the FIFO overrun and underrun condition by stopping interface clock
  - Up to 3200Mbits per second data rate using 8 parallel data lines (eMMC HS400)
  - Up to 1600Mbits per second data rate using 8 parallel data lines (eMMC HS200)
  - Up to 832Mbits per second data rate using 8 parallel data lines (eMMC DDR52 mode)
  - Transfers the data in 1 bit, 4 bit and 8 bit modes

- Cyclic Redundancy Check CRC7 for command and CRC16 for data integrity

- SD/MMC Interface
  - Compatible with SD3.0, MMC ver4.51
  - Provide SD boot sequence to receive boot data from external SD card
  - Support FIFO over-run and under-run prevention by stopping card clock automatically
  - Support CRC generation and error detection
  - Embedded clock frequency division control to provide programmable baud rate
  - Support block size from 1 to 65535Bytes
  - Data bus width is 4bits

1.1.5 System Component

- Cortex-M0
  - Two Cortex-M0 inside RK3399 to cooperate with Cortex-A72/Cortex-A53
  - Thumb instruction set combines high code density with 32-bit performance
  - Integrated sleep modes for low power consumption
  - Fast code execution permits slower processor clock or increases sleep mode time
  - Deterministic, high-performance interrupt handling for time-critical applications
  - Serial Wire Debug reduces the number of pins required for debugging

- CRU (clock & reset unit)
  - Support clock gating control for individual components inside RK3399
  - One oscillator with 24MHz clock input and 8 embedded PLLs
  - Support global soft-reset control for whole SOC, also individual soft-reset for every components

- PMU(power management unit)
  - Multiple configurable work modes to save power by different frequency or automatical clock gating control or power domain on/off control
  - Lots of wakeup sources in different mode
  - 6 separate voltage domains
  - 30 separate power domains, which can be power up/down by software based on different application scenes

- Timer
  - 14 on-chip 64bits Timers in SoC with interrupt-based operation for non-secure application
  - 12 on-chip 64bits Timers in SoC with interrupt-based operation for secure application
  - Provide two operation modes: free-running and user-defined count
  - Support timer work state checkable
  - Fixed 24MHz clock input

- PWM
  - Four on-chip PWMs with interrupt-based operation
  - Programmable pre-scaled operation to bus clock and then further scaled
  - Embedded 32-bit timer/counter facility
  - Support capture mode
  - Support continuous mode or one-shot mode
  - Provides reference mode and output various duty-cycle waveform

- WatchDog
  - Three WatchDogs in SoC with 32 bits counter width
  - Counter clock is from apb bus clock
  - Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
  - WDT can perform two types of operations when timeout occurs:
    - Generate a system reset
    - First generate an interrupt and if this is not cleared by the service routine by the

time a second timeout occurs then generate a system reset
  - Programmable reset pulse length
  - Totally 16 defined-ranges of main timeout period

- MailBox
  - Two MailBoxs in SoC to service muti-core communication
  - Support four mailbox elements per mailbox, each element includes one data word, one command word register and one flag bit that can represent one interrupt
  - Provide 32 lock registers for software to use to indicate whether mailbox is occupied

- Bus Architecture
  - 128-bit/64-bit/32-bit multi-layer AXI/AHB/APB composite bus architecture
  - CCI500 embedded to support two clusters cache coherency
  - 5 embedded AXI interconnect
    - PERI low performance interconnect with one 128-bits AXI master, seven 64-bits AXI masters, one 32-bits AXI master, two 64-bits AXI slaves, five 32-bits AHB masters and lots of 32-bits AHB/APB slaves
    - PERI high performance interconnect with one 128-bits AXI master, one 128-bits AXI slave, four 32-bits AHB masters and lots of 32-bits AHB/APB slaves
    - DISPLAY interconnect with two 128-bits AXI masters, two 64-bits AXI masters, one 32-bits AXI master and lots of 32-bits AHB/APB slaves
    - GPU interconnect with one 128-bits AXI master and 32-bits APB slave
    - VIDEO interconnect with two 128-bits AXI masters, two 64-bits AXI masters and four 32-bits AHB slaves
  - Flexible different QoS solution to improve the utility of bus bandwidth

- Interrupt Controller
  - Support 8 PPI interrupt source and 148 SPI interrupt sources input from different components inside RK3399
  - Support 16 softwre-triggered interrupts
  - Input interrupt level is fixed, high-level sensitive for SPI and low-level sensitive for PPI
  - Support Locality-specific Peripheral Interrupts(LPIs). These interrupts are generated by a peripheral writing to a memory-mapped register in the controller
  - Two axi stream interrupt interfaces separately for each cluster
  - Support different interrupt priority for each interrupt source, and they are always software-programmable

- DMAC
  - Micro-code programming based DMA
  - The specific instruction set provides flexibility for programming DMA transfers
  - Linked list DMA function is supported to complete scatter-gather transfer
  - Support internal instruction cache
  - Embedded DMA manager thread
  - Support data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory
  - Signals the occurrence of various DMA events using the interrupt output signals
  - Mapping relationship between each channel and different interrupt outputs is software-programmable
  - Two embedded DMA controllers for peripheral system
  - DMAC0 features:
    - 6 channels totally
    - 10 hardware request from peripherals
    - 2 interrupt output
    - Dual APB slave interface for register config, designated as secure and non-secure
    - Support trustzone technology and programmable secure state for each DMA channel
  - DMAC1 features:

- 8 channels totally
- 20 hardware request from peripherals
- 2 interrupt output
- Dual APB slave interface for register config, designated as secure and non-secure
- Support trustzone technology and programmable secure state for each DMA channel

- Security system
  - Support trustzone technology for the following components inside RK3399
    - Cortex-A72, support security and non-security mode, switch by software
    - Cortex-A53, support security and non-security mode, switch by software
    - Except Cortex-A72 and Cortex-A53, the other masters in the SoC can also support security and non-security mode by software-programmable
    - Some slave components in SoC can only be addressed by security master and the other slave components can be addressed by security master or non-security master by software-programmable
    - Internal memory, part of space is addressed only in security mode, detailed size is software-programmable together with TZMA(trustzone memory adapter)
    - External DDR space can be divided into eight parts, each part can be software-programmable to be addressed in security mode or non-security mode
  - Embedded dual-channel encryption and decryption engine
    - Support AES 128/192/256 bits key mode, ECB/CBC/CTR/XTS chain mode, Slave/FIFO mode
    - Support DES/3DES(ECB and CBC chain mode), 3DES(EDE/EEE key mode), Slave/FIFO mode
    - Support SHA1/SHA256/MD5(with hardware padding) HASH function, FIFO mode only
    - Support 160 bit Pseudo Random Number Generator (PRNG)
    - Support 256 bit True Random Number Generator (TRNG)
    - Support PKA 512/1024/2048 bit Exp Modulator
  - Support security boot
  - Support security debug

1.1.6 Video CODEC

- Video Decoder
  - Real-time video decoder of MPEG-1, MPEG-2, MPEG-4, H.263, H.264, H.265, VC-1, VP9, VP8, MVC
  - MMU Embedded
  - Supports frame timeout interrupt, frame finish interrupt and bitstream error interrupt
  - Error detection and concealment support for all video formats
  - Output data format YUV420 semi-planar, YUV400(monochrome), YUV422 is supported by H.264
  - H.264 10bit up to HP level 5.1 : 2160p@60fps (4096x2304)②
  - VP9 : 2160p@60fps (4096x2304)
  - H.265/HEVC 10bit : 2160p@60fps (4096x2304)
  - MPEG-4 up to ASP level 5 : 1080p@60fps (1920x1088)
  - MPEG-2 up to MP : 1080p@60fps (1920x1088)
  - MPEG-1 up to MP : 1080p@60fps (1920x1088)
  - H.263 : 576p@60fps (720x576)
  - VC-1 up to AP level 3 : 1080p@30fps (1920x1088)
  - VP8 : 1080p@60fps (1920x1088)
  - MVC : 1080p@60fps (1920x1088)
  - For H.264, image cropping not supported
  - For MPEG-4, GMC(global motion compensation) not supported
  - For VC-1, upscaling and range mapping are supported in image post-processor

- For MPEG-4 SP/H.263, using a modified H.264 in-loop filter to implement deblocking filter in post-processor unit

- Video Encoder
  - Support video encoder for H.264 UP to HP@level4.1, MVC and VP8
  - MMU Embedded
  - Only support I and P slices, not B slices
  - Support error resilience based on constrained intra prediction and slices
  - Input data format:
    - YCbCr 4:2:0 planar
    - YCbCr 4:2:0 semi-planar
    - YCbYCr 4:2:2
    - CbYCrY 4:2:2 interleaved
    - RGB444 and BGR444
    - RGB555 and BGR555
    - RGB565 and BGR565
    - RGB888 and BRG888
    - RGB101010 and BRG101010
  - Image size is from 96x96 to 1920x1080(Full HD)
  - Maximum frame rate is up to 1920x1080@30FPS[2]

1.1.7 JPEG CODEC

- JPEG decoder
  - Input JPEG file : YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 sampling formats
  - Output raw image : YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 semi-planar
  - Decoder size is from 48x48 to 8176x8176(66.8Mpixels)
  - Support JPEG ROI(region of image) decode
  - Maximum data rate[3] is up to 76million pixels per second
  - Embedded memory management unit(MMU)

- JPEG encoder
  - Input raw image :
    - YCbCr 4:2:0 planar
    - YCbCr 4:2:0 semi-planar
    - YCbYCr 4:2:2
    - CbYCrY 4:2:2 interleaved
    - RGB444 and BGR444
    - RGB555 and BGR555
    - RGB565 and BGR565
    - RGB888 and BRG888
    - RGB101010 and BRG101010
  - Output JPEG file : JFIF file format 1.02 or Non-progressive JPEG
  - Encoder image size up to 8192x8192(64million pixels) from 96x32
  - Maximum data rate[3] up to 90million pixels per second
  - Embedded memory management unit(MMU)

1.1.8 Image Enhancement

- Image pre-processor
  - Only used together with HD video encoder inside RK3399, not support stand-alone mode
  - Provides RGB to YCbCr 4:2:0 color space conversion, compatible with BT601, BT709 or user defined coefficients
  - Provides YCbCr4:2:2 to YCbCr4:2:0 color space conversion
  - Support cropping operation from 8192x8192 to any supported encoding size
  - Support rotation with 90 or 270 degrees

- Video stabilization

- Work in combined mode with HD video encoder inside RK3399 and stand-alone mode
- Adaptive motion compensation filter
- Support scene detection from video sequence, encodes key frame when scene change noticed

- Image Post-Processor (embedded inside video decoder)
  - Combined with HD video decoder and JPEG decoder, post-processor can read input data directly from decoder output to reduce bus bandwidth
  - Also work as a stand-alone mode, its input data is from image data stored in external memory
  - Input data format:
    - Any format generated by video decoder in combined mode
    - YCbCr 4:2:0 semi-planar
    - YCbCr 4:2:0 planar
    - YCbYCr 4:2:2
    - YCrYCb 4:2:2
    - CbYCrY 4:2:2
    - CrYCbY 4:2:2
  - Output data format:
    - YCbCr 4:2:0 semi-planar
    - YCbYCr 4:2:2
    - YCrYCb 4:2:2
    - CbYCrY 4:2:2
    - CrYCbY 4:2:2
    - Fully configurable ARGB channel lengths and locations inside 32bits, such as ARGB8888, RGB565, ARGB4444 etc.
  - Input image size:
    - Combined mode: from 48x48 to 8176x8176 (66.8Mpixels)
    - Stand-alone mode: width from 48 to 8176,height from 48 to 8176, and maximum size limited to 16.7Mpixels
    - Step size is 16 pixels
  - Output image size: from 16x16 to 1920x1088 (horizontal step size 8, vertical step size 2)
  - Support image up-scaling:
    - Bicubic polynomial interpolation with a four-tap horizontal kernel and a two-tap vertical kernel
    - Arbitrary non-integer scaling ratio separately for both dimensions
    - Maximum output width is 3x input width
    - Maximum output height is 3x input height
  - Support image down-scaling:
    - Arbitrary non-integer scaling ratio separately for both dimensions
    - Unlimited down-scaling ratio
  - Support YUV to RGB color conversion, compatible with BT.601-5, BT.709 and user definable conversion coefficient
  - Support dithering (2x2 ordered spatial dithering) for 4/5/6bit RGB channel precision
  - Support programmable alpha channel and alpha blending operation with the following overlay input formats:
    - 8bit alpha + YUV444, big endian channel order with AYUV8888
    - 8bit alpha + 24bit RGB, big endian channel order with ARGB8888
  - Support deinterlacing with conditional spatial deinterlace filtering, only compatible with YUV420 input format
  - Support RGB image contrast/brightness/color saturation adjustment
  - Support image cropping & digital zoom only for JPEG or stand-alone mode
  - Support picture in picture
  - Support image rotation (horizontal flip, vertical flip, rotation 90, 180 or 270 degrees)

- Image Enhancement-Processor (IEP)

- Image format
  - Input data: XRGB/RGB565/YUV420/YUV422
  - Output data: ARGB/RGB565/YUV420/YUV422
  - The format ARGB/XRGB/RGB565/YUV support swap
  - Support YUV semi-planar/planar
  - Support BT601_l/BT601_f/BT709_l/BT709_f color space conversion
  - Support RGB dither up/down conversion
  - Support YUV up/down sampling conversion
  - Max resolution for static image up to 8192x8192
  - Max resolution for dynamic image
    - Deinterlace: 1920x1080
    - Sampling noise reduction: 1920x1080
    - Compression noise reduction: 4096x2304
    - Enhancement: 4096x2304
- Enhancement
  - Gamma adjustment with programmable mapping table
  - Hue/Saturation/Brightness/Contrast enhancement
  - Color enhancement with programmable coefficient
  - Detail enhancement with filter matrix up to 7x7
  - Edge enhancement with filter matrix up to 7x7
  - Programmable difference table for detail enhancement
  - Programmable distance table for detail and edge enhancement
- Noise reduction
  - Compression noise reduction with filter matrix up to 7x7
  - Programmable difference table for compression noise reduction
  - Programmable distance table for compression noise reduction
  - Spatial sampling noise reduction
  - Temporal sampling noise reduction
  - Optional coefficient for sampling noise reduction
- Deinterlace
  - Input 4 fields, output 2 frames mode
  - Input 4 fields, output 1 frames mode
  - Input 2 fields, output 1 frames mode
  - Programmable motion detection coefficient
  - Programmable high frequency factor
  - Programmable edge interpolation parameter
  - Source width up to 1920
- Embedded memory management unit(MMU)

1.1.9 Graphics Engine

- 3D Graphics Engine
  - High performance OpenGL ES1.1/2.0/3.0, OpenCL1.2, DirectX11.1 etc.
  - Embedded 4 shader cores with shared hierarchical tiler
  - Provide MMU and L2 Cache with 256KB size
  - Image quality using double-precision FP64, and anti-aliasing capabilities
  - 10-bit and 16-bit YUV input and output formats

- 2D Graphics Engine
  - Source format:
    - ARGB/RGB888/RGB565/RGB4444/RGB5551/YUV420/YUV422(Support YUV422SP10bit/YUV420SP10bit)
  - Destination formats:
    - ARGB/RGB888/RGB565/RGB4444/RGB5551/YUV420/YUV422(Support YVYU422/420 output)
  - Max resolution: 8192x8192 source, 4096x4096 destination
  - Block transfer and Transparency mode
  - Color fill with gradient fill, and pattern fill

- Alpha blending modes including global alpha, per pixel alpha (color/alpha channel separately) and fading
- Arbitrary non-integer scaling ratio, from 1/16 to 16
- 0, 90, 180, 270 degree rotation, x-mirror, y-mirror & rotation operation
- ROP2, ROP3, ROP4
- Support 4k/64k page size MMU

1.1.10 Video IN/OUT

- Camera Interface and Image Processer(Interface and Image Processing)
  - Maximum input resolution of 14M pixels
  - Main scaler with pixel-accurate up- and down-scaling to any resolution between 4416x3312 and 32x16 pixel in processing mode
  - Self scaler with pixel-accurate up- and down-scaling to any resolution between 1920x1080 and 32x16 pixel in processing mode
  - support of semiplanar NV21 color storage format
  - support of independent image cropping on main and self path
  - ITU-R BT 601/656 compliant video interface supporting YCbCr or RGB Bayer data
  - 12 bit camera interface
  - 12 bit resolution per color component internally
  - YCbCr 4:2:2 processing
  - quantization and Huffman tables
  - Windowing and frame synchronization
  - Macro block line, frame end, capture error, data loss interrupts and sync. (h_start, v_start) interrupts
  - Luminance/chrominance and chrominance blue/red swapping for YUV input signals
  - Continuous resize support
  - Color processing (contrast, saturation, brightness, hue, offset, range)
  - Display-ready RGB output in self-picture path (RGB888, RGB666 and RGB565)
  - Rotation unit in self-picture path (90°, 180°, 270° and h/v flipping) for RGB output
  - Read port provided to read back a picture from system memory
  - Simultaneous picture read back, resizing and storing through self path while main
  - path captures the camera picture
  - Black level compensation
  - Four channel Lens shade correction (Vignetting)
  - Auto focus measurement
  - White balancing and black level measurement
  - Auto exposure support by brightness measurement in 5x5 sub windows
  - Defect pixel cluster correction unit (DPCC) supports on the fly and table based pixel correction
  - De-noising pre filter (DPF)
  - Enhanced color interpolation (RGB Bayer demosaicing)
  - Chromatic aberration correction
  - Combined edge sensitive Sharpening / Blurring filter (Noise filter)
  - Color correction matrix (cross talk matrix)
  - Global Tone Mapping with wide dynamic range unit (WDR)
  - Image Stabilization support and Video Stabilization Measurement
  - Flexible Histogram calculation
  - Digital image effects (Emboss, Sketch, Sepia, B/W (Grayscale), Color Selection, Negative image, sharpening)
  - Solarize effect through gamma correction

- Video Output Processor(VOP_BIG)
  - Display interface
    - Parallel RGB LCD Interface
      - RGB888, RGB666, RGB565
    - HDMI interface
      - Support 480p/480i/576p/576i/720p/1080p/1080i/4k

- Support RGB/YUV420(up to 10bit) format
- DP interface
  - Support progressive/interlace
  - Support RGB/YUV420/YUV422/YUV444(up to 10bit) format
- MIPI interface
  - MIPI DCS command mode
  - Dual-MIPI
- EDP interface
- Max resolution
  - Max input resolution：4096x2304
  - Max output resolution：4096x2160
- Scaning timing 8192x4096
- Support configurable polarity of DCLK/HSYNC/VSYNC/DEN

■ Display process
- CABC
- BCSH,10bit
- Support display data swap
- Support YUV2RGB transition and RGB2YUV transition
- Support YUV2YUV
- GAMMA
- Support blank display and black display
- Support standby mode
- X-MIRROR, Y-MIRROR for win0/win1/win2/win3/hwc
- scale down for TV overscan

■ Layer process
- Background layer
  - programmable 30 bit color
- Afbcd
  - format: ARGB8888/RGB888/RGB565
  - Support block split
  - win_sel(win0/win1/win2/win3)
- Win0/Win1 layer
  - Support data format
    - RGB888, ARGB888, RGB565,
    - YCbCr420SP, YCbCr422SP, CbCr444SP, YUYV420, YUYV422, YVYU420, YVYU422
    - RGB(8bit), YUV(8bit/10bit), YVYU/YUYV(8bit)
  - YUV clip
    - Y-8bit: 16~235; UV-8bit: 16~240
    - Y-10bit: 64~940; UV-10bit: 64~960
  - CSC
    - RGB2YUV, YUV2RGB, RGB2RGB, YUV2YUV
  - Support max input resolution 4096x8192
  - Support max output resolution 4096x2160
  - Support virtual display
  - Support 1/8 to 8 scaling-down and scaling-up engine
    - scale up using bicubic and bilinear
    - scale down using bilinear and average
    - per-pix alpha + scale
  - Support data swap
    - RGB/BPP: rb_swap
    - YUV: mid_swap, uv_swap
  - transparency color key, prior to alpha blending and fading
  - Support fading/alpha blending
  - Support interlace output
- Win2/Win3 layer
  - Support data format

- ✧ RGB888, ARGB888, RGB565
- ✧ 8BPP
- ✧ little endian and big endian for BPP
- ✧ BYPASS and LUT mode(32bit LUT，8bit AA+8bit-RGB) for BPP

➢ CSC
- ✧ RGB2YUV, RGB2RGB

➢ 4 display regions
- ✧ only one region at one scanning line

➢ Support data swap
- ✧ RGB/BPP: rb_swap

➢ Support transparency color key, prior to alpha blending and fading
➢ Support fading/alpha blending
➢ Support interlace output

◆ Hardware Cursor layer
➢ Support data format
- ✧ RGB888, ARGB888, RGB565
- ✧ 8BPP
- ✧ little endian and big endian for BPP
- ✧ BYPASS and LUT mode(32bit LUT，8bit AA+8bit-RGB)for BPP

➢ CSC
- ✧ RGB2YUV

➢ Support four hwc size: 32x32, 64x64, 96x96, 128x128
➢ Support 2 color modes: normal and reversed color
➢ Support fading/alpha blending
➢ Support displaying out of panel, right or bottom
➢ Support interlace output

◆ Support p2i
◆ Overlay
➢ support RGB and YUV domain overlay
➢ Support 6 layers, background/win0/win1/win2/win3/hwc
➢ Win0/Win1/Win2/Win3 overlay position exchangeable
➢ Alpha blending
- ✧ Support multi alpha blending modes
- ✧ Support pre-multiplied alpha
- ✧ Support global alpha and per_pix alpha
- ✧ Support 256 level alpha
- ✧ Layer0/layer1/layer2/layer3/hwc support alpha

■ Write back
◆ Support format
➢ RGB565(8bit), RGB888P(8bit)
➢ YUV420(8bit)
◆ Support scale
➢ horizontal scale down using bilinear, 0.25~1.0
➢ vertical throw odd/even line
■ Embedded memory management unit(MMU)

- Video Output Processor(VOP_LIT)
■ Display interface
◆ Parallel RGB LCD Interface
➢ RGB888, RGB666, RGB565
◆ HDMI interface
➢ Support 480p/480i/576p/576i/720p/1080p/1080i
➢ Support RGB format
◆ DP interface
➢ Support progressive/interlace
➢ Support RGB/YUV420/YUV422/YUV444 format
◆ MIPI interface

- MIPI DCS command mode
- Dual-MIPI

- EDP interface
- Max resolution
  - Max input resolution：4096x2304
  - Max output resolution：2560x1600
- Scaning timing 8192x4096
- Support configurable polarity of DCLK/HSYNC/VSYNC/DEN

- Display process
  - CABC
  - BCSH,10bit
  - Support display data swap
  - Support YUV2RGB transition and RGB2YUV transition
  - Support YUV2YUV
  - GAMMA
  - Support blank display and black display
  - Support standby mode
  - X-MIRROR, Y-MIRROR for win0/win2/hwc
  - scale down for TV overscan
- Layer process
  - Background layer
    - programmable 30 bit color
  - Win0 layer
    - Support data format
      - RGB888, ARGB888, RGB565,
      - YCbCr420SP, YCbCr422SP, CbCr444SP, YUYV420, YUYV422, YVYU420, YVYU422
      - RGB(8bit), YUV(8bit), YVYU/YUYV(8bit)
    - YUV clip
      - Y-8bit: 16~235; UV-8bit: 16~240
    - CSC
      - RGB2YUV, YUV2RGB, RGB2RGB, YUV2YUV
    - Support max input resolution 4096x8192
    - Support max output resolution 2560x1600
    - Support virtual display
    - Support 1/8 to 8 scaling-down and scaling-up engine
      - scale up using bicubic and bilinear
      - scale down using bilinear and average
      - per-pix alpha + scale
    - Support data swap
      - RGB/BPP: rb_swap
      - YUV: mid_swap, uv_swap
    - transparency color key, prior to alpha blending and fading
    - Support fading/alpha blending
    - Support interlace output
  - Win2 layer
    - Support data format
      - RGB888, ARGB888, RGB565
      - 8BPP
      - little endian and big endian for BPP
      - BYPASS and LUT mode(32bit LUT，8bit AA+8bit-RGB) for BPP
    - CSC
      - RGB2YUV, RGB2RGB
    - 4 display regions
      - only one region at one scanning line
    - Support data swap
      - RGB/BPP: rb_swap

- Support transparency color key, prior to alpha blending and fading
- Support fading/alpha blending
- Support interlace output

- Hardware Cursor layer
  - Support data format
    - RGB888, ARGB888, RGB565
    - 8BPP
    - little endian and big endian for BPP
    - BYPASS and LUT mode(32bit LUT，8bit AA+8bit-RGB)for BPP
  - CSC
    - RGB2YUV
  - Support four hwc size: 32x32, 64x64, 96x96, 128x128
  - Support 2 color modes: normal and reversed color
  - Support fading/alpha blending
  - Support displaying out of panel, right or bottom
  - Support interlace output
- Support p2i
- Overlay
  - support RGB and YUV domain overlay
  - Support 4 layers, background/win0/win2/hwc
  - Win0/Win2 overlay position exchangeable
  - Alpha blending
    - Support multi alpha blending modes
    - Support pre-multiplied alpha
    - Support global alpha and per_pix alpha
    - Support 256 level alpha
    - Layer0/layer2/hwc support alpha
- Embedded memory management unit(MMU)

1.1.11 HDMI Interface

- Single Physical Layer PHY with support for HDMI 1.4 and 2.0 operation
- For HDMI operation, support for the following:
  - HPD input analog comparator
  - 13.5–600MHz input reference clock
  - Up to 10-bit Deep Color modes
  - Up to 18Gbps aggregate bandwidth
  - Up to 1080p at 120Hz and 4kx2k at 60Hz HDTV display resolutions and up to QXGA graphic display resolutions
  - 3-D video formats
- Link controller flexible interface with 30-, 60- or 120-bit SDR data access
- Support HDCP 1.4/2.2

1.1.12 MIPI Interface

- Embedded 3 MIPI PHY, MIPI0 only for TX, MIPI1 for TX and RX, MIPI2 only for RX
- Lane operation ranging from 80 Mbps to 1.2Gbps in forward direction
- Support 4 data lane, providing up to 4.8Gbps data rate
- Support 1080p@60fps output with single channel
- Support 2560x1600@60fps output with dual channel

1.1.13 eDP Interface

- Compliant with eDP™ Specification, version 1.3
- Support RGB 6/8/10 bit video format
- Up to 4 physical lanes of 2.7/1.62 Gbps/lane
- Support VESA DMT and CVT timing standards
- Fully support EIA/CEA-861D video timing and Info Frame structure
- Hot plug and unplug detection and link status monitor
- Supports Panel Self Refresh(PSR)

1.1.14 DisplayPort Controller

- Compliant with DisplayPort Specification, version 1.3
- Compliant with HDCP2.2 (and back compatible with HDCP1.3)
- 25-600Mhz pixel clk
- Supports 8/10 bpp RGB, YCbCr422, YCbCr420 formats
- Supports up to 4kx2k at 60Hz resolution
- Variety of audio formats – PCM and compressed, over I2S or SPDIF interfaces
- 1Mbps AUX channel

1.1.15 TYPE-C Interface

- Embedded 2 Type-C phy
- Compliant with USB Type-C Specification, revision 1.1
- Complant with USB Power Delivery Specification, revision 2.0
- Attach/detach detection and signaling as DFP, UFP and DRP
- Plug orientation/cable twist detection
- Enable/disable VBUS as DFP and DRP(when operating as DFP)
- VBUS detection as UFP and DRP(when operating as UFP)
- USB Power Delivery communication across the CC wire
- Support USB3.0 Type-C and DisplayPort1.3 Alt Mode on USB Type-C. Two PMA TX-only lanes and two PMA half-duplex TX/RX lanes(can be configured as TX-only or RX-only)
- Up to 5Gbps data rate for USB3.0
- Up to 5.4Gbps(HBR2) data rate for DP1.3, can suport 1/2/4 lane mode
- Support DisplayPort AUX channel

1.1.16 Audio Interface

- I2S/PCM
  - Three I2S/PCM in SoC
  - I2S0/I2S2 support up to 8 channels TX and 8 channels RX. I2S2 is connected to HDMI and DisplayPort internally. I2S0 and I2S1 are exposed for peripherals
  - I2S1 supports up to 2 channels TX and 2 channels RX
  - Audio resolution from 16bits to 32bits
  - Sample rate up to 192KHz
  - Provides master and slave work mode, software configurable
  - Support 3 I2S formats (normal, left-justified, right-justified)
  - Support 4 PCM formats(early, late1, late2, late3)
  - I2S and PCM mode cannot be used at the same time

- SPDIF
  - Support two 16-bit audio data store together in one 32-bit wide location
  - Support biphase format stereo audio data output
  - Support 16 to 31 bit audio data left or right justified in 32-bit wide sample data buffer
  - Support 16, 20, 24 bits audio data transfer in linear PCM mode
  - Support non-linear PCM transfer

1.1.17 Connectivity

- SDIO interface
  - Compatible with SDIO 3.0 protocol
  - 4bits data bus widths

- GMAC 10/100/1000M Ethernet Controller
  - Supports 10/100/1000-Mbps data transfer rates with the RGMII interfaces
  - Supports 10/100-Mbps data transfer rates with the RMII interfaces
  - Supports both full-duplex and half-duplex operation
    - Supports CSMA/CD Protocol for half-duplex operation
    - Supports packet bursting and frame extension in 1000 Mbps half-duplex operation

        - Supports IEEE 802.3x flow control for full-duplex operation
        - Optional forwarding of received pause control frames to the user application in full-duplex operation
        - Back-pressure support for half-duplex operation
        - Automatic transmission of zero-quanta pause frame on deassertion of flow control input in full-duplex operation
    - Preamble and start-of-frame data (SFD) insertion in Transmit, and deletion in Receive paths
    - Automatic CRC and pad generation controllable on a per-frame basis
    - Options for Automatic Pad/CRC Stripping on receive frames
    - Programmable Inter-Frame-Gap (40-96 bit times in steps of 8)
    - Supports a variety of flexible address filtering modes
    - Separate 32-bit status returned for transmission and reception packets
    - Supports IEEE 802.1Q VLAN tag detection for reception frames
    - Support detection of LAN wake-up frames and AMD Magic Packet frames
    - Support checksum off-load for received IPv4 and TCP packets encapsulated by the Ethernet frame
    - Support checking IPv4 header checksum and TCP, UDP, or ICMP checksum encapsulated in IPv4 or IPv6 datagram
    - Comprehensive status reporting for normal operation and transfers with errors
    - Automatic generation of PAUSE frame control or backpressure signal to the GMAC core based on Receive FIFO-fill (threshold configurable) level
    - Handles automatic retransmission of Collision frames for transmission
    - Discards frames on late collision, excessive collisions, excessive deferral and under-run conditions

- SPI Controller
    - 6 on-chip SPI controller inside RK3399
    - Support serial-master and serial-slave mode, software-configurable
    - DMA-based or interrupt-based operation
    - Embedded two 32x16bits FIFO for TX and RX operation respectively
    - Support 2 chip-selects output in serial-master mode

- UART Controller
    - 5 on-chip UART controller inside RK3399
    - DMA-based or interrupt-based operation
    - Embedded two 64Bytes FIFO for TX and RX operation respectively
    - Support 5bit, 6bit, 7bit, 8bit serial data transmit or receive
    - Standard asynchronous communication bits such as start, stop and parity
    - Support different input clock for UART operation to get up to 4Mbps or other special baud rate
    - Support non-integer clock divides for baud clock generation
    - Support auto flow control mode for UART0 and UART3

- I2C controller
    - 9 on-chip I2C controller in RK3399
    - Multi-master I2C operation
    - Support 7bits and 10bits address mode
    - Serial 8bits oriented and bidirectional data transfers can be made at up to 100Kbit/s in the standard mode
    - Software programmable clock frequency and transfer rate up to 400Kbit/s in the fast speed mode and 1Mbit/s in the high speed mode

- GPIO
    - 5 groups of GPIO (GPIO0~GPIO4), totally have 122 GPIOs
    - All of GPIOs can be used to generate interrupt to Cortex-A72/Cortex-A53
    - GPIO0/GPIO1 can be used to wakeup system from low-power mode

- The pull direction(pullup or pulldown) for all of GPIOs are software-programmable
- All of GPIOs are always in input direction in default after power-on-reset
- The drive strength for all of GPIOs is software-programmable

- USB OTG3.0
  - Embedded 2 USB OTG3.0 interfaces
  - Compatible Specification
    - Universal Serial Bus 3.0 Specification, Revision 1.0
    - Universal Serial Bus Specification, Revision 2.0
    - eXtensible Host Controller Interface for Universal Serial Bus (xHCI), Revision 1.1
  - Support Control/Bulk(including stream)/Interrupt/Isochronous Transfer
  - Simultaneous IN and OUT transfer for USB3.0, up to 8Gbps bandwidth
  - Descriptor Caching and Data Pre-fetching
  - USB3.0 Device Features
    - Up to 7 IN endpoints, including control endpoint 0
    - Up to 6 OUT endpoints, including control endpoint 0
    - Up to 13 endpoint transfer resources, each one for each endpoint
    - Flexible endpoint configuration for multiple applications/USB set-configuration modes
    - Hardware handles ERDY and burst
    - Stream-based bulk endpoints with controller automatically initiating data movement
    - Isochronous endpoints with isochronous data in data buffers
    - Flexible Descriptor with rich set of features to support buffer interrupt moderation, multiple transfers, isochronous, control, and scattered buffering support
  - USB 3.0 xHCI Host Features
    - Support up to 64 devices
    - Support 1 interrupter
    - Support 1 USB2.0 port and 1 Super-Speed port
    - Concurrent USB3.0/USB2.0 traffic, up to 8.48Gbps bandwidth
    - Support standard or open-source xHCI and class driver
    - Support xHCI Debug Capability
  - USB 3.0 Dual-Role Device (DRD) Features
    - Static Device operation
    - Static Host operation
    - USB3.0/USB2.0 OTG A device and B device basing on ID
    - UFP/DFP and Data Role Swap Defined in USB TypeC Specification
    - Not support USB3.0/USB2.0 OTG session request protocol(SRP), host negotiation protocol(HNP) and Role Swap Protocol(RSP)

- USB Host2.0
  - Embedded 2 USB Host 2.0 interfaces
  - Compatible Specification
    - Universal Serial Bus Specification, Revision 2.0
    - Enhanced Host Controller Interface Specification(EHCI), Revision 1.0
    - Open Host Controller Interface Specification(OHCI), Revision 1.0a
  - Support high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps)

- PCIe2.1 Interface
  - Compatible with PCI Express Base Specification Revision 2.1
  - Dual operation mode: Root Complex(RC) and End Point(EP)
  - Maximum link width is 4, single bi-directional Link interface
  - Support 2.5GT/s and 5.0 GT/s serial data transmission rate per lane per direction
  - Support 100MHz differential clock output(optional with SSC) for system application
  - Support DMA within the module, 2 channels, 2 RAM partitions, 2K bytes depth
  - Support Resizable BAR Capability
  - Support Single Physical PCI Functions in Endpoint Mode

- Support Legacy Interrupt and MSI and MSI-X interrupt
- Support Outbound and Inbound Address Translation
- Support 8 Virtual Functions attached to Physical Function
- Support PCI Express Active State Power Management (ASPM) state L0s and L1
- Support L1 Power Management Substate
- Support PCI Function power states D0, D1 and D3, and the corresponding link power states L0, L1 and L2

1.1.18 Others

- Temperature Sensor(TS-ADC)
  - Embedded 2 channel TS-ADC in RK3399
  - TS-ADC clock must be less than 800KHZ
  - 10-bits TS-ADC up to 50KS/s sampling rate
  - -40~125C temperature range and 5℃ temperature resolution

- SAR-ADC(Successive Approximation Register)
  - 6-channel single-ended 10-bit SAR analog-to-digital converter
  - SAR-ADC clock must be less than 13MHZ
  - Conversion speed range is up to 1MS/s sampling rate

- eFuse
  - Two 1024bits(32x32) high-density electrical Fuse are integrated in RK3399
  - Support standby mode and power down mode
  - Embedded power-switch
  - Embedded four redundancy bits

- Package Type
  - FCBGA828(body: 21mmx21mm; ball size: 0.35mm; ball pitch: 0.65mm)

Notes:
①:DDR3/DDR3L/LPDDR3/LPDDR4 are not used simultaneously
②:Actual maximum frame rate will depend on the clock frequency and system bus performance
③:Actual maximum data rate will depend on the clock frequency and JPEG compression rate

1.2 Block Diagram

The following diagram shows the basic block diagram for RK3399.

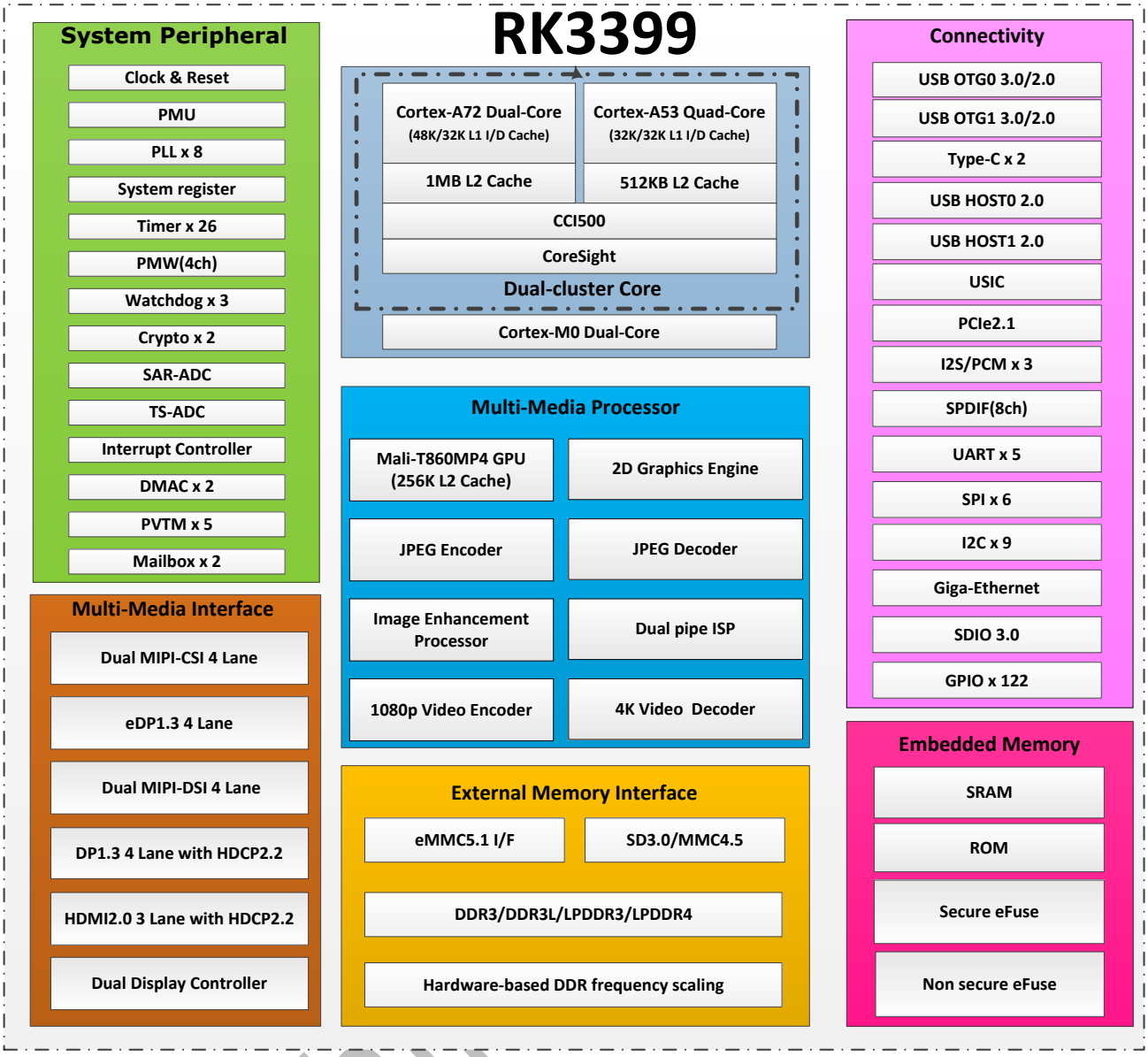


Fig. 1-1 RK3399 Block Diagram

Chapter 2 System Overview

2.1 Address Mapping

RK3399 supports to boot from internal bootrom, which supports remap function by software programming. Remap is controlled by SGRF_PMU_CON0[15]. When remap is set to 0, the 0xFFFF0000 address is mapped to bootrom. When remap is set to 1, the 0xFFFF0000 address is mapped to INTMEM0.

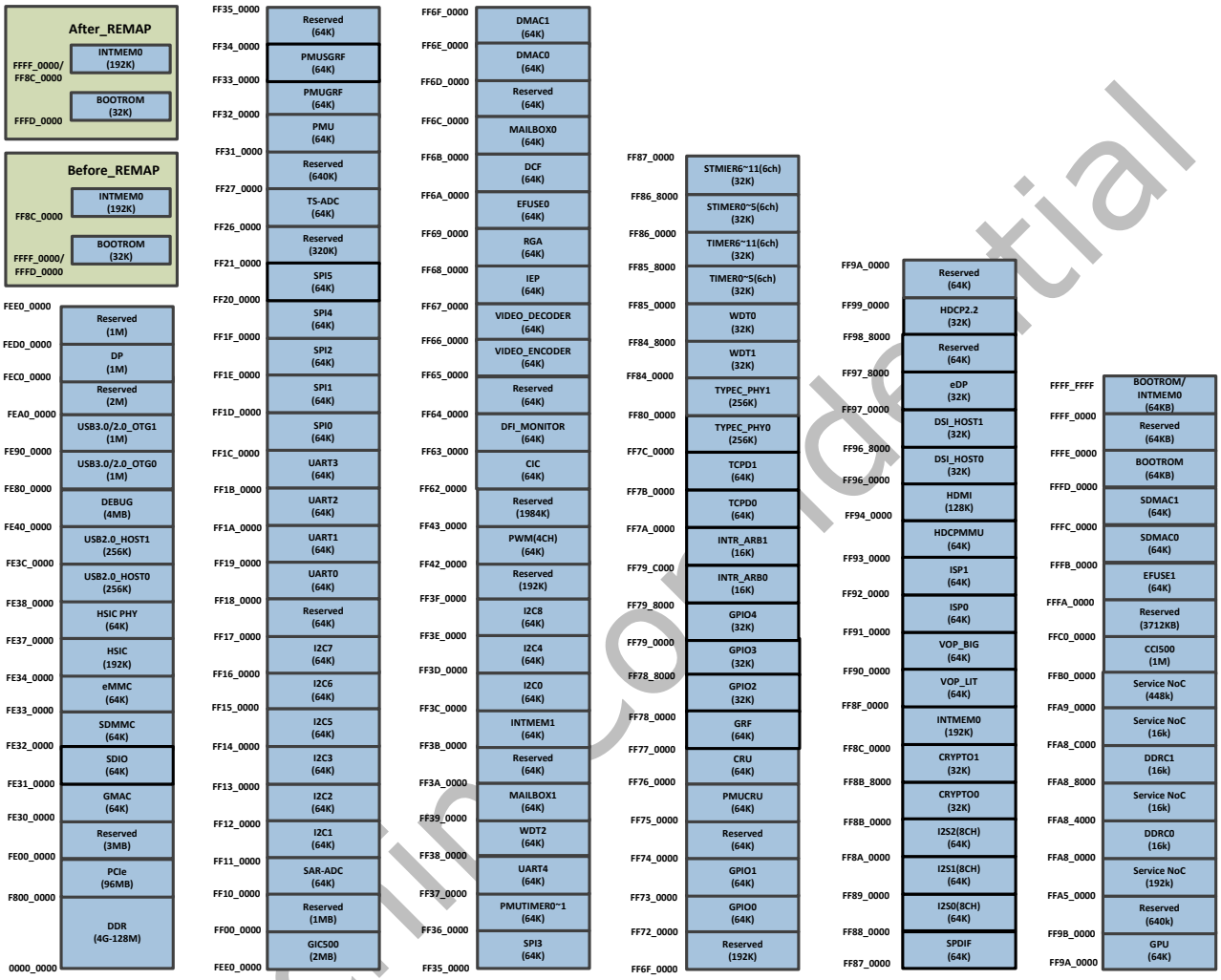


Fig. 2-1 RK3399 Address Mapping

2.2 System Boot

RK3399 provides system boot from off-chip devices such as serial nand or nor flash, eMMC memory, SD/MMC card. When boot code is not ready in these devices, also provide system code download into them by USB OTG interface. All of the boot code will be stored in internal bootrom. The following is the whole boot procedure for boot code, which will be stored in bootrom in advance.

The following features are supports.

- Support secure boot mode and non-secure boot mode
- Support system boot from the following device:
  - SPI interface
  - eMMC interface
  - SD/MMC Card
- Support system code download by USB OTG

Following figure shows RK3399 boot procedure flow.

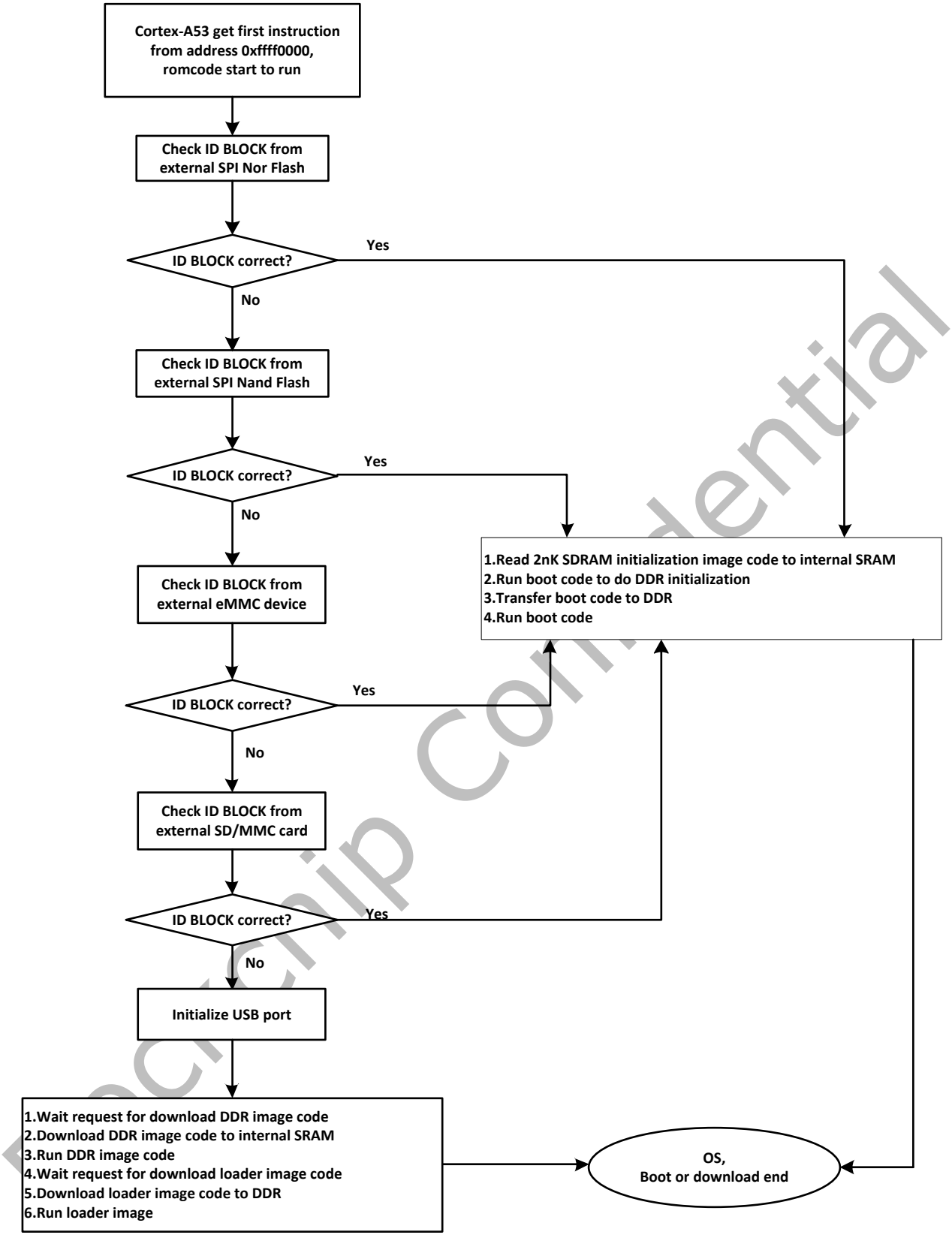


Fig. 2-2 RK3399 boot procedure flow

2.3 System Interrupt Connection for Cortex-A72/Cortex-A53

RK3399 provides an general interrupt controller(GIC) for Cortex-A72/Cortex-A53, which has 148 SPI(shared peripheral interrupts) interrupt sources and 8 PPI(Private peripheral interrupt) interrupt sources. GIC communicate with CPU through two axi stream interrupt interfaces separately for each cluster. The triggered type for each SPI interrupt is high level sensitive, and for each PPI interrupt is low level sensitive, not programmable. The detailed interrupt sources connection is in the following table. For detailed GIC setting, please refer to Chapter

GIC.

Table 2-1 RK3399 Interrupt connection list for Cortex-A72/Cortex-A53

Interrupt Type	Interrupt ID	Source	Polarity
Source(PPI)	16	NA	Low level
	17	NA	Low level
	18	NA	Low level
	19	NA	Low level
	20	NA	Low level
	21	NA	Low level
	22	ncommirq	Low level
	23	npmuirq	Low level
	24	nctiirqack	Low level
	25	nvcpumntirq	Low level
	26	ncnthpirq	Low level
	27	ncntvirq	Low level
	28	NA	Low level
	29	ncntpsirq	Low level
	30	ncntpnsirq	Low level
	31	NA	Low level
Source(SPI)	32	crypto0_int	High level
	33	dcf_done_int	High level
	34	dcf_error_int	High level
	35	ddrc0_int	High level
	36	ddrc1_int	High level
	37	dmac0_perilp_irq_abort	High level
	38	dmac0_perilp_irq	High level
	39	dmac1_perilp_irq_abort	High level
	40	dmac1_perilp_irq	High level
	41	dp_irq	High level
	42	edp_irq	High level
	43	emmccore_int	High level
	44	gmac_int	High level
	45	gmac_pmt_int	High level
	46	gpio0_int	High level
	47	gpio1_int	High level
	48	gpio2_intr	High level
	49	gpio3_intr	High level
	50	gpio4_intr	High level
	51	gpu_irqgpu	High level
	52	gpu_irqjob	High level
	53	gpu_irqmmu	High level
	54	hdcp22_irq	High level
	55	hdmi_irq	High level
	56	hdmi_wakeup_irq	High level

Interrupt Type	Interrupt ID	Source	Polarity
	57	host0_arb_int	High level
	58	host0_ehci_int	High level
	59	host0_linestate_irq	High level
	60	host0_ohci_int	High level
	61	host1_arb_int	High level
	62	host1_ehci_int	High level
	63	host1_linestate_irq	High level
	64	host1_ohci_int	High level
	65	hsic_int	High level
	66	i2c3_int	High level
	67	i2c2_int	High level
	68	i2c7_int	High level
	69	i2c6_int	High level
	70	i2c5_int	High level
	71	i2s0_int	High level
	72	i2s1_int	High level
	73	i2s2_int	High level
	74	iep_intr	High level
	75	isp0_irq	High level
	76	isp1_irq	High level
	77	mipi_dsi_host0_irq	High level
	78	mipi_dsi_host1_irq	High level
	79	errirq_cci	High level
	80	noc_intr	High level
	81	pcie_sys_int	High level
	82	pcie_legacy_int	High level
	83	pcie_client_int	High level
	84	spi2_int	High level
	85	spi1_int	High level
	86	pmu_int	High level
	87	rga_intr	High level
	88	i2c4_int	High level
	89	i2c0_int	High level
	90	i2c8_int	High level
	91	i2c1_int	High level
	92	spi3_int	High level
	93	pwm_int	High level
	94	saradc_int	High level
	95	sd_detectn_irq	High level
	96	sdio_int	High level
	97	sdmmc_int	High level
	98	spdif_int	High level

Interrupt Type	Interrupt ID	Source	Polarity
	99	spi4_int	High level
	100	spi0_int	High level
	101	stimer_intr0	High level
	102	stimer_intr1	High level
	103	stimer_intr2	High level
	104	stimer_intr3	High level
	105	stimer_intr4	High level
	106	stimer_intr5	High level
	107	stimer_intr6	High level
	108	stimer_intr7	High level
	109	stimer_intr8	High level
	110	stimer_intr9	High level
	111	stimer_intr10	High level
	112	stimer_intr11	High level
	113	timer_intr0	High level
	114	timer_intr1	High level
	115	timer_intr2	High level
	116	timer_intr3	High level
	117	timer_intr4	High level
	118	timer_intr5	High level
	119	timer_intr6	High level
	120	timer_intr7	High level
	121	timer_intr8	High level
	122	timer_intr9	High level
	123	timer_intr10	High level
	124	timer_intr11	High level
	125	perf_int_a53	High level
	126	perf_int_a72	High level
	127	pmutimer_int0	High level
	128	pmutimer_int1	High level
	129	tsadc_int	High level
	130	uart1_int	High level
	131	uart0_int	High level
	132	uart2_int	High level
	133	uart3_int	High level
	134	uart4_int	High level
	135	usb3otg0_bvalid_irq	High level
	136	usb3otg0_id_irq	High level
	137	usb3otg0_int	High level
	138	usb3otg0_linestate_irq	High level
	139	usb3otg0_rxdet_irq	High level
	140	usb3otg1_bvalid_irq	High level

Interrupt Type	Interrupt ID	Source	Polarity
	141	usb3otg1_id_irq	High level
	142	usb3otg1_int	High level
	143	usb3otg1_linestate_irq	High level
	144	usb3otg1_rxdet_irq	High level
	145	vcodec_dec_int	High level
	146	vcodec_enc_int	High level
	147	vcodec_mmu_int	High level
	148	vdu_dec_irq	High level
	149	vdu_mmu_irq	High level
	150	vopbig_irq	High level
	151	voplit_irq	High level
	152	wdt0_intr	High level
	153	wdt1_intr	High level
	154	wdt2_int	High level
	155	usb3otg0_pme_generation	High level
	156	usb3otg0_host_legacy_smi_interrupt	High level
	157	usb3otg0_host_sys_err	High level
	158	usb3otg1_pme_generation	High level
	159	usb3otg1_host_legacy_smi_interrupt	High level
	160	usb3otg1_host_sys_err	High level
	161	vopbig_irq_ddr	High level
	162	voplit_irq_ddr	High level
	163	ddr_mon_intr	High level
	164	spi5_int	High level
	165	tcpd_int0	High level
	166	tcpd_int1	High level
	167	crypto1_int	High level
	168	gasket_irq	High level
	169	pcie_rc_mode_elec_idle_irq	High level
	170	N/A	High level
	171	N/A	High level
	172	mailbox1_int[0]	High level
	173	mailbox1_int[1]	High level
	174	mailbox1_int[2]	High level
	175	mailbox1_int[3]	High level
	176	mailbox0_int[0]	High level
	177	mailbox0_int[1]	High level
	178	mailbox0_int[2]	High level
	179	mailbox0_int[3]	High level
	180	exterrirq_pd_core_l	High level
	181	exterrirq_pd_core_b	High level

2.4 System Interrupt Connection for Cortex-M0

RK3399 provides two interrupt arbiters for Cortex-M0, one for each Cortex-M0; Interrupt arbiter has 142 SPI interrupt sources and output 18 interrupt signals to M0 after arbitration. The triggered type for each SPI interrupt is high level sensitive, not programmable. The detailed interrupt sources connection is in the following table. In the Table, for perilpm0, the mailbox interrupt is from mailbox0; For pmum0, the mailbox interrupt is from mailbox1; For detailed interrupt arbiter setting, please refer to Chapter Cortex M0.

Table 2-2 RK3399 Interrupt connection list for Cortex-M0

Interrupt Type	Interrupt ID	Source	Polarity
Source(SPI)	0	crypto0_int	High level
	1	dcf_done_int	High level
	2	dcf_error_int	High level
	3	ddrc0_int	High level
	4	ddrc1_int	High level
	5	dmac0_perilp_irq_abort	High level
	6	dmac0_perilp_irq	High level
	7	dmac1_perilp_irq_abort	High level
	8	dmac1_perilp_irq	High level
	9	dp_irq	High level
	10	edp_irq	High level
	11	emmccore_int	High level
	12	gmac_int	High level
	13	gmac_pmt_int	High level
	14	gpio0_int	High level
	15	gpio1_int	High level
	16	gpio2_intr	High level
	17	gpio3_intr	High level
	18	gpio4_intr	High level
	19	gpu_irqgpu	High level
	20	gpu_irqjob	High level
	21	gpu_irqmmu	High level
	22	hdcp22_irq	High level
	23	hdmi_irq	High level
	24	hdmi_wakeup_irq	High level
	25	host0_arb_int	High level
	26	host0_ehci_int	High level
	27	host0_linestate_irq	High level
	28	host0_ohci_int	High level
	29	host1_arb_int	High level
	30	host1_ehci_int	High level
	31	host1_linestate_irq	High level
	32	host1_ohci_int	High level
	33	hsic_int	High level

Interrupt Type	Interrupt ID	Source	Polarity
	34	i2c3_int	High level
	35	i2c2_int	High level
	36	i2c7_int	High level
	37	i2c6_int	High level
	38	i2c5_int	High level
	39	i2s0_int	High level
	40	i2s1_int	High level
	41	i2s2_int	High level
	42	iep_intr	High level
	43	isp0_irq	High level
	44	isp1_irq	High level
	45	mipi_dsi_host0_irq	High level
	46	mipi_dsi_host1_irq	High level
	47	errirq_cci	High level
	48	noc_intr	High level
	49	pcie_sys_int	High level
	50	pcie_legacy_int	High level
	51	pcie_client_int	High level
	52	spi2_int	High level
	53	spi1_int	High level
	54	pmu_int	High level
	55	rga_intr	High level
	56	i2c4_int	High level
	57	i2c0_int	High level
	58	i2c8_int	High level
	59	i2c1_int	High level
	60	spi3_int	High level
	61	pwm_int	High level
	62	saradc_int	High level
	63	sd_detectn_irq	High level
	64	sdio_int	High level
	65	sdmmc_int	High level
	66	spdif_int	High level
	67	spi4_int	High level
	68	spi0_int	High level
	69	stimer_intr0	High level
	70	stimer_intr1	High level
	71	stimer_intr2	High level
	72	stimer_intr3	High level
	73	stimer_intr4	High level
	74	stimer_intr5	High level
	75	stimer_intr6	High level

Interrupt Type	Interrupt ID	Source	Polarity
	76	stimer_intr7	High level
	77	stimer_intr8	High level
	78	stimer_intr9	High level
	79	stimer_intr10	High level
	80	stimer_intr11	High level
	81	timer_intr0	High level
	82	timer_intr1	High level
	83	timer_intr2	High level
	84	timer_intr3	High level
	85	timer_intr4	High level
	86	timer_intr5	High level
	87	timer_intr6	High level
	88	timer_intr7	High level
	89	timer_intr8	High level
	90	timer_intr9	High level
	91	timer_intr10	High level
	92	timer_intr11	High level
	93	perf_int_a53	High level
	94	perf_int_a72	High level
	95	pmutimer_int0	High level
	96	pmutimer_int1	High level
	97	tsadc_int	High level
	98	uart1_int	High level
	99	uart0_int	High level
	100	uart2_int	High level
	101	uart3_int	High level
	102	uart4_int	High level
	103	usb3otg0_bvalid_irq	High level
	104	usb3otg0_id_irq	High level
	105	usb3otg0_int	High level
	106	usb3otg0_linestate_irq	High level
	107	usb3otg0_rxdet_irq	High level
	108	usb3otg1_bvalid_irq	High level
	109	usb3otg1_id_irq	High level
	110	usb3otg1_int	High level
	111	usb3otg1_linestate_irq	High level
	112	usb3otg1_rxdet_irq	High level
	113	vcodec_dec_int	High level
	114	vcodec_enc_int	High level
	115	vcodec_mmu_int	High level
	116	vdu_dec_irq	High level
	117	vdu_mmu_irq	High level

Interrupt Type	Interrupt ID	Source	Polarity
	118	vopbig_irq	High level
	119	voplit_irq	High level
	120	wdt0_intr	High level
	121	wdt1_intr	High level
	122	wdt2_int	High level
	123	usb3otg0_pme_generation	High level
	124	usb3otg0_host_legacy_smi_interrupt	High level
	125	usb3otg0_host_sys_err	High level
	126	usb3otg1_pme_generation	High level
	127	usb3otg1_host_legacy_smi_interrupt	High level
	128	usb3otg1_host_sys_err	High level
	129	vopbig_irq_ddr	High level
	130	voplit_irq_ddr	High level
	131	ddr_mon_intr	High level
	132	spi5_int	High level
	133	tcpd_int0	High level
	134	tcpd_int1	High level
	135	crypto1_int	High level
	136	gasket_irq	High level
	137	pcie_rc_mode_elec_idle_irq	High level
	138	N/A	High level
	139	N/A	High level
	140	mailbox*_int[0]	High level
	141	mailbox*_int[1]	High level
	142	mailbox*_int[2]	High level
	143	mailbox*_int[3]	High level

2.5 System DMA Hardware Request Connection

RK3399 provides two DMA controllers: DMAC0 and DMAC1, both are in the pd_peri_lp system. As for DMAC0, there are 10 hardware request ports. The trigger type for each of them is high level, not programmable. As for DMAC1, there are 20 hardware request ports. Also the trigger type for each of them is high level, not programmable. For detailed descriptions of DMAC0/DMAC1, please refer to Chapter DMAC. Following two tables include DMAC0/DMAC1 hardware request connection list separately.

Table 2-3 RK3399 DMAC0 Hardware Request Connection List

DMAC0		
Req Number	**Source**	**Polarity**
0	I2S0 tx	High level
1	I2S0 rx	High level
2	I2S1 tx	High level
3	I2S1 rx	High level
4	I2S2 tx	High level

DMAC0		
Req Number	**Source**	**Polarity**
5	I2S2 rx	High level
6	PWM rx	High level
7	SPDIF tx	High level
8	SPI5 tx	High level
9	SPI5 rx	High level

Table 2-4 RK3399 DMAC1 Hardware Request Connection List

DMAC1		
Req Number	**Source**	**Polarity**
0	UART0 tx	High level
1	UART0 rx	High level
2	UART1 tx	High level
3	UART1 rx	High level
4	UART2 tx	High level
5	UART2 rx	High level
6	UART3 tx	High level
7	UART3 rx	High level
8	UART4 tx	High level
9	UART4 rx	High level
10	SPI0 tx	High level
11	SPI0 rx	High level
12	SPI1 tx	High level
13	SPI1 rx	High level
14	SPI2 tx	High level
15	SPI2 rx	High level
16	SPI3 tx	High level
17	SPI3 rx	High level
18	SPI4 tx	High level
19	SPI4 rx	High level

Chapter 3 Clock & Reset Unit (CRU)

3.1 Overview

The CRU is an APB slave module that is designed for generating all of the internal and system clocks, resets of chip. CRU generates system clock from PLL output clock or external clock source, and generates system reset from external power-on-reset, watchdog timer reset or software reset.

CRU supports the following features:

- Compliance to the AMBA APB interface
- Embedded 8 PLLs: BPLL/LPLL/DPLL/CPLL/GPLL/NPLL/VPLL/PPLL
- Flexible selection of clock source
- Supports the respective gating of all clocks
- Supports the respective software reset of all modules

3.2 Block Diagram

The CRU comprises with:

- PLL
- Register configuration unit
- Clock generate unit
- Reset generate unit

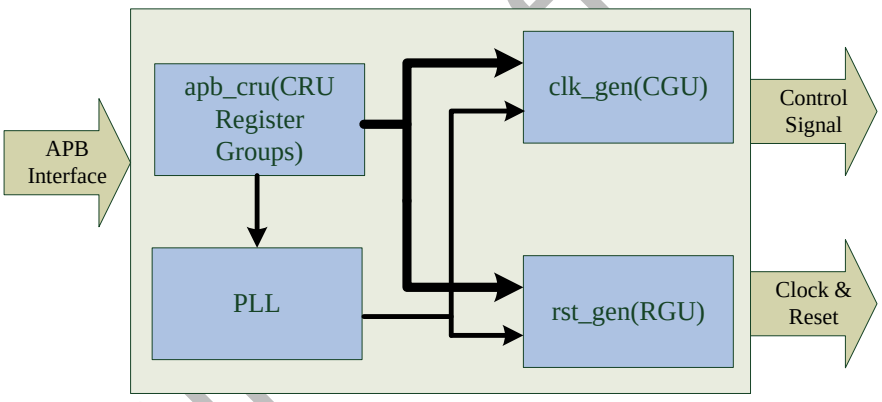


Fig. 3-1 CRU Architecture

3.3 System Clock Solution

The following tables show clock architecture (mux and divider information).

	clk		parents (ID)											
MODULE	ID	CLKNAME	0	1	2	3	4	5	6	7	MUX	GATE	DIV	FRAC
PMU	1000	pclk_pmu_src	8	-	-	-	-	-	-	-	-	PMUGRF0[4]	PS0[4:0]	-
PMU	1001	fclk_cm0s_pmu_ppll_src	8	-	-	-	-	-	-	-	-	PG0[1]	-	-
PMU	1516	fclk_cm0s_src_pmu	1001	0	-	-	-	-	-	-	GF_PS0[15]	-	PS0[12:8]	-
PMU	1040	clk_spi3_pmu	0	8	-	-	-	-	-	-	PS1[7]	PG0[2]	PS1[6:0]	-
PMU	1004	clk_wifi_div	8	0	-	-	-	-	-	-	PS1[13]	PG0[8]	PS1[12:8]	-
PMU	1005	clk_wifi_frac	1004	-	-	-	-	-	-	-	-	-	-	PS7
PMU	1006	clk_wifi_pmu	1004	1005	-	-	-	-	-	-	PS1[14]	-	-	-
PMU	1007	clk_timer_src_pmu	0	10	-	-	-	-	-	-	GF_PS1[15]	-	-	-
PMU	1020	clk_i2c0_pmu	8	-	-	-	-	-	-	-	-	PG0[9]	PS2[6:0]	-
PMU	1022	clk_i2c8_pmu	8	-	-	-	-	-	-	-	-	PG0[11]	PS2[14:8]	-
PMU	1021	clk_i2c4_pmu	8	-	-	-	-	-	-	-	-	PG0[10]	PS3[6:0]	-
cif_testout	1011	clk_32k_suspend_pmu	0	-	-	-	-	-	-	-		-	PS4[9:0]	-
PMU	1030	clk_uart4_div	0	8	-	-	-	-	-	-	PS5[10]	PG0[5]	PS5[6:0]	-
PMU	1031	clk_uart4_frac	1030	-	-	-	-	-	-	-	-	PG0[6]	-	PS6
PMU	1032	clk_uart4_pmu	1030	1031	0	-	-	-	-	-	PS5[9:8]	-	-	-
PMU	1012	clk_timer0_pmu	1007	-	-	-	-	-	-	-	-	PG0[3]	-	-
PMU	1013	clk_timer1_pmu	1007	-	-	-	-	-	-	-	-	PG0[4]	-	-
PMU	1014	clk_pvtm_pmu	0	-	-	-	-	-	-	-	-	PG0[7]	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
PMU	1015	pclk_pmu	1000	-	-	-	-	-	-	-	-	PG1[0]	-	-
PMU	15	pclk_pmugrf_pmu	10	-	-	-	-	-	-	-	-	PG1[1]	-	-

	clk		parents (ID)										
	01		00										
PMU	15 02	pclk_intmem1_pmu	10 00	-	-	-	-	-	-	-	-	PG1[2]	-	-
PMU	15 03	pclk_gpio0_pmu	10 00	-	-	-	-	-	-	-	-	PG1[3]	-	-
PMU	15 04	pclk_gpio1_pmu	10 00	-	-	-	-	-	-	-	-	PG1[4]	-	-
PMU	15 05	pclk_sgrf_pmu	10 00	-	-	-	-	-	-	-	-	PG1[5]	-	-
PMU	15 06	pclk_noc_pmu	10 00	-	-	-	-	-	-	-	-	PG1[6]	-	-
PMU	15 07	pclk_i2c0_pmu	10 00	-	-	-	-	-	-	-	-	PG1[7]	-	-
PMU	15 08	pclk_i2c4_pmu	10 00	-	-	-	-	-	-	-	-	PG1[8]	-	-
PMU	15 09	pclk_i2c8_pmu	10 00	-	-	-	-	-	-	-	-	PG1[9]	-	-
PMU	15 10	pclk_rkpwm_pmu	10 00	-	-	-	-	-	-	-	-	PG1[10]	-	-
PMU	15 11	pclk_spi3_pmu	10 00	-	-	-	-	-	-	-	-	PG1[11]	-	-
PMU	15 12	pclk_timer_pmu	10 00	-	-	-	-	-	-	-	-	PG1[12]	-	-
PMU	15 13	pclk_mailbox_pmu	10 00	-	-	-	-	-	-	-	-	PG1[13]	-	-
PMU	15 14	pclk_uart4_pmu	10 00	-	-	-	-	-	-	-	-	PG1[14]	-	-
PMU	15 15	pclk_wdt_m0_pmu	10 00	-	-	-	-	-	-	-	-	PG1[15]	-	-
PMU	10 02	fclk_cm0s_pmu	15 16	-	-	-	-	-	-	-	-	PG2[0]	-	-
PMU	15 18	sclk_cm0s_pmu	15 16	-	-	-	-	-	-	-	-	PG2[1]	-	-
PMU	15 19	hclk_cm0s_pmu	15 16	-	-	-	-	-	-	-	-	PG2[2]	-	-
PMU	15 20	dclk_cm0s_pmu	15 16	-	-	-	-	-	-	-	-	PG2[3]	-	-
PMU	15 21	hclk_noc_pmu	15 16	-	-	-	-	-	-	-	-	PG2[5]	-	-

Note :

*PS** *PMUCRU_CLKSEL_CON**

*PG** *PMUCRU_GATE_CON**

*GF_PS** *glitch-free*

Fig. 3-2 RK3399 PMUCRU Clock Architecture Diagram

	clk		parents (ID)											
MODULE	ID	CLKNAME	0	1	2	3	4	5	6	7	MUX	GATE	DIV	FRAC
IO_CLK	0	clk_24m<IO>	-	-	-	-	-	-	-	-	-	-	-	-
PLL	1	lpll	0	-	-	-	-	-	-	-	-	-	-	-
PLL	2	bpll	0	-	-	-	-	-	-	-	-	-	-	-
PLL	3	dpll	0	-	-	-	-	-	-	-	-	-	-	-
PLL	4	cpll	0	-	-	-	-	-	-	-	-	-	-	-
PLL	5	gpll	0	-	-	-	-	-	-	-	-	-	-	-
PLL	6	npll	0	-	-	-	-	-	-	-	-	-	-	-
PLL	7	vpll	0	-	-	-	-	-	-	-	-	-	-	-
PLL	8	ppll	0	-	-	-	-	-	-	-	-	-	-	-
usbphy	9	upll	0	132	-	-	-	-	-	-	S14[15]	-	-	-
IO_CLK	10	clk_32k<IO>	-	-	-	-	-	-	-	-	-	-	-	-
IO_CLK	355	pclkin_cif<IO>	-	-	-	-	-	-	-	-	-	-	-	-
isp	356	pclkin_cifinv	355	-	-	-	-	-	-	-	-	-	INVERT	-
isp	357	pclkin_cifmux	355	356	-	-	-	-	-	-	GRF20[9]	-	-	-
corel	11	clk_core_l_lpll_src	1	-	-	-	-	-	-	-	-	G0[0]	-	-
corel	12	clk_core_l_bpll_src	2	-	-	-	-	-	-	-	-	G0[1]	-	-
corel	13	clk_core_l_dpll_src	3	-	-	-	-	-	-	-	-	G0[2]	-	-
corel	14	clk_core_l_gpll_src	5	-	-	-	-	-	-	-	-	G0[3]	-	-
corel	15	clk_core_l	11	12	13	14	-	-	-	-	GF_S0[7:6]	-	S0[4:0]	-
corel	16	aclkm_core_l	15	-	-	-	-	-	-	-	-	G0[4]	ICG_S0[12:8]	-
corel	17	atclk_core_l	15	-	-	-	-	-	-	-	-	G0[5]	ICG_S1[4:0]	-
corel	18	pclk_dbg_core_l	15	-	-	-	-	-	-	-	-	G0[6]	ICG_S1[12:8]	-
corel	19	clk_pvtm_core_l	0	-	-	-	-	-	-	-	-	G0[7]	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
coreb	20	clk_core_b_lpll_src	1	-	-	-	-	-	-	-	-	G1[0]	-	-

	clk		parents (ID)											
coreb	21	clk_core_b_bpll_src	2	-	-	-	-	-	-	-	-	G1[1]	-	-
coreb	22	clk_core_b_dpll_src	3	-	-	-	-	-	-	-	-	G1[2]	-	-
coreb	23	clk_core_b_gpll_src	5	-	-	-	-	-	-	-	-	G1[3]	-	-
coreb	24	clk_core_b	20	21	22	23	-	-	-	-	GF_S2[7:6]	-	S2[4:0]	-
coreb	25	aclkm_core_b	24	-	-	-	-	-	-	-	-	G1[4]	ICG_S2[12:8]	-
coreb	26	atclk_core_b	24	-	-	-	-	-	-	-	-	G1[5]	ICG_S3[4:0]	-
coreb	27	pclk_dbg_core_b	24	-	-	-	-	-	-	-	-	G1[6]	S3[12:8]	-
coreb	28	pclken_dbg_core_b	27	-	-	-	-	-	-	-	-	-	ICG_S3[14:13]	-
coreb	29	clk_pvtm_core_b	0	-	-	-	-	-	-	-	-	G1[7]	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
gmac	30	aclk_gmac_cpll_src	4	-	-	-	-	-	-	-	-	G6[9]	-	-
gmac	31	aclk_gmac_gpll_src	5	-	-	-	-	-	-	-	-	G6[8]	-	-
gmac	32	aclk_gmac_pre	30	31	-	-	-	-	-	-	S20[7]	G6[10]	S20[4:0]	-
gmac	33	pclk_gmac_pre	32	-	-	-	-	-	-	-	-	G6[11]	S19[10:8]	-
gmac	34	clk_gmac	4	5	6	-	-	-	-	-	S20[15:14]	G5[5]	S20[12:8]	-
gmac	35	clk_rmii_src	34	48	-	-	-	-	-	-	S19[4]	-	-	-
gmac	36	clk_mac_refout	35	-	-	-	-	-	-	-	-	G5[6]	-	-
gmac	37	clk_mac_ref	35	-	-	-	-	-	-	-	-	~GRF5[6]|G5[7]	-	-
gmac	38	clk_rmii_rx_src	35	-	-	-	-	-	-	-	-	~GRF5[6]|G5[8]	-	-
gmac	39	clk_rmii_d2	38	-	-	-	-	-	-	-	-	-	F2	-
gmac	40	clk_rmii_d20	38	-	-	-	-	-	-	-	-	-	F20	-
gmac	41	clk_rmii_tx_src	35	-	-	-	-	-	-	-	-	G5[9]	-	-
gmac	42	clk_rmii_d5	41	-	-	-	-	-	-	-	-	-	F5	-

	clk		parents (ID)											
gmac	43	clk_rmii_d50	41	-	-	-	-	-	-	-	-	-	F50	-
gmac	44	clk_rmii_rx_mux	39	40	-	-	-	-	-	-	GRF5[3]	-	-	-
gmac	45	clk_rmii_tx_mux	41	-	43	42	-	-	-	-	GRF5[5:4]	-	-	-
gmac	46	clk_mac_rx	49	44	-	-	-	-	-	-	GRF5[6]	-	-	-
gmac	47	clk_mac_tx	45	44	-	-	-	-	-	-	GRF5[6]	-	-	-
IO_CLK	48	clkin_gmac<IO>	-	-	-	-	-	-	-	-	-	-	-	-
IO_CLK	49	gmac_phy_rx_clk<IO>	-	-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
i2s	50	clk_i2s0_div	4	5	-	-	-	-	-	-	S28[7]	G8[3]	S28[6:0]	-
i2s	51	clk_i2s0_frac	50	-	-	-	-	-	-	-	-	G8[4]	-	S96
i2s	52	clk_i2s0_mux	50	51	64	65	-	-	-	-	S28[9:8]	-	-	-
i2s	53	clk_i2s0	52	-	-	-	-	-	-	-	-	G8[5]	-	-
i2s	54	clk_i2s1_div	4	5	-	-	-	-	-	-	S29[7]	G8[6]	S29[6:0]	-
i2s	55	clk_i2s1_frac	54	-	-	-	-	-	-	-	-	G8[7]	-	S97
i2s	56	clk_i2s1_mux	54	55	64	65	-	-	-	-	S29[9:8]	-	-	-
i2s	57	clk_i2s1	56	-	-	-	-	-	-	-	-	G8[8]	-	-
i2s	58	clk_i2s2_div	4	5	-	-	-	-	-	-	S30[7]	G8[9]	S30[6:0]	-
i2s	59	clk_i2s2_frac	58	-	-	-	-	-	-	-	-	G8[10]	-	S98
i2s	60	clk_i2s2_mux	58	59	64	65	-	-	-	-	S30[9:8]	-	-	-
i2s	61	clk_i2s2	60	-	-	-	-	-	-	-	-	G8[11]	-	-
i2s	62	clk_i2sout_src	53	57	61	-	-	-	-	-	S31[1:0]	-	-	-
i2s	63	clk_i2sout	62	64	-	-	-	-	-	-	GF_S31[2]	G8[12]	-	-
i2s	64	clk_12m	0	-	-	-	-	-	-	-	-	-	F2	-

	clk		parents (ID)											
IO_CLK	65	clkin_i2s<IO>	-	-	-	-	-	-	-	-	-	-	-	-
i2s	66	clk_spdif_div	4	5	-	-	-	-	-	-	S32[7]	G8[13]	S32[6:0]	-
i2s	67	clk_spdif_frac	66	-	-	-	-	-	-	-	-	G8[14]	-	S99
i2s	68	clk_spdif	66	67	64	65	-	-	-	-	S32[14:13]	G8[15]	-	-
i2s	69	clk_spdif_rec_dptx	4	5	-	-	-	-	-	-	S32[15]	G10[6]	S32[12:8]	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
uart	70	clk_uart0_src	4	5	9	-	-	-	-	-	S33[13:12]	-	-	-
uart	71	clk_uart_src	4	5	-	-	-	-	-	-	S33[15]	-	-	-
uart	72	clk_uart0_div	70	-	-	-	-	-	-	-	-	G9[0]	S33[6:0]	-
uart	73	clk_uart0_frac	72	-	-	-	-	-	-	-	-	G9[1]	-	S100
uart	74	clk_uart0	72	73	0	-	-	-	-	-	S33[9:8]	-	-	-
uart	75	clk_uart1_div	71	-	-	-	-	-	-	-	-	G9[2]	S34[6:0]	-
uart	76	clk_uart1_frac	75	-	-	-	-	-	-	-	-	G9[3]	-	S101
uart	77	clk_uart1	75	76	0	-	-	-	-	-	S34[9:8]	-	-	-
uart	78	clk_uart2_div	71	-	-	-	-	-	-	-	-	G9[4]	S35[6:0]	-
uart	79	clk_uart2_frac	78	-	-	-	-	-	-	-	-	G9[5]	-	S102
uart	80	clk_uart2	78	79	0	-	-	-	-	-	S35[9:8]	-	-	-
uart	81	clk_uart3_div	71	-	-	-	-	-	-	-	-	G9[6]	S36[6:0]	-
uart	82	clk_uart3_frac	81	-	-	-	-	-	-	-	-	G9[7]	-	S103
uart	83	clk_uart3	81	82	0	-	-	-	-	-	S36[9:8]	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
ddrc	85	clk_ddrc_lpll_src	1	-	-	-	-	-	-	-	-	G3[0]	-	-
ddrc	86	clk_ddrc_bpll_src	2	-	-	-	-	-	-	-	-	G3[1]	-	-
ddrc	8	clk_ddrc_dpll	3	-	-	-	-	-	-	-	-	G3[2]	-	-

	clk		parents (ID)											
	7	_src												
ddrc	88	clk_ddrc_gpll_src	5	-	-	-	-	-	-	-	-	G3[3]	-	-
ddrc	89	clk_ddrc	85	86	87	88	-	-	-	-	S6[5:4]	-	S6[2:0]	-
ddrc	90	clk_ddrc_div2	89	-	-	-	-	-	-	-	-	-	F2	-
ddrc	91	pclk_ddr	4	5	-	-	-	-	-	-	S6[15]	G3[4]	S6[12:8]	-
ddrc	92	clk_pvtm_ddr	0	-	-	-	-	-	-	-	-	G4[11]	-	-
ddrc	93	clk_dfimon0_timer	0	-	-	-	-	-	-	-	-	G3[5]	-	-
ddrc	94	clk_dfimon1_timer	0	-	-	-	-	-	-	-	-	G3[6]	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
cci	95	aclk_cci_cpll_src	4	-	-	-	-	-	-	-	-	G2[0]	-	-
cci	96	aclk_cci_gpll_src	5	-	-	-	-	-	-	-	-	G2[1]	-	-
cci	97	aclk_cci_npll_src	6	-	-	-	-	-	-	-	-	G2[2]	-	-
cci	98	aclk_cci_vpll_src	7	-	-	-	-	-	-	-	-	G2[3]	-	-
cci	99	aclk_cci_pre	95	96	97	98	-	-	-	-	GF_S5[7:6]	G2[4]	S5[4:0]	-
cci	100	clk_cci_trace_cpll_src	4	-	-	-	-	-	-	-	-	G2[5]	-	-
cci	101	clk_cci_trace_gpll_src	5	-	-	-	-	-	-	-	-	G2[6]	-	-
cci	102	clk_cci_trace	100	101	-	-	-	-	-	-	GF_S5[15]	G2[7]	S5[12:8]	-
cci	103	clk_cs_cpll_src	4	-	-	-	-	-	-	-	-	G2[8]	-	-
cci	104	clk_cs_gpll_src	5	-	-	-	-	-	-	-	-	G2[9]	-	-
cci	105	clk_cs_npll_src	6	-	-	-	-	-	-	-	-	G2[10]	-	-
cci	1	clk_cs	1	10	1	-	-	-	-	-	GF_S4[7:	-	S4[4:0]	-

	clk		parents (ID)											
	06		03	4	05						6]			
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
vcodec	110	aclk_vcodec_pre	4	5	6	8	-	-	-	-	S7[7:6]	G4[0]	S7[4:0]	-
vcodec	111	hclk_vcodec_pre	110	-	-	-	-	-	-	-	-	G4[1]	S7[12:8]	-
vdu	112	aclk_vdu_pre	4	5	6	8	-	-	-	-	S8[7:6]	G4[2]	S8[4:0]	-
vdu	113	hclk_vdu_pre	112	-	-	-	-	-	-	-	-	G4[3]	S8[12:8]	-
vdu	114	clk_vdu_core	4	5	6	-	-	-	-	-	S9[7:6]	G4[4]	S9[4:0]	-
vdu	115	clk_vdu_ca	4	5	6	-	-	-	-	-	S9[15:14]	G4[5]	S9[12:8]	-
iep	116	aclk_iep_pre	4	5	6	8	-	-	-	-	S10[7:6]	G4[6]	S10[4:0]	-
iep	117	hclk_iep_pre	116	-	-	-	-	-	-	-	-	G4[7]	S10[12:8]	-
rga	118	aclk_rga_pre	4	5	6	8	-	-	-	-	S11[7:6]	G4[8]	S11[4:0]	-
rga	119	hclk_rga_pre	118	-	-	-	-	-	-	-	-	G4[9]	S11[12:8]	-
rga	120	clk_rga_core	4	5	6	8	-	-	-	-	S12[7:6]	G4[10]	S12[4:0]	-
center	121	aclk_center	4	5	6	-	-	-	-	-	GF_S12[15:14]	G3[7]	S12[12:8]	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
gpu	123	aclk_gpu_pre	8	4	5	6	9	-	-	-	GF_S13[7:5]	G13[0]	S13[4:0]	-
gpu	12	clk_pvtm_gpu	0	-	-	-	-	-	-	-	-	G13[1]	-	-

	clk		parents (ID)											
	4													
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
perihp	126	aclk_perihp_gpll_src	5	-	-	-	-	-	-	-	-	G5[0]	-	-
perihp	125	aclk_perihp_cpll_src	4	-	-	-	-	-	-	-	-	G5[1]	-	-
perihp	127	aclk_perihp	125	126	-	-	-	-	-	-	GF_S14[7]	G5[2]	S14[4:0]	-
perihp	128	hclk_perihp	127	-	-	-	-	-	-	-	-	G5[3]	S14[9:8]	-
perihp	129	pclk_perihp	127	-	-	-	-	-	-	-	-	G5[4]	S14[14:12]	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
usbphy	130	clk_usbphy0_480m<PHY>	-	-	-	-	-	-	-	-	-	-	-	-
usbphy	131	clk_usbphy1_480m<PHY>	-	-	-	-	-	-	-	-	-	-	-	-
usbphy	330	clk_usbphy0_480m_src	130	-	-	-	-	-	-	-	-	G13[12]	-	-
usbphy	331	clk_usbphy1_480m_src	131	-	-	-	-	-	-	-	-	G13[12]	-	-
usbphy	132	clk_usbphy_480m	330	331	-	-	-	-	-	-	S14[6]	-	-	-
usbphy	133	clk_hsicphy	4	5	6	132	-	-	-	-	S19[1:0]	G6[4]	-	-
usbphy	310	clk_usb2phy0_ref	0	-	-	-	-	-	-	-	-	G6[5]	-	-
usbphy	311	clk_usb2phy1_ref	0	-	-	-	-	-	-	-	-	G6[6]	-	-
usbphy	185	clk_uphy0_tcpdphy_ref	0	10	-	-	-	-	-	-	GF_S64[15]	G13[4]	S64[12:8]	-

	clk		parents (ID)											
usbphy	186	clk_uphy0_tcpdcore	0	10	4	5	-	-	-	-	GF_S64[7:6]	G13[5]	S64[4:0]	-
usbphy	187	clk_uphy1_tcpdphy_ref	0	10	-	-	-	-	-	-	GF_S65[15]	G13[6]	S65[12:8]	-
usbphy	188	clk_uphy1_tcpdcore	0	10	4	5	-	-	-	-	GF_S65[7:6]	G13[7]	S65[4:0]	-
usbphy	180	aclk_usb3	4	5	6	-	-	-	-	-	S39[7:6]	G12[0]	S39[4:0]	-
usbphy	183	clk_usb3otg0_suspend	0	10	-	-	-	-	-	-	S40[15]	G12[3]	S40[9:0]	-
usbphy	184	clk_usb3otg1_suspend	0	10	-	-	-	-	-	-	S41[15]	G12[4]	S41[9:0]	-
usbphy	181	clk_usb3otg0_ref	0	-	-	-	-	-	-	-	-	G12[1]	-	-
usbphy	182	clk_usb3otg1_ref	0	-	-	-	-	-	-	-	-	G12[2]	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
sd	325	hclk_sd	4	5	-	-	-	-	-	-	S13[15]	G12[13]	S13[12:8]	-
sd	135	clk_sdio	4	5	6	8	9	0	-	-	S15[10:8]	G6[0]	S15[6:0]	-
sd	136	clk_sdmmc	4	5	6	8	9	0	-	-	S16[10:8]	G6[1]	S16[6:0]	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
pcie	137	clk_pcie_pm	4	5	6	0	-	-	-	-	S17[10:8]	G6[2]	S17[6:0]	-
pcie	138	clk_pciephy_ref100m	6	-	-	-	-	-	-	-	-	G12[6]	S18[15:11]	-
pcie	139	clk_pciephy_ref	0	138	-	-	-	-	-	-	S18[10]	-	-	-
pcie	1	clk_pcie_core	4	5	6	-	-	-	-	-	S18[9:8]	G6[3]	S18[6:0]	-

	clk		parents (ID)											
	40	_cru												
pcie	141	clk_pcie_core_phy<PHY>	-	-	-	-	-	-	-	-	-	-	-	-
pcie	142	clk_pcie_core	140	141	-	-	-	-	-	-	S18[7]	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
emmc	146	aclk_emmc_gpll_src	5	-	-	-	-	-	-	-	-	G6[12]	-	-
emmc	145	aclk_emmc_cpll_src	4	-	-	-	-	-	-	-	-	G6[13]	-	-
emmc	147	aclk_emmc	145	146	-	-	-	-	-	-	S21[7]	-	S21[4:0]	-
emmc	148	clk_emmc	4	5	6	9	0	-	-	-	S22[10:8]	G6[14]	S22[6:0]	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
perilp0	150	aclk_perilp0_cpll_src	4	-	-	-	-	-	-	-	-	G7[1]	-	-
perilp0	151	aclk_perilp0_gpll_src	5	-	-	-	-	-	-	-	-	G7[0]	-	-
perilp0	152	aclk_perilp0	150	151	-	-	-	-	-	-	GF_S23[7]	G7[2]	S23[4:0]	-
perilp0	153	hclk_perilp0	152	-	-	-	-	-	-	-	-	G7[3]	ICG_S23[9:8]	-
perilp0	154	pclk_perilp0	152	-	-	-	-	-	-	-	-	G7[4]	ICG_S23[14:12]	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
crypto	155	clk_crypto0	4	5	8	-	-	-	-	-	S24[7:6]	G7[7]	S24[4:0]	-
crypto	156	clk_crypto1	4	5	8	-	-	-	-	-	S26[7:6]	G7[8]	S26[4:0]	-
cm0s_p	1	fclk_cm0s_cpl	4	-	-	-	-	-	-	-	-	G7[6]	-	-

	clk		parents (ID)											
erilp	57	l_src												
cm0s_perilp	158	fclk_cm0s_gpll_src	5	-	-	-	-	-	-	-	-	G7[5]	-	-
cm0s_perilp	159	fclk_cm0s	157	158	-	-	-	-	-	-	GF_S24[15]	G7[9]	S24[12:8]	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
perilp1	160	hclk_perilp1_cpll_src	4	-	-	-	-	-	-	-	-	G8[1]	-	-
perilp1	161	hclk_perilp1_gpll_src	5	-	-	-	-	-	-	-	-	G8[0]	-	-
perilp1	162	hclk_perilp1	160	161	-	-	-	-	-	-	GF_S25[7]	-	S25[4:0]	-
perilp1	163	pclk_perilp1	162	-	-	-	-	-	-	-	-	G8[2]	ICG_S25[10:8]	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
saradc	165	clk_saradc	0	-	-	-	-	-	-	-	-	G9[11]	S26[15:8]	-
tsadc	166	clk_tsadc	0	10	-	-	-	-	-	-	S27[15]	G9[10]	S27[9:0]	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
cif_testout	173	clk_testout1_pll_src	4	5	6	-	-	-	-	-	S38[7:6]	-	-	-
cif_testout	174	clk_testout1	173	0	-	-	-	-	-	-	S38[5]	G13[14]	S38[4:0]	-
cif_testout	178	clk_testout2_pll_src	4	5	6	-	-	-	-	-	S38[15:14]	-	-	-
cif_testout	179	clk_testout2	178	0	-	-	-	-	-	-	S38[13]	G13[15]	S38[12:8]	-
cif_testout	172	clk_testout2_2io	179	1011	-	-	-	-	-	-	PS4[15]	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

	clk		parents (ID)											
vio	190	aclk_vio	4	5	8	-	-	-	-	-	S42[7:6]	G11[0]	S42[4:0]	-
vio	191	pclk_vio	190	-	-	-	-	-	-	-	-	G11[1]	ICG_S43[4:0]	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
hdcp	193	aclk_hdcp	4	5	8	-	-	-	-	-	S42[15:14]	G11[2]	S42[12:8]	-
hdcp	194	hclk_hdcp	193	-	-	-	-	-	-	-	-	G11[3]	S43[9:5]	-
hdcp	195	pclk_hdcp	193	-	-	-	-	-	-	-	-	G11[10]	S43[14:10]	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
edp	197	pclk_edp	4	5	-	-	-	-	-	-	S44[15]	G11[11]	S44[13:8]	-
edp	201	clk_dp_core	6	4	5	-	-	-	-	-	S46[7:6]	G11[8]	S46[4:0]	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
hdmi	199	clk_hdmi_cec	0	10	-	-	-	-	-	-	S45[15]	G11[7]	S45[9:0]	-
hdmi	200	clk_hdmi_sfr	0	-	-	-	-	-	-	-	-	G11[6]	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
vop0	203	aclk_vop0_pre	7	4	5	6	-	-	-	-	GF_S47[7:6]	G10[8]	S47[4:0]	-
vop0	204	hclk_vop0_pre	203	-	-	-	-	-	-	-	-	G10[9]	S47[12:8]	-
vop1	205	aclk_vop1_pre	7	4	5	6	-	-	-	-	GF_S48[7:6]	G10[10]	S48[4:0]	-
vop1	206	hclk_vop1_pre	205	-	-	-	-	-	-	-	-	G10[11]	S48[12:8]	-
vop0	20	dclk_vop0_div	7	4	5	-	-	-	-	-	GF_S49[9:8]	G10[12]	S49[7:0]	-

	clk		parents (ID)											
	7													
vop0	208	dclk_vop0_frac	207	-	-	-	-	-	-	-	-	-	-	S106
vop0	209	dclk_vop0	207	208	-	-	-	-	-	-	S49[11]	-	-	-
vop1	210	dclk_vop1_div	7	4	5	-	-	-	-	-	GF_S50[9:8]	G10[13]	S50[7:0]	-
vop1	211	dclk_vop1_frac	210	-	-	-	-	-	-	-	-	-	-	S107
vop1	212	dclk_vop1	210	211	-	-	-	-	-	-	S50[11]	-	-	-
vop0	214	clk_vop0_pwm	7	4	5	0	-	-	-	-	GF_S51[7:6]	G10[14]	S51[4:0]	-
vop1	215	clk_vop1_pwm	7	4	5	0	-	-	-	-	GF_S52[7:6]	G10[15]	S52[4:0]	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
isp	217	aclk_isp0	4	5	8	-	-	-	-	-	S53[7:6]	G12[8]	S53[4:0]	-
isp	218	hclk_isp0	217	-	-	-	-	-	-	-	-	G12[9]	S53[12:8]	-
isp	219	clk_isp0	4	5	6	-	-	-	-	-	S55[7:6]	G11[4]	S55[4:0]	-
isp	221	aclk_isp1	4	5	8	-	-	-	-	-	S54[7:6]	G12[10]	S54[4:0]	-
isp	222	hclk_isp1	221	-	-	-	-	-	-	-	-	G12[11]	S54[12:8]	-
isp	223	clk_isp1	4	5	6	-	-	-	-	-	S55[15:14]	G11[5]	S55[12:8]	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
cif	225	clk_cifout_pll_src	4	5	6	-	-	-	-	-	S56[7:6]	G10[7]	-	-

	clk		parents (ID)											
cif	226	clk_cifout	225	0	-	-	-	-	-	-	S56[5]	-	S56[4:0]	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
gic	228	aclk_gic_pre	4	5	-	-	-	-	-	-	S56[15]	G12[12]	S56[12:8]	-
alive	230	pclk_alive_gpll_src	5	-	-	-	-	-	-	-	-	PMUGRF0[6]	-	-
alive	231	pclk_alive	230	-	-	-	-	-	-	-	-	-	S57[4:0]	-
testout	234	clk_test_frac	4	5	-	-	-	-	-	-	S58[7]	G13[9]	-	S105
testout	235	clk_test_24m	0	-	-	-	-	-	-	-	-	-	S57[15:6]	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
spi	240	clk_spi0	4	5	-	-	-	-	-	-	S59[7]	G9[12]	S59[6:0]	-
spi	241	clk_spi1	4	5	-	-	-	-	-	-	S59[15]	G9[13]	S59[14:8]	-
spi	242	clk_spi2	4	5	-	-	-	-	-	-	S60[7]	G9[14]	S60[6:0]	-
spi	243	clk_spi4	4	5	-	-	-	-	-	-	S60[15]	G9[15]	S60[14:8]	-
spi	244	clk_spi5	4	5	-	-	-	-	-	-	S58[15]	G13[13]	S58[14:8]	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
i2c	250	clk_i2c1	4	5	-	-	-	-	-	-	S61[7]	G10[0]	S61[6:0]	-
i2c	252	clk_i2c2	4	5	-	-	-	-	-	-	S62[7]	G10[2]	S62[6:0]	-
i2c	254	clk_i2c3	4	5	-	-	-	-	-	-	S63[7]	G10[4]	S63[6:0]	-

	clk		parents (ID)											
i2c	251	clk_i2c5	4	5	-	-	-	-	-	-	S61[15]	G10[1]	S61[14:8]	-
i2c	253	clk_i2c6	4	5	-	-	-	-	-	-	S62[15]	G10[3]	S62[14:8]	-
i2c	255	clk_i2c7	4	5	-	-	-	-	-	-	S63[15]	G10[5]	S63[14:8]	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
alive	260	clk_mipidphy_ref	0	-	-	-	-	-	-	-	-	G11[14]	-	-
alive	261	clk_mipidphy_cfg	0	-	-	-	-	-	-	-	-	G11[15]	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
timer	340	clk_timer0	0	-	-	-	-	-	-	-	-	G26[0]	-	-
timer	341	clk_timer1	0	-	-	-	-	-	-	-	-	G26[1]	-	-
timer	342	clk_timer2	0	-	-	-	-	-	-	-	-	G26[2]	-	-
timer	343	clk_timer3	0	-	-	-	-	-	-	-	-	G26[3]	-	-
timer	344	clk_timer4	0	-	-	-	-	-	-	-	-	G26[4]	-	-
timer	345	clk_timer5	0	-	-	-	-	-	-	-	-	G26[5]	-	-
timer	346	clk_timer6	0	-	-	-	-	-	-	-	-	G26[6]	-	-
timer	347	clk_timer7	0	-	-	-	-	-	-	-	-	G26[7]	-	-
timer	348	clk_timer8	0	-	-	-	-	-	-	-	-	G26[8]	-	-
timer	3	clk_timer9	0	-	-	-	-	-	-	-	-	G26[9]	-	-

	clk		parents (ID)											
	49													
timer	350	clk_timer10	0	-	-	-	-	-	-	-	-	G26[10]	-	-
timer	351	clk_timer11	0	-	-	-	-	-	-	-	-	G26[11]	-	-

	clk		parents (ID)																		
MODULE	ID	CLKNAME	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	MUX	GATE	DIV	FRAC
test	232	clk_test	24	15	9	27	52	62	21	89	23	20	14	38	09	01	35	34	M[3:0]	G13[11]	S58[4:0]	-

Fig. 3-3 RK3399 CRU Clock Architecture Diagram

	clk		parents (ID)											
MODULE	ID	CLKNAME	0	1	2	3	4	5	6	7	MUX	GATE	DIV	FRAC
coreb	500	clk_dbg_pd_core_b	24	-	-	-	-	-	-	-	-	G14[1]	-	-
coreb	501	pclk_dbg_cxcs_pd_core_b	27	-	-	-	-	-	-	-	-	G14[2]	-	-
coreb	502	aclk_core_adb400_gic_2_core_b	24	-	-	-	-	-	-	-	-	G14[3]	-	-
coreb	503	aclk_core_adb400_core_b_2_gic	24	-	-	-	-	-	-	-	-	G14[4]	-	-
coreb	504	aclk_core_adb400_core_b_2_cci500	25	-	-	-	-	-	-	-	-	G14[5]	-	-
coreb	505	aclk_perf_core_b	25	-	-	-	-	-	-	-	-	G14[6]	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
corel	508	clk_dbg_pd_core_l	15	-	-	-	-	-	-	-	-	G14[9]	-	-
corel	509	aclk_core_adb400_gic_2_core_l	15	-	-	-	-	-	-	-	-	G14[10]	-	-
corel	510	aclk_core_adb400_core_l_2_gic	15	-	-	-	-	-	-	-	-	G14[11]	-	-
corel	511	aclk_core_adb400_core_l_2_cci500	16	-	-	-	-	-	-	-	-	G14[12]	-	-
corel	512	aclk_perf_core_l	16	-	-	-	-	-	-	-	-	G14[13]	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
cci	515	aclk_adb400m_pd_core_l	99	-	-	-	-	-	-	-	-	G15[0]	-	-
cci	516	aclk_adb400m_pd_core_b	99	-	-	-	-	-	-	-	-	G15[1]	-	-
cci	517	aclk_cci	99	-	-	-	-	-	-	-	-	G15[2]	-	-
cci	518	aclk_cci_noc0	99	-	-	-	-	-	-	-	-	G15[3]	-	-
cci	519	aclk_cci_noc1	99	-	-	-	-	-	-	-	-	G15[4]	-	-

	clk		parents (ID)											
cci	520	clk_dbg_cxcs	106	-	-	-	-	-	-	-	-	G15[5]	-	-
cci	521	clk_dbg_noc	106	-	-	-	-	-	-	-	-	G15[6]	-	-
cci	522	aclk_cci_grf	99	-	-	-	-	-	-	-	-	G15[7]	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
iep	525	aclk_iep	116	-	-	-	-	-	-	-	-	G16[0]	-	-
iep	526	aclk_iep_noc	116	-	-	-	-	-	-	-	-	G16[1]	-	-
iep	527	hclk_iep	117	-	-	-	-	-	-	-	-	G16[2]	-	-
iep	528	hclk_iep_noc	117	-	-	-	-	-	-	-	-	G16[3]	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
rga	530	aclk_rga	118	-	-	-	-	-	-	-	-	G16[8]	-	-
rga	531	aclk_rga_noc	118	-	-	-	-	-	-	-	-	G16[9]	-	-
rga	532	hclk_rga	119	-	-	-	-	-	-	-	-	G16[10]	-	-
rga	533	hclk_rga_noc	119	-	-	-	-	-	-	-	-	G16[11]	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
vcodec	535	aclk_vcodec	110	-	-	-	-	-	-	-	-	G17[0]	-	-
vcodec	536	aclk_vcodec_noc	110	-	-	-	-	-	-	-	-	G17[1]	-	-
vcodec	537	hclk_vcodec	111	-	-	-	-	-	-	-	-	G17[2]	-	-
vcodec	538	hclk_vcodec_noc	111	-	-	-	-	-	-	-	-	G17[3]	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
vdu	540	aclk_vdu	112	-	-	-	-	-	-	-	-	G17[8]	-	-
vdu	541	aclk_vdu_noc	112	-	-	-	-	-	-	-	-	G17[9]	-	-
vdu	542	hclk_vdu	113	-	-	-	-	-	-	-	-	G17[10]	-	-
vdu	543	hclk_vdu_noc	113	-	-	-	-	-	-	-	-	G17[11]	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
ddrc	545	clk_ddr0_msch	90	-	-	-	-	-	-	-	-	G18[0]	-	-
ddrc	546	clk_ddrc0	90	-	-	-	-	-	-	-	-	G18[1]	-	-
ddrc	547	clk_ddrphy_ctrl0	90	-	-	-	-	-	-	-	-	G18[2]	-	-
ddrc	548	clk_ddrphy0	90	-	-	-	-	-	-	-	-	G18[3]	-	-
ddrc	549	clk_ddrcfg_msch0	90	-	-	-	-	-	-	-	-	G18[4]	-	-
ddrc	550	clk_ddr1_msch	90	-	-	-	-	-	-	-	-	G18[5]	-	-
ddrc	551	clk_ddrc1	90	-	-	-	-	-	-	-	-	G18[6]	-	-
ddrc	552	clk_ddrphy_ctrl1	90	-	-	-	-	-	-	-	-	G18[7]	-	-
ddrc	553	clk_ddrphy1	90	-	-	-	-	-	-	-	-	G18[8]	-	-
ddrc	554	clk_ddrcfg_msch1	90	-	-	-	-	-	-	-	-	G18[9]	-	-
ddrc	555	pclk_center_main_noc	91	-	-	-	-	-	-	-	-	G18[10]	-	-
ddrc	556	clk_ddr_cic	90	-	-	-	-	-	-	-	-	G18[11]	-	-
ddrc	557	pclk_ddr_mon	91	-	-	-	-	-	-	-	-	G18[12]	-	-
ddrc	558	clk_ddr_mon	90	-	-	-	-	-	-	-	-	G18[13]	-	-
ddrc	559	clk_ddr_mon_timer	0	-	-	-	-	-	-	-	-	G18[14]	-	-
ddrc	560	pclk_cic	91	-	-	-	-	-	-	-	-	G18[15]	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
center	562	aclk_center_main_noc	121	-	-	-	-	-	-	-	-	G19[0]	-	-
center	563	aclk_center_peri_noc	121	-	-	-	-	-	-	-	-	G19[1]	-	-
ddrc	564	pclk_ddr_sgrf	91	-	-	-	-	-	-	-	-	G19[2]	-	-

	clk		parents (ID)											
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
perihp	566	aclk_perf_pcie	127	-	-	-	-	-	-	-	-	G20[2]	-	-
perihp	567	pclk_perihp_grf	129	-	-	-	-	-	-	-	-	G20[4]	-	-
perihp	568	hclk_host0	128	-	-	-	-	-	-	-	-	G20[5]	-	-
perihp	569	hclk_host0_arb	128	-	-	-	-	-	-	-	-	G20[6]	-	-
perihp	570	hclk_host1	128	-	-	-	-	-	-	-	-	G20[7]	-	-
perihp	571	hclk_host1_arb	128	-	-	-	-	-	-	-	-	G20[8]	-	-
perihp	572	hclk_hsic	128	-	-	-	-	-	-	-	-	G20[9]	-	-
perihp	573	aclk_pcie	127	-	-	-	-	-	-	-	-	G20[10]	-	-
perihp	574	pclk_pcie	129	-	-	-	-	-	-	-	-	G20[11]	-	-
perihp	575	aclk_perihp_noc	127	-	-	-	-	-	-	-	-	G20[12]	-	-
perihp	576	hclk_perihp_noc	128	-	-	-	-	-	-	-	-	G20[13]	-	-
perihp	577	pclk_perihp_noc	129	-	-	-	-	-	-	-	-	G20[14]	-	-
perihp	578	hclk_ahb1tom	128	-	-	-	-	-	-	-	-	G20[15]	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
alive	581	clk_dphy_pll	260	-	-	-	-	-	-	-	-	G21[0]	-	-
alive	582	clk_dphy_tx0_cfg	261	-	-	-	-	-	-	-	-	G21[1]	-	-
alive	583	clk_dphy_tx1rx1_cfg	261	-	-	-	-	-	-	-	-	G21[2]	-	-
alive	584	clk_dphy_rx0_cfg	261	-	-	-	-	-	-	-	-	G21[3]	-	-
alive	585	pclk_uphy_mux_g	231	-	-	-	-	-	-	-	-	G21[4]	-	-
alive	586	pclk_uphy0_tcphy_g	231	-	-	-	-	-	-	-	-	G21[5]	-	-
alive	587	pclk_uphy0_tcpd_g	231	-	-	-	-	-	-	-	-	G21[6]	-	-
alive	588	pclk_uphy1_tcphy_g	231	-	-	-	-	-	-	-	-	G21[8]	-	-
alive	589	pclk_uphy1_tcpd_g	231	-	-	-	-	-	-	-	-	G21[9]	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
perilp1	591	pclk_uart0	163	-	-	-	-	-	-	-	-	G22[0]	-	-
perilp1	592	pclk_uart1	163	-	-	-	-	-	-	-	-	G22[1]	-	-
perilp1	593	pclk_uart2	163	-	-	-	-	-	-	-	-	G22[2]	-	-
perilp1	594	pclk_uart3	163	-	-	-	-	-	-	-	-	G22[3]	-	-
perilp1	595	pclk_rki2c7	163	-	-	-	-	-	-	-	-	G22[5]	-	-
perilp1	596	pclk_rki2c1	163	-	-	-	-	-	-	-	-	G22[6]	-	-
perilp1	597	pclk_rki2c5	163	-	-	-	-	-	-	-	-	G22[7]	-	-
perilp1	598	pclk_rki2c6	163	-	-	-	-	-	-	-	-	G22[8]	-	-
perilp1	599	pclk_rki2c2	163	-	-	-	-	-	-	-	-	G22[9]	-	-
perilp1	600	pclk_rki2c3	163	-	-	-	-	-	-	-	-	G22[10]	-	-
perilp1	601	pclk_mailbox0	163	-	-	-	-	-	-	-	-	G22[11]	-	-
perilp1	602	pclk_saradc	163	-	-	-	-	-	-	-	-	G22[12]	-	-
perilp1	603	pclk_tsadc	163	-	-	-	-	-	-	-	-	G22[13]	-	-
perilp1	604	pclk_efuse1024ns	163	-	-	-	-	-	-	-	-	G22[14]	-	-
perilp1	605	pclk_efuse1024s	163	-	-	-	-	-	-	-	-	G22[15]	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
perilp0	607	aclk_intmem	152	-	-	-	-	-	-	-	-	G23[0]	-	-
perilp0	608	aclk_tzma	152	-	-	-	-	-	-	-	-	G23[1]	-	-
perilp0	609	clk_intmem0	152	-	-	-	-	-	-	-	-	G23[2]	-	-

	clk		parents (ID)											
perilp0	610	clk_intmem1	152	-	-	-	-	-	-	-	-	G23[3]	-	-
perilp0	611	clk_intmem2	152	-	-	-	-	-	-	-	-	G23[4]	-	-
perilp0	612	clk_intmem3	152	-	-	-	-	-	-	-	-	G23[5]	-	-
perilp0	613	clk_intmem4	152	-	-	-	-	-	-	-	-	G23[6]	-	-
perilp0	614	clk_intmem5	152	-	-	-	-	-	-	-	-	G23[7]	-	-
perilp0	615	aclk_dcf	152	-	-	-	-	-	-	-	-	G23[8]	-	-
perilp0	616	pclk_dcf	154	-	-	-	-	-	-	-	-	G23[9]	-	-
perilp1	617	pclk_spi0	163	-	-	-	-	-	-	-	-	G23[10]	-	-
perilp1	618	pclk_spi1	163	-	-	-	-	-	-	-	-	G23[11]	-	-
perilp1	619	pclk_spi2	163	-	-	-	-	-	-	-	-	G23[12]	-	-
perilp1	620	pclk_spi4	163	-	-	-	-	-	-	-	-	G23[13]	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
perilp0	622	hclk_rom	153	-	-	-	-	-	-	-	-	G24[4]	-	-
perilp0	623	hclk_m_crypto0	153	-	-	-	-	-	-	-	-	G24[5]	-	-
perilp0	624	hclk_s_crypto0	153	-	-	-	-	-	-	-	-	G24[6]	-	-
cm0s_perilp	625	sclk_m0_perilp	159	-	-	-	-	-	-	-	-	G24[8]	-	-
cm0s_perilp	626	hclk_m0_perilp	159	-	-	-	-	-	-	-	-	G24[9]	-	-
cm0s_perilp	627	dclk_m0_perilp	159	-	-	-	-	-	-	-	-	G24[10]	-	-
cm0s_perilp	628	clk_m0_perilp_dec	159	-	-	-	-	-	-	-	-	G24[11]	-	-
perilp1	629	pclk_perilp_sgrf	163	-	-	-	-	-	-	-	-	G24[13]	-	-
perilp0	630	hclk_m_crypto1	153	-	-	-	-	-	-	-	-	G24[14]	-	-
perilp0	631	hclk_s_crypto1	153	-	-	-	-	-	-	-	-	G24[15]	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
perilp0	634	aclk_dmac0_perilp	152	-	-	-	-	-	-	-	-	G25[5]	-	-
perilp0	635	aclk_dmac1_perilp	152	-	-	-	-	-	-	-	-	G25[6]	-	-
perilp0	636	aclk_perilp0_noc	152	-	-	-	-	-	-	-	-	G25[7]	-	-
perilp0	637	hclk_perilp0_noc	153	-	-	-	-	-	-	-	-	G25[8]	-	-
perilp1	638	hclk_perilp1_noc	162	-	-	-	-	-	-	-	-	G25[9]	-	-
perilp1	639	pclk_perilp1_noc	163	-	-	-	-	-	-	-	-	G25[10]	-	-
cm0s_perilp	640	hclk_m0_perilp_noc	159	-	-	-	-	-	-	-	-	G25[11]	-	-
perilp1	641	hclk_sdio_noc	162	-	-	-	-	-	-	-	-	G25[12]	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
isp	643	hclk_isp0_noc	218	-	-	-	-	-	-	-	-	G27[0]	-	-
isp	644	aclk_isp0_noc	217	-	-	-	-	-	-	-	-	G27[1]	-	-
isp	645	hclk_isp1_noc	222	-	-	-	-	-	-	-	-	G27[2]	-	-
isp	646	aclk_isp1_noc	221	-	-	-	-	-	-	-	-	G27[3]	-	-
isp	647	hclk_isp0_wrapper	218	-	-	-	-	-	-	-	-	G27[4]	-	-
isp	648	aclk_isp0_wrapper	217	-	-	-	-	-	-	-	-	G27[5]	-	-
isp	649	pclkin_isp1_wrapper	357	-	-	-	-	-	-	-	-	G27[6]	-	-
isp	650	hclk_isp1_wrapper	217	-	-	-	-	-	-	-	-	G27[7]	-	-

	clk		parents (ID)											
isp	651	aclk_isp1_wrapper	222	-	-	-	-	-	-	-	-	G27[8]	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
vop0	653	hclk_vop0_noc	204	-	-	-	-	-	-	-	-	G28[0]	-	-
vop0	654	aclk_vop0_noc	203	-	-	-	-	-	-	-	-	G28[1]	-	-
vop0	655	hclk_vop0	204	-	-	-	-	-	-	-	-	G28[2]	-	-
vop0	656	aclk_vop0	203	-	-	-	-	-	-	-	-	G28[3]	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
vop1	658	hclk_vop1_noc	206	-	-	-	-	-	-	-	-	G28[4]	-	-
vop1	659	aclk_vop1_noc	205	-	-	-	-	-	-	-	-	G28[5]	-	-
vop1	660	hclk_vop1	206	-	-	-	-	-	-	-	-	G28[6]	-	-
vop1	661	aclk_vop1	205	-	-	-	-	-	-	-	-	G28[7]	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
vio	663	aclk_vio_noc	190	-	-	-	-	-	-	-	-	G29[0]	-	-
vio	664	pclk_mipi_dsi0	191	-	-	-	-	-	-	-	-	G29[1]	-	-
vio	665	pclk_mipi_dsi1	191	-	-	-	-	-	-	-	-	G29[2]	-	-
hdcp	666	pclk_hdcp_noc	195	-	-	-	-	-	-	-	-	G29[3]	-	-
hdcp	667	aclk_hdcp_noc	193	-	-	-	-	-	-	-	-	G29[4]	-	-
hdcp	668	hclk_hdcp_noc	194	-	-	-	-	-	-	-	-	G29[5]	-	-
hdcp	669	pclk_hdmi_ctrl	195	-	-	-	-	-	-	-	-	G29[6]	-	-
hdcp	670	pclk_dp_ctrl	195	-	-	-	-	-	-	-	-	G29[7]	-	-
hdcp	671	pclk_hdcp22	195	-	-	-	-	-	-	-	-	G29[8]	-	-
hdcp	672	hclk_hdcp22	194	-	-	-	-	-	-	-	-	G29[9]	-	-
hdcp	673	aclk_hdcp22	193	-	-	-	-	-	-	-	-	G29[10]	-	-
hdcp	674	pclk_gasket	195	-	-	-	-	-	-	-	-	G29[11]	-	-
vio	675	pclk_vio_grf	191	-	-	-	-	-	-	-	-	G29[12]	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
usbphy	677	aclk_usb3_noc	180	-	-	-	-	-	-	-	-	G30[0]	-	-
usbphy	678	aclk_usb3otg0	180	-	-	-	-	-	-	-	-	G30[1]	-	-
usbphy	679	aclk_usb3otg1	180	-	-	-	-	-	-	-	-	G30[2]	-	-
usbphy	680	aclk_usb3_rksoc_axi_perf	180	-	-	-	-	-	-	-	-	G30[3]	-	-
usbphy	681	aclk_usb3_grf	180	-	-	-	-	-	-	-	-	G30[4]	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
gpu	683	aclk_gpu	123	-	-	-	-	-	-	-	-	G30[8]	-	-
gpu	684	aclk_perf_gpu	123	-	-	-	-	-	-	-	-	G30[10]	-	-
gpu	685	aclk_gpu_grf	123	-	-	-	-	-	-	-	-	G30[11]	-	-
-	-	-		-	-	-	-	-	-	-	-	-	-	-
alive	687	pclk_grf	231	-	-	-	-	-	-	-	-	G31[1]	-	-
alive	688	pclk_intr_arb	231	-	-	-	-	-	-	-	-	G31[2]	-	-
alive	689	pclk_gpio2	231	-	-	-	-	-	-	-	-	G31[3]	-	-
alive	690	pclk_gpio3	231	-	-	-	-	-	-	-	-	G31[4]	-	-
alive	691	pclk_gpio4	231	-	-	-	-	-	-	-	-	G31[5]	-	-
alive	692	pclk_timer0	231	-	-	-	-	-	-	-	-	G31[6]	-	-
alive	693	pclk_timer1	231	-	-	-	-	-	-	-	-	G31[7]	-	-
perihp	694	pclk_hsicphy	129	-	-	-	-	-	-	-	-	G31[8]	-	-

	clk		parents (ID)											
alive	695	pclk_pmu_intr_arb	231	-	-	-	-	-	-	-	-	G31[9]	-	-
alive	696	pclk_sgrf	231	-	-	-	-	-	-	-	-	G31[10]	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
gmac	698	aclk_gmac	32	-	-	-	-	-	-	-	-	G32[0]	-	-
gmac	699	aclk_gmac_noc	32	-	-	-	-	-	-	-	-	G32[1]	-	-
gmac	700	pclk_gmac	33	-	-	-	-	-	-	-	-	G32[2]	-	-
gmac	701	pclk_gmac_noc	33	-	-	-	-	-	-	-	-	G32[3]	-	-
gmac	702	aclk_perf_gmac	32	-	-	-	-	-	-	-	-	G32[4]	-	-
-	-	-		-	-	-	-	-	-	-	-	-	-	-
emmc	704	aclk_emmc_core	147	-	-	-	-	-	-	-	-	G32[8]	-	-
emmc	705	aclk_emmc_noc	147	-	-	-	-	-	-	-	-	G32[9]	-	-
emmc	706	aclk_emmc_grf	147	-	-	-	-	-	-	-	-	G32[10]	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
edp	708	pclk_edp_noc	197	-	-	-	-	-	-	-	-	G32[12]	-	-
edp	709	pclk_edp_ctrl	197	-	-	-	-	-	-	-	-	G32[13]	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
gic	711	aclk_gic	228	-	-	-	-	-	-	-	-	G33[0]	-	-
gic	712	aclk_gic_noc	228	-	-	-	-	-	-	-	-	G33[1]	-	-
gic	713	aclk_gic_adb400_core_l_2_gic	228	-	-	-	-	-	-	-	-	G33[2]	-	-
gic	714	aclk_gic_adb400_core_b_2_gic	228	-	-	-	-	-	-	-	-	G33[3]	-	-
gic	715	aclk_gic_adb400_gic_2_core_l	228	-	-	-	-	-	-	-	-	G33[4]	-	-
gic	716	aclk_gic_adb400_gic_2_core_b	228	-	-	-	-	-	-	-	-	G33[5]	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
sd	718	hclk_sdmmc	325	-	-	-	-	-	-	-	-	G33[8]	-	-
sd	719	hclk_sdmmc_noc	325	-	-	-	-	-	-	-	-	G33[9]	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
perilp1	721	hclk_i2s0	162	-	-	-	-	-	-	-	-	G34[0]	-	-
perilp1	722	hclk_i2s1	162	-	-	-	-	-	-	-	-	G34[1]	-	-
perilp1	723	hclk_i2s2	162	-	-	-	-	-	-	-	-	G34[2]	-	-
perilp1	724	hclk_spdif	162	-	-	-	-	-	-	-	-	G34[3]	-	-
perilp1	725	hclk_sdio	162	-	-	-	-	-	-	-	-	G34[4]	-	-
perilp1	726	pclk_spi5	162	-	-	-	-	-	-	-	-	G34[5]	-	-
perilp1	727	hclk_sdioaudio_noc	162	-	-	-	-	-	-	-	-	G34[6]	-	-

Note:

*S**	*CRU_CLKSEL_CON**
*G**	*CRU_GATE_CON**
*M**	*CRU_MISC_CON*
GRF5[3]	*rmii_clk_sel*
GRF5[5:4]	*gmac_clk_sel[1:0]*
GRF5[6]	*rmii_mode*
*GF_**	*glitch-free*
*ICG_**	*ICG DIV*

*F** *Fixed_div=**

Fig. 3-4 RK3399 Clock Architecture Diagram-ipgating

3.4 System Reset Solution

The following diagram shows reset architecture.

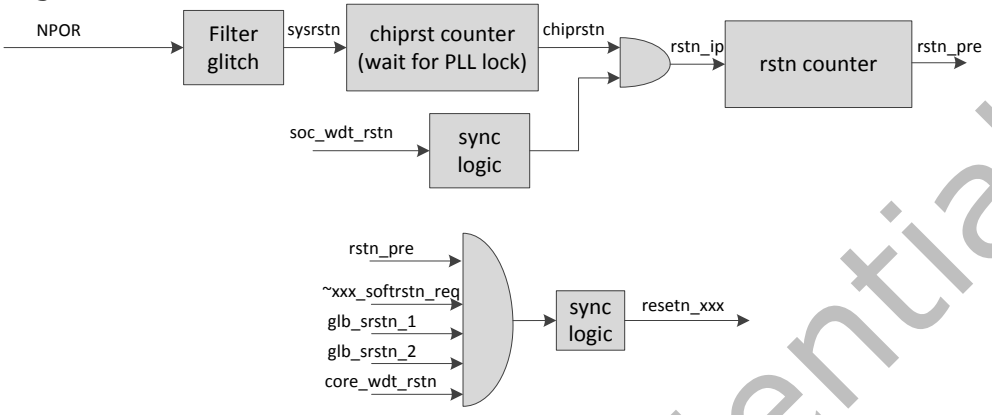


Fig. 3-5 Reset Architecture Diagram

Reset source of each reset signal includes hardware reset(NPOR), soc watch dog reset(soc_wdt_rstn), software reset request(xxx_softrstn_req), global software reset1(glb_srstn_1), global software reset2(glb_srstn_2) and A9 core watch dog reset(core_wdt_rstn).

The 'xxx' of resetn_xxx and xxx_softrstn_req is the module name.

soc_wdt_rstn is the reset from watch-dog IP in the SoC, but core_wdt_rstn is the reset from A7 core watch-dog block.

glb_srstn_1 and glb_srstn_2 are the global software reset by programming CRU register. When writing register CRU_GLB_SRST_FST_VALUE as 0xfdb9, glb_srstn_1 will be asserted, and when writing register

CRU_GLB_SRST_SND_VALUE as 0xeca8, glb_srstn_2 will be asserted. The two software reset will be self-clear by hardware. glb_srstn_1 will reset the all logic, and glb_srstn_2 will reset the all logic except GRF and all GPIOs.

3.5 Function Description

There are three PLLs in the chip: ARM PLL, DDR PLL and GENERAL PLL, and it supports only onecrystal oscillator: 24MHz. Each PLL can only receive 24MHz oscillator.

Three PLLs all can be set to slow mode or deep slow mode, directly output selectable 24MHz. When power on or changing PLL setting, we must force PLL into slow mode to ensure output stable clock.

To maximize the flexibility, some of clocks can select divider source from three three PLLs.

To provide some specific frequency, another solution is integrated: fractional divider. In order to be sure the performance for divided clock, there is some usage limit, we can only get low frequency and divider factor must be larger than 20.

All clocks can be software gated and all reset can be software generated.

3.6 PLL Introduction

3.6.1 Overview

The chip uses 2.4GHz PLL for all three PLLs.The 2.4GHz PLL is a general purpose, high-performance PLL-based clock generator. ThePLL is a multi-function, general purposefrequency synthesizer. Ultra-wide input and output ranges along with best-in-class jitter performanceallow the PLL to be used for almost any clocking application. With excellent supply noise immunity,the PLL is ideal for use in noisy mixed signal SoC environments. By combining ultra-low jitter outputclocks into a low power, low area, widely programmable design, Silicon Creations can greatly simplifyan SoC by enabling a single macro to be used for

all clocking applications in the system.
2.4GHz PLL supports the following features:

- Input frequency range:1MHz to 800MHz(Integer Mode) and10MHz to 800MHz (Fractional Mode)
- Output Frequency Range: 16MHz to 3.2GHz
- 24 bit fractional accuracy, and fractional mode jitter performance to nearly match integer mode performance.
- 4:1 VCO frequency range allows PLL to be optimized for minimum jitter or minimum power.
- Isolated analog supply (2.5V) allows for excellent supply rejection in noisy SoC applications.
- Lock Detect Signal indicates when frequency lock has been achieved.

3.6.2 Block diagram

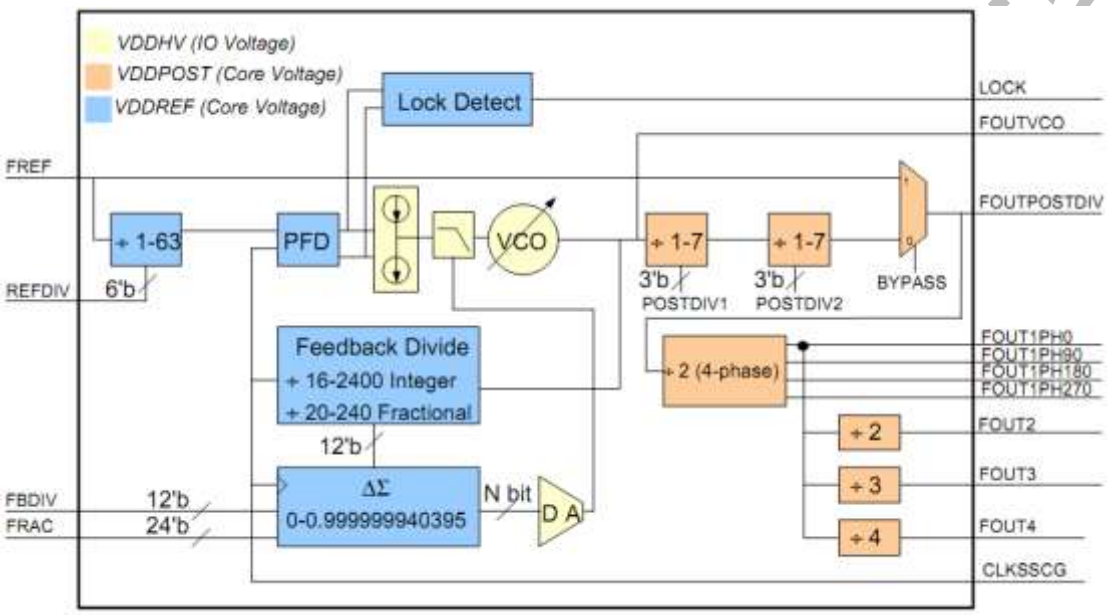


Fig. 3-6 PLL Block Diagram

How to calculate the PLL

The Fractional PLL output frequency can be calculated using some simple formulas. These formulas also embedded within the Fractional PLL Verilog model:
If DSMPD = 1 (DSM is disabled, "integer mode")
FOUTVCO = FREF / REFDIV * FBDIV
FOUTPOSTDIV = FOUTVCO / POSTDIV1 / POSTDIV2
If DSMPD = 0 (DSM is enabled, "fractional mode")
FOUTVCO = FREF / REFDIV * (FBDIV + FRAC / 224)
FOUTPOSTDIV = FOUTVCO / POSTDIV1 / POSTDIV2
Where:
FOUTVCO = Fractional PLL non-divided output frequency
FOUTPOSTDIV = Fractional PLL divided output frequency (output of second post divider)
FREF = Fractional PLL input reference frequency
REFDIV = Fractional PLL input reference clock divider
FVCO = Frequency of internal VCO
FBDIV = Integer value programmed into feedback divide
FRAC = Fractional value programmed into DSM

Changing the PLL Programming

In most cases the PLL programming can be changed on-the-fly and the PLL will simply slew to the new frequency. However, certain changes have the potential to cause glitches on the PLL output clocks. These changes include:

- Switching into or out of BYPASS mode may cause a glitch on FOUTPOSTDIV
- Changing POSTDIV1 or POSTDIV2 may cause a short pulse with width equal to as little as one VCO period on FOUTPOSTDIV
- Changing POSTDIV could cause a shortened pulse on FOUT1PH* or FOUT2/3/4

- Asserting PD or FOUTPOSTDIVPD may cause a glitch on FOUTPOSTDIV

3.7 Register Description

This section describes the control/status registers of the design.

3.7.1 Registers Summary-PMUCRU

Name	Offset	Size	Reset Value	Description
PMUCRU_PPLL_CON0	0x0000	W	0x000000a9	PPLL configuration register0
PMUCRU_PPLL_CON1	0x0004	W	0x00001203	PPLL configuration register1
PMUCRU_PPLL_CON2	0x0008	W	0x0000031f	PPLL configuration register2
PMUCRU_PPLL_CON3	0x000c	W	0x00000008	PPLL configuration register3
PMUCRU_PPLL_CON4	0x0010	W	0x00000007	PPLL configuration register4
PMUCRU_PPLL_CON5	0x0014	W	0x00007f00	PPLL configuration register5
PMUCRU_CLKSEL_CON0	0x0080	W	0x00000706	Internal clock select and divide register0
PMUCRU_CLKSEL_CON1	0x0084	W	0x00001986	Internal clock select and divide register1
PMUCRU_CLKSEL_CON2	0x0088	W	0x00000303	Internal clock select and divide register2
PMUCRU_CLKSEL_CON3	0x008c	W	0x00000003	Internal clock select and divide register3
PMUCRU_CLKSEL_CON4	0x0090	W	0x000002dc	Internal clock select and divide register4
PMUCRU_CLKSEL_CON5	0x0094	W	0x00000200	Internal clock select and divide register5
PMUCRU_CLKFRAC_CON0	0x0098	W	0x0bb8ea60	Internal clock select and divide register6
PMUCRU_CLKFRAC_CON1	0x009c	W	0x0bb8ea60	Internal clock select and divide register7
PMUCRU_CLKGATE_CON0	0x0100	W	0x00000000	Internal clock gating register0
PMUCRU_CLKGATE_CON1	0x0104	W	0x00000000	Internal clock gating register1
PMUCRU_CLKGATE_CON2	0x0108	W	0x00000000	Internal clock gating register2
PMUCRU_SOFTRST_CON0	0x0110	W	0x00000024	Internal software reset control register0
PMUCRU_SOFTRST_CON1	0x0114	W	0x00000000	Internal software reset control register1
PMUCRU_RSTNHOLD_CON0	0x0120	W	0x00000000	Internal reset hold control register0
PMUCRU_RSTNHOLD_CON1	0x0124	W	0x00000000	Internal reset hold control register1
PMUCRU_GATEDIS_CON0	0x0130	W	0x00000000	Internal gate disable control register0

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

3.7.2 Detail Register Description

PMUCRU_PPLL_CON0
Address: Operational Base + offset (0x0000)
PPLL configuration register0

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:12	RO	0x0	reserved
11:0	RW	0x0a9	fbdiv Feedback Divide Value Valid divider settings are: [16, 3200] in integer mode [20, 320] in fractional mode Tips: no plus one operation

PMUCRU_PPLL_CON1
Address: Operational Base + offset (0x0004)
PPLL configuration register1

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14:12	RW	0x1	postdiv2 Second Post Divide Value (1-7)
11	RO	0x0	reserved
10:8	RW	0x2	postdiv1 First Post Divide Value (1-7)
7:6	RO	0x0	reserved
5:0	RW	0x03	refdiv Reference Clock Divide Value (1-63)

PMUCRU_PPLL_CON2
Address: Operational Base + offset (0x0008)
PPLL configuration register2

Bit	Attr	Reset Value	Description
31	RO	0x0	pll_lock PLL lock status 1'b0: unlock 1'b1: lock

Bit	Attr	Reset Value	Description
30:24	RO	0x0	reserved
23:0	RW	0x00031f	fracdiv Fractional part of feedback divide (fraction = FRAC/2^24)

PMUCRU_PPLL_CON3
Address: Operational Base + offset (0x000c)
PPLL configuration register3

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:10	RO	0x0	reserved
9:8	RW	0x0	pll_work_mode PLL work mode select 2'b00: Slow mode, clock from external 24MHz/26MHz OSC (default) 2'b01: Normal mode, clock from PLL output 2'b10: Deep slow mode, clock from external 32.768kHz
7	RO	0x0	reserved
6	RW	0x0	fout4phasepd Power down 4-phase clocks and 2X, 3X, 4X clocks 1'b0: no power down 1'b1: power down
5	RW	0x0	foutvcopd Power down buffered VCO clock 1'b0: no power down 1'b1: power down
4	RW	0x0	foutpostdivpd Power down all outputs except for buffered VCO clock 1'b0: no power down 1'b1: power down
3	RW	0x1	dsmpd PLL saturation behavior enable 1'b0: no power down 1'b1: power down DSMPD = 1'b1 (modulator is disabled, "integer mode")
2	RW	0x0	dacpd Power down quantization noise cancellation DAC 1'b0: no power down 1'b1: power down

Bit	Attr	Reset Value	Description
1	RW	0x0	bypass PLL Bypass. FREF bypasses PLL to FOUTPOSTDIV 1'b0: no bypass 1'b1: bypass
0	RW	0x0	power_down Global power down 1'b0: no power down 1'b1: power down

PMUCRU_PPLL_CON4
Address: Operational Base + offset (0x0010)
PPLL configuration register4

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:13	RO	0x0	reserved
12:8	RW	0x00	ssmod_spread spread amplitude % = 0.1 * SPREAD[4:0]
7:4	RW	0x0	ssmod_divval Divider required to set the modulation frequency Divider required to set the modulation frequency
3	RW	0x0	ssmod_downspread Selects center spread or downs pread 1'b0: center spread 1'b1: down spread
2	RW	0x1	ssmod_reset Reset modulator state 1'b0: no reset 1'b1: reset
1	RW	0x1	ssmod_disable_sscg Bypass SSMOD by module 1'b0: no bypass 1'b1: bypass
0	RW	0x1	ssmod_bp Bypass SSMOD by integration 1'b0: no bypass 1'b1: bypass

PMUCRU_PPLL_CON5
Address: Operational Base + offset (0x0014)
PPLL configuration register5

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:8	RW	0x7f	ssmod_ext_maxaddr External wave table data inputs (0-255)
7:1	RO	0x0	reserved
0	RW	0x0	ssmod_sel_ext_wave select external wave 1'b0: no select ext_wave 1'b1: select ext_wave

PMUCRU_CLKSEL_CON0
Address: Operational Base + offset (0x0080)
Internal clock select and divide register0

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	cm0s_clk_pll_sel cm0s_clk divider control register 1'b0:PPLL 1'b1:xin_24m
14:13	RO	0x0	reserved
12:8	RW	0x07	cm0s_div_con cm0s clock source select control register clk=clk_src/(div_con+1)
7:5	RO	0x0	reserved
4:0	RW	0x06	pmu_pclk_div_con pmu_pclk divider control register clk=clk_src/(div_con+1)

PMUCRU_CLKSEL_CON1
Address: Operational Base + offset (0x0084)
Internal clock select and divide register1

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit

Bit	Attr	Reset Value	Description
15	RW	0x0	clk_timer_sel clk_timer source select control register 1'b0:xin_24m 1'b1:clk_32k
14	RW	0x0	clk_wifi_sel clk_wifi source select control register 1'b0:clk_wifi_divout 1'b1:clk_wifi_frac
13	RW	0x0	clk_wifi_pll_sel clk_wifi_pll source select control register 1'b0:PPLL 1'b1:xin_24m
12:8	RW	0x19	clk_wifi_div_con clk_wifi divider control register clk=clk_src/(div_con+1)
7	RW	0x1	clk_spi3_pll_sel clk_spi3_pll source select control register 1'b0:xin_24m 1'b1:PPLL
6:0	RW	0x06	clk_spi3_div_con clk_spi3 divider control register clk=clk_src/(div_con+1)

PMUCRU_CLKSEL_CON2
Address: Operational Base + offset (0x0088)
Internal clock select and divide register2

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14:8	RW	0x03	i2c8_div_con i2c8 divider control register clk=clk_src/(div_con+1)
7	RO	0x0	reserved
6:0	RW	0x03	i2c0_div_con i2c0 divider control register clk=clk_src/(div_con+1)

PMUCRU_CLKSEL_CON3
Address: Operational Base + offset (0x008c)
Internal clock select and divide register3

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:7	RO	0x0	reserved
6:0	RW	0x03	i2c4_div_con i2c4 divider control register clk=clk_src/(div_con+1)

PMUCRU_CLKSEL_CON4
Address: Operational Base + offset (0x0090)
Internal clock select and divide register4

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	clk_32k_suspend_sel clk_32k_suspend source select control register 1'b0:test clock out 1'b1:32k from pmu 24m div
14:10	RO	0x0	reserved
9:0	RW	0x2dc	clk_32k_suspend_div_con clk_32k_suspend divider control register clk=clk_src/(div_con+1)

PMUCRU_CLKSEL_CON5
Address: Operational Base + offset (0x0094)
Internal clock select and divide register5

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:11	RO	0x0	reserved
10	RW	0x0	clk_uart_pll_sel clk_uart_pll source select control register 1'b0:xin_24m 1'b1:PPLL
9:8	RW	0x2	uart4_clk_sel uart4_clk source select control register 2'b00:clk_uart4_divout 2'b01:clk_uart4_frac 2'b10:xin_24m
7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6:0	RW	0x00	uart4_div_con uart4 divider control register clk=clk_src/(div_con+1)

PMUCRU_CLKFRAC_CON0
Address: Operational Base + offset (0x0098)
Internal clock select and divide register6

Bit	Attr	Reset Value	Description
31:0	RW	0x0bb8ea60	uart4_frac_div_con uart4_frac divider control register Fout = Fsrc*numerator/denominator High 16-bit for numerator Low 16-bit for denominator

PMUCRU_CLKFRAC_CON1
Address: Operational Base + offset (0x009c)
Internal clock select and divide register7

Bit	Attr	Reset Value	Description
31:0	RW	0x0bb8ea60	wifi_frac_div_con wifi_frac divider control register Fout = Fsrc*numerator/denominator High 16-bit for numerator Low 16-bit for denominator

PMUCRU_CLKGATE_CON0
Address: Operational Base + offset (0x0100)
Internal clock gating register0

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:12	RO	0x0	reserved
11	RW	0x0	clk_i2c8_src_en clk_i2c8_src clock disable bit When HIGH, disable clock
10	RW	0x0	clk_i2c4_src_en clk_i2c4_src clock disable bit When HIGH, disable clock
9	RW	0x0	clk_i2c0_src_en clk_i2c0_src clock disable bit When HIGH, disable clock
8	RW	0x0	clk_wifi_en clk_wifi clock disable bit When HIGH, disable clock

Bit	Attr	Reset Value	Description
7	RW	0x0	clk_pvtm_pmu_en clk_pvtm_pmu clock disable bit When HIGH, disable clock
6	RW	0x0	clk_uart4_frac_src_en clk_uart4_frac_src clock disable bit When HIGH, disable clock
5	RW	0x0	clk_uart4_src_en clk_uart4_src clock disable bit When HIGH, disable clock
4	RW	0x0	clk_timer1_en clk_timer1 clock disable bit When HIGH, disable clock
3	RW	0x0	clk_timer0_en clk_timer0 clock disable bit When HIGH, disable clock
2	RW	0x0	clk_spi3_src_en clk_spi3_src clock disable bit When HIGH, disable clock
1	RW	0x0	fclk_cm0s_pmu_ppll_src_en fclk_cm0s_pmu_ppll_src clock disable bit When HIGH, disable clock
0	RO	0x0	reserved

PMUCRU_CLKGATE_CON1
Address: Operational Base + offset (0x0104)
Internal clock gating register1

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	pclk_wdt_m0_pmu_en pclk_wdt_m0_pmu clock disable bit When HIGH, disable clock
14	RW	0x0	pclk_uartm0_en pclk_uartm0 clock disable bit When HIGH, disable clock
13	RW	0x0	pclk_mailbox_pmu_en pclk_mailbox_pmu clock disable bit When HIGH, disable clock
12	RW	0x0	pclk_timer_pmu_en pclk_timer_pmu clock disable bit When HIGH, disable clock

Bit	Attr	Reset Value	Description
11	RW	0x0	pclk_spi3_en pclk_spi3 clock disable bit When HIGH, disable clock
10	RW	0x0	pclk_rkpwm_pmu_en pclk_rkpwm_pmu clock disable bit When HIGH, disable clock
9	RW	0x0	pclk_i2c8_en pclk_i2c8 clock disable bit When HIGH, disable clock
8	RW	0x0	pclk_i2c4_en pclk_i2c4 clock disable bit When HIGH, disable clock
7	RW	0x0	pclk_i2c0_en pclk_i2c0 clock disable bit When HIGH, disable clock
6	RW	0x0	pclk_noc_pmu_en pclk_noc_pmu clock disable bit When HIGH, disable clock Suggest always on
5	RW	0x0	pclk_sgrf_en pclk_sgrf clock disable bit When HIGH, disable clock Suggest always on
4	RW	0x0	pclk_gpio1_en pclk_gpio1 clock disable bit When HIGH, disable clock
3	RW	0x0	pclk_gpio0_en pclk_gpio0 clock disable bit When HIGH, disable clock
2	RW	0x0	pclk_intmem1_en pclk_intmem1 clock disable bit When HIGH, disable clock
1	RW	0x0	pclk_pmugrf_en pclk_pmugrf clock disable bit When HIGH, disable clock Suggest always on
0	RW	0x0	pclk_pmu_en pclk_pmu clock disable bit When HIGH, disable clock

PMUCRU_CLKGATE_CON2
Address: Operational Base + offset (0x0108)
Internal clock gating register2

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:6	RO	0x0	reserved
5	RW	0x0	hclk_noc_pmu_en hclk_noc_pmu clock disable bit When HIGH, disable clock Suggest always on
4	RO	0x0	reserved
3	RW	0x0	dclk_cm0s_en dclk_cm0s clock disable bit When HIGH, disable clock
2	RW	0x0	hclk_cm0s_en hclk_cm0s clock disable bit When HIGH, disable clock
1	RW	0x0	sclk_cm0s_en sclk_cm0s clock disable bit When HIGH, disable clock
0	RW	0x0	fclk_cm0s_en fclk_cm0s clock disable bit When HIGH, disable clock

PMUCRU_SOFTRST_CON0

Address: Operational Base + offset (0x0110)

Internal software reset control register0

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RO	0x0	reserved
13	RW	0x0	presetn_wdt_pmu_req presetn_wdt_pmu request bit When HIGH, reset relative logic
12	RW	0x0	resetn_uart_m0_pmu_req resetn_uart_m0_pmu request bit When HIGH, reset relative logic
11	RW	0x0	presetn_uart_m0_pmu_req presetn_uart_m0_pmu request bit When HIGH, reset relative logic
10	RW	0x0	resetn_timer_pmu_1_req resetn_timer_pmu_1 request bit When HIGH, reset relative logic

Bit	Attr	Reset Value	Description
9	RW	0x0	resetn_timer_pmu_0_req resetn_timer_pmu_0 request bit When HIGH, reset relative logic
8	RW	0x0	presetn_timer_pmu_0_1_req presetn_timer_pmu_0_1 request bit When HIGH, reset relative logic
7	RW	0x0	resetn_spi3_req resetn_spi3 request bit When HIGH, reset relative logic
6	RW	0x0	presetn_spi3_req presetn_spi3 request bit When HIGH, reset relative logic
5	RW	0x1	poresetn_cm0s_pmu_req poresetn_cm0s_pmu request bit When HIGH, reset relative logic
4	RW	0x0	dbgresetn_cm0s_pmu_req dbgresetn_cm0s_pmu request bit When HIGH, reset relative logic
3	RW	0x0	hresetn_cm0s_noc_pmu_req hresetn_cm0s_noc_pmu request bit When HIGH, reset relative logic
2	RW	0x1	hresetn_cm0s_pmu_req hresetn_cm0s_pmu request bit When HIGH, reset relative logic
1	RW	0x0	presetn_intmem_pmu_req presetn_intmem_pmu request bit When HIGH, reset relative logic
0	RW	0x0	presetn_noc_pmu_req presetn_noc_pmu request bit When HIGH, reset relative logic

PMUCRU_SOFTRST_CON1

Address: Operational Base + offset (0x0114)

Internal software reset control register1

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14	RW	0x0	resetn_i2c8_req resetn_i2c8 request bit When HIGH, reset relative logic

Bit	Attr	Reset Value	Description
13	RW	0x0	resetn_i2c4_req resetn_i2c4 request bit When HIGH, reset relative logic
12	RW	0x0	resetn_i2c0_req resetn_i2c0 request bit When HIGH, reset relative logic
11	RW	0x0	resetn_pvtm_pmu_req resetn_pvtm_pmu request bit When HIGH, reset relative logic
10	RW	0x0	presetn_intr_arb_req presetn_intr_arb request bit When HIGH, reset relative logic
9	RW	0x0	presetn_cru_pmu_req presetn_cru_pmu request bit When HIGH, reset relative logic
8	RW	0x0	presetn_gpio1_req presetn_gpio1 request bit When HIGH, reset relative logic
7	RW	0x0	presetn_gpio0_req presetn_gpio0 request bit When HIGH, reset relative logic
6	RW	0x0	presetn_sgrf_req presetn_sgrf request bit When HIGH, reset relative logic
5	RW	0x0	presetn_pmugrf_req presetn_pmugrf request bit When HIGH, reset relative logic
4	RW	0x0	presetn_rkpwm_pmu_req presetn_rkpwm_pmu request bit When HIGH, reset relative logic
3	RW	0x0	presetn_mailbox_pmu_req presetn_mailbox_pmu request bit When HIGH, reset relative logic
2	RW	0x0	presetn_i2c8_req presetn_i2c8 request bit When HIGH, reset relative logic
1	RW	0x0	presetn_i2c4_req presetn_i2c4 request bit When HIGH, reset relative logic
0	RW	0x0	presetn_i2c0_req presetn_i2c0 request bit When HIGH, reset relative logic

PMUCRU_RSTNHOLD_CON0
Address: Operational Base + offset (0x0120)

Internal reset hold control register0

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14	RW	0x0	presetn_wdt_pmu_hold presetn_wdt_pmu_hold control bit When HIGH, reset hold, can't be reset by any reset source
13	RW	0x0	resetn_uart_m0_pmu_hold resetn_uart_m0_pmu_hold control bit When HIGH, reset hold, can't be reset by any reset source
12	RW	0x0	presetn_uart_m0_pmu_hold presetn_uart_m0_pmu_hold control bit When HIGH, reset hold, can't be reset by any reset source
11	RW	0x0	resetn_timer_pmu_1_hold resetn_timer_pmu_1_hold control bit When HIGH, reset hold, can't be reset by any reset source
10	RW	0x0	resetn_timer_pmu_0_hold resetn_timer_pmu_0_hold control bit When HIGH, reset hold, can't be reset by any reset source
9	RW	0x0	presetn_timer_pmu_0_1_hold presetn_timer_pmu_0_1_hold control bit When HIGH, reset hold, can't be reset by any reset source
8	RW	0x0	resetn_spi3_hold resetn_spi3_hold control bit When HIGH, reset hold, can't be reset by any reset source
7	RW	0x0	presetn_spi3_hold presetn_spi3_hold control bit When HIGH, reset hold, can't be reset by any reset source
6	RW	0x0	poresetn_cm0s_pmu_hold poresetn_cm0s_pmu_hold control bit When HIGH, reset hold, can't be reset by any reset source
5	RW	0x0	dbgresetn_cm0s_pmu_hold dbgresetn_cm0s_pmu_hold control bit When HIGH, reset hold, can't be reset by any reset source
4	RW	0x0	hresetn_cm0s_noc_pmu_hold hresetn_cm0s_noc_pmu_hold control bit When HIGH, reset hold, can't be reset by any reset source
3	RW	0x0	hresetn_cm0s_pmu_hold hresetn_cm0s_pmu_hold control bit When HIGH, reset hold, can't be reset by any reset source
2	RW	0x0	presetn_intmem_pmu_hold presetn_intmem_pmu_hold control bit When HIGH, reset hold, can't be reset by any reset source

Bit	Attr	Reset Value	Description
1	RW	0x0	presetn_noc_pmu_hold presetn_noc_pmu_hold control bit When HIGH, reset hold, can't be reset by any reset source
0	RO	0x0	reserved

PMUCRU_RSTNHOLD_CON1
Address: Operational Base + offset (0x0124)
Internal reset hold control register1

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14	RW	0x0	resetn_i2c8_hold resetn_i2c8_hold control bit When HIGH, reset hold, can't be reset by any reset source
13	RW	0x0	resetn_i2c4_hold resetn_i2c4_hold control bit When HIGH, reset hold, can't be reset by any reset source
12	RW	0x0	resetn_i2c0_hold resetn_i2c0_hold control bit When HIGH, reset hold, can't be reset by any reset source
11	RW	0x0	resetn_pvtm_pmu_hold resetn_pvtm_pmu_hold control bit When HIGH, reset hold, can't be reset by any reset source
10	RW	0x0	presetn_intr_arb_hold presetn_intr_arb_hold control bit When HIGH, reset hold, can't be reset by any reset source
9	RW	0x0	presetn_cru_pmu_hold presetn_cru_pmu_hold control bit When HIGH, reset hold, can't be reset by any reset source
8	RW	0x0	presetn_gpio1_hold presetn_gpio1_hold control bit When HIGH, reset hold, can't be reset by any reset source
7	RW	0x0	presetn_gpio0_hold presetn_gpio0_hold control bit When HIGH, reset hold, can't be reset by any reset source
6	RW	0x0	presetn_sgrf_hold presetn_sgrf_hold control bit When HIGH, reset hold, can't be reset by any reset source
5	RW	0x0	presetn_pmugrf_hold presetn_pmugrf_hold control bit When HIGH, reset hold, can't be reset by any reset source

Bit	Attr	Reset Value	Description
4	RW	0x0	presetn_rkpwm_pmu_hold presetn_rkpwm_pmu_hold control bit When HIGH, reset hold, can't be reset by any reset source
3	RW	0x0	presetn_mailbox_pmu_hold presetn_mailbox_pmu_hold control bit When HIGH, reset hold, can't be reset by any reset source
2	RW	0x0	presetn_i2c8_hold presetn_i2c8_hold control bit When HIGH, reset hold, can't be reset by any reset source
1	RW	0x0	presetn_i2c4_hold presetn_i2c4_hold control bit When HIGH, reset hold, can't be reset by any reset source
0	RW	0x0	presetn_i2c0_hold presetn_i2c0_hold control bit When HIGH, reset hold, can't be reset by any reset source

PMUCRU_GATEDIS_CON0

Address: Operational Base + offset (0x0130)

Internal gate disable control register0

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	clk_sdioaudio_gating_dis clk_sdioaudio gate disable bit When HIGH, gate disable, open all clocks power domain idle request needed
28	RW	0x0	clk_sd_gating_dis clk_sd gate disable bit When HIGH, gate disable, open all clocks power domain idle request needed
27	RW	0x0	clk_gic_gating_dis clk_gic gate disable bit When HIGH, gate disable, open all clocks power domain idle request needed
26	RW	0x0	clk_gpu_gating_dis clk_gpu gate disable bit When HIGH, gate disable, open all clocks power domain idle request needed
25	RW	0x0	clk_perilp_gating_dis clk_perilp gate disable bit When HIGH, gate disable, open all clocks power domain idle request needed
24	RW	0x0	clk_perihp_gating_dis clk_perihp gate disable bit When HIGH, gate disable, open all clocks power domain idle request needed

Bit	Attr	Reset Value	Description
23	RW	0x0	clk_vcodec_gating_dis clk_vcodec gate disable bit When HIGH, gate disable, open all clocks power domain idle request needed
22	RW	0x0	clk_vdu_gating_dis clk_vdu gate disable bit When HIGH, gate disable, open all clocks power domain idle request needed
21	RW	0x0	clk_rga_gating_dis clk_rga gate disable bit When HIGH, gate disable, open all clocks power domain idle request needed
20	RW	0x0	clk_iep_gating_dis clk_iep gate disable bit When HIGH, gate disable, open all clocks power domain idle request needed
19	RW	0x0	clk_vopb_gating_dis clk_vopb gate disable bit When HIGH, gate disable, open all clocks power domain idle request needed
18	RW	0x0	clk_vopl_gating_dis clk_vopl gate disable bit When HIGH, gate disable, open all clocks power domain idle request needed
17	RW	0x0	clk_isp0_gating_dis clk_isp0 gate disable bit When HIGH, gate disable, open all clocks power domain idle request needed
16	RW	0x0	clk_isp1_gating_dis clk_isp1 gate disable bit When HIGH, gate disable, open all clocks power domain idle request needed
15	RW	0x0	clk_hdcp_gating_dis clk_hdcp gate disable bit When HIGH, gate disable, open all clocks power domain idle request needed
14	RW	0x0	clk_usb3_gating_dis clk_usb3 gate disable bit When HIGH, gate disable, open all clocks power domain idle request needed
13	RW	0x0	clk_perilpm0_gating_dis clk_perilpm0 gate disable bit When HIGH, gate disable, open all clocks power domain idle request needed

Bit	Attr	Reset Value	Description
12	RW	0x0	clk_center_gating_dis clk_center gate disable bit When HIGH, gate disable, open all clocks power domain idle request needed
11	RW	0x0	clk_ccim0_gating_dis clk_ccim0 gate disable bit When HIGH, gate disable, open all clocks power domain idle request needed
10	RW	0x0	clk_ccim1_gating_dis clk_ccim1 gate disable bit When HIGH, gate disable, open all clocks power domain idle request needed
9	RW	0x0	clk_vio_gating_dis clk_vio gate disable bit When HIGH, gate disable, open all clocks power domain idle request needed
8	RW	0x0	clk_msch0_gating_dis clk_msch0 gate disable bit When HIGH, gate disable, open all clocks power domain idle request needed
7	RW	0x0	clk_msch1_gating_dis clk_msch1 gate disable bit When HIGH, gate disable, open all clocks power domain idle request needed
6	RW	0x0	clk_alive_gating_dis clk_alive gate disable bit When HIGH, gate disable, open all clocks power domain idle request needed
5	RW	0x0	clk_pmu_gating_dis clk_pmu gate disable bit When HIGH, gate disable, open all clocks power domain idle request needed
4	RW	0x0	clk_edp_gating_dis clk_edp gate disable bit When HIGH, gate disable, open all clocks power domain idle request needed
3	RW	0x0	clk_gmac_gating_dis clk_gmac gate disable bit When HIGH, gate disable, open all clocks power domain idle request needed
2	RW	0x0	clk_emmc_gating_dis clk_emmc gate disable bit When HIGH, gate disable, open all clocks power domain idle request needed

Bit	Attr	Reset Value	Description
1	RW	0x0	clk_center1_gating_dis clk_center1 gate disable bit When HIGH, gate disable, open all clocks power domain idle request needed
0	RW	0x0	clk_pmum0_gating_dis clk_pmum0 gate disable bit When HIGH, gate disable, open all clocks power domain idle request needed

3.7.3 Registers Summary-CRU

Name	Offset	Size	Reset Value	Description
CRU_LPLL_CON0	0x0000	W	0x00000096	LPLL configuration register0
CRU_LPLL_CON1	0x0004	W	0x00001202	LPLL configuration register1
CRU_LPLL_CON2	0x0008	W	0x0000031f	LPLL configuration register2
CRU_LPLL_CON3	0x000c	W	0x00000008	LPLL configuration register3
CRU_LPLL_CON4	0x0010	W	0x00000007	LPLL configuration register4
CRU_LPLL_CON5	0x0014	W	0x00007f00	LPLL configuration register5
CRU_BPLL_CON0	0x0020	W	0x00000064	BPLL configuration register0
CRU_BPLL_CON1	0x0024	W	0x00001201	BPLL configuration register1
CRU_BPLL_CON2	0x0028	W	0x0000031f	BPLL configuration register2
CRU_BPLL_CON3	0x002c	W	0x00000008	BPLL configuration register3
CRU_BPLL_CON4	0x0030	W	0x00000007	BPLL configuration register4
CRU_BPLL_CON5	0x0034	W	0x00007f00	BPLL configuration register5
CRU_DPLL_CON0	0x0040	W	0x00000064	DPLL configuration register0
CRU_DPLL_CON1	0x0044	W	0x00001301	DPLL configuration register1
CRU_DPLL_CON2	0x0048	W	0x0000031f	DPLL configuration register2
CRU_DPLL_CON3	0x004c	W	0x00000008	DPLL configuration register3
CRU_DPLL_CON4	0x0050	W	0x00000007	DPLL configuration register4
CRU_DPLL_CON5	0x0054	W	0x00007f00	DPLL configuration register5
CRU_CPLL_CON0	0x0060	W	0x000000c0	CPLL configuration register0
CRU_CPLL_CON1	0x0064	W	0x00001302	CPLL configuration register1
CRU_CPLL_CON2	0x0068	W	0x0000031f	CPLL configuration register2
CRU_CPLL_CON3	0x006c	W	0x00000008	CPLL configuration register3
CRU_CPLL_CON4	0x0070	W	0x00000007	CPLL configuration register4
CRU_CPLL_CON5	0x0074	W	0x00007f00	CPLL configuration register5
CRU_GPLL_CON0	0x0080	W	0x000000c6	GPLL configuration register0
CRU_GPLL_CON1	0x0084	W	0x00002202	GPLL configuration register1
CRU_GPLL_CON2	0x0088	W	0x0000031f	GPLL configuration register2
CRU_GPLL_CON3	0x008c	W	0x00000008	GPLL configuration register3
CRU_GPLL_CON4	0x0090	W	0x00000007	GPLL configuration register4
CRU_GPLL_CON5	0x0094	W	0x00007f00	GPLL configuration register5
CRU_NPLL_CON0	0x00a0	W	0x000000fa	NPLL configuration register0

Name	Offset	Size	Reset Value	Description
CRU_NPLL_CON1	0x00a4	W	0x00001203	NPLL configuration register1
CRU_NPLL_CON2	0x00a8	W	0x0000031f	NPLL configuration register2
CRU_NPLL_CON3	0x00ac	W	0x00000008	NPLL configuration register3
CRU_NPLL_CON4	0x00b0	W	0x00000007	NPLL configuration register4
CRU_NPLL_CON5	0x00b4	W	0x00007f00	NPLL configuration register5
CRU_VPLL_CON0	0x00c0	W	0x000000c6	VPLL configuration register0
CRU_VPLL_CON1	0x00c4	W	0x00001202	VPLL configuration register1
CRU_VPLL_CON2	0x00c8	W	0x0000031f	VPLL configuration register2
CRU_VPLL_CON3	0x00cc	W	0x00000008	VPLL configuration register3
CRU_VPLL_CON4	0x00d0	W	0x00000007	VPLL configuration register4
CRU_VPLL_CON5	0x00d4	W	0x00007f00	VPLL configuration register5
CRU_CLKSEL_CON0	0x0100	W	0x00000101	Internal clock select and divide register0
CRU_CLKSEL_CON1	0x0104	W	0x00000303	Internal clock select and divide register1
CRU_CLKSEL_CON2	0x0108	W	0x00000141	Internal clock select and divide register2
CRU_CLKSEL_CON3	0x010c	W	0x00006303	Internal clock select and divide register3
CRU_CLKSEL_CON4	0x0110	W	0x00000041	Internal clock select and divide register4
CRU_CLKSEL_CON5	0x0114	W	0x00008341	Internal clock select and divide register5
CRU_CLKSEL_CON6	0x0118	W	0x00000320	Internal clock select and divide register6
CRU_CLKSEL_CON7	0x011c	W	0x00000101	Internal clock select and divide register7
CRU_CLKSEL_CON8	0x0120	W	0x00000101	Internal clock select and divide register8
CRU_CLKSEL_CON9	0x0124	W	0x00004141	Internal clock select and divide register9
CRU_CLKSEL_CON10	0x0128	W	0x00000101	Internal clock select and divide register10
CRU_CLKSEL_CON11	0x012c	W	0x00000101	Internal clock select and divide register11
CRU_CLKSEL_CON12	0x0130	W	0x00000100	Internal clock select and divide register12
CRU_CLKSEL_CON13	0x0134	W	0x00000361	Internal clock select and divide register13
CRU_CLKSEL_CON14	0x0138	W	0x00003181	Internal clock select and divide register14
CRU_CLKSEL_CON15	0x013c	W	0x00000500	Internal clock select and divide register15

Name	Offset	Size	Reset Value	Description
CRU_CLKSEL_CON16	0x0140	W	0x00000500	Internal clock select and divide register16
CRU_CLKSEL_CON17	0x0144	W	0x00000300	Internal clock select and divide register17
CRU_CLKSEL_CON18	0x0148	W	0x00004a87	Internal clock select and divide register18
CRU_CLKSEL_CON19	0x014c	W	0x00000100	Internal clock select and divide register19
CRU_CLKSEL_CON20	0x0150	W	0x00009303	Internal clock select and divide register20
CRU_CLKSEL_CON21	0x0154	W	0x00000003	Internal clock select and divide register21
CRU_CLKSEL_CON22	0x0158	W	0x00000400	Internal clock select and divide register22
CRU_CLKSEL_CON23	0x015c	W	0x00003181	Internal clock select and divide register23
CRU_CLKSEL_CON24	0x0160	W	0x00008103	Internal clock select and divide register24
CRU_CLKSEL_CON25	0x0164	W	0x00000183	Internal clock select and divide register25
CRU_CLKSEL_CON26	0x0168	W	0x00000103	Internal clock select and divide register26
CRU_CLKSEL_CON27	0x016c	W	0x000002dc	Internal clock select and divide register27
CRU_CLKSEL_CON28	0x0170	W	0x00000300	Internal clock select and divide register28
CRU_CLKSEL_CON29	0x0174	W	0x00000300	Internal clock select and divide register29
CRU_CLKSEL_CON30	0x0178	W	0x00000300	Internal clock select and divide register30
CRU_CLKSEL_CON31	0x017c	W	0x00000000	Internal clock select and divide register31
CRU_CLKSEL_CON32	0x0180	W	0x00006300	Internal clock select and divide register32
CRU_CLKSEL_CON33	0x0184	W	0x00000200	Internal clock select and divide register33
CRU_CLKSEL_CON34	0x0188	W	0x00000200	Internal clock select and divide register34
CRU_CLKSEL_CON35	0x018c	W	0x00000200	Internal clock select and divide register35
CRU_CLKSEL_CON36	0x0190	W	0x00000200	Internal clock select and divide register36
CRU_CLKSEL_CON38	0x0198	W	0x00003f3f	Internal clock select and divide register38

Name	Offset	Size	Reset Value	Description
CRU_CLKSEL_CON39	0x019c	W	0x00000041	Internal clock select and divide register39
CRU_CLKSEL_CON40	0x01a0	W	0x00000000	Internal clock select and divide register40
CRU_CLKSEL_CON41	0x01a4	W	0x00000000	Internal clock select and divide register41
CRU_CLKSEL_CON42	0x01a8	W	0x00000101	Internal clock select and divide register42
CRU_CLKSEL_CON43	0x01ac	W	0x00000421	Internal clock select and divide register43
CRU_CLKSEL_CON44	0x01b0	W	0x00000700	Internal clock select and divide register44
CRU_CLKSEL_CON45	0x01b4	W	0x000002dc	Internal clock select and divide register45
CRU_CLKSEL_CON46	0x01b8	W	0x00000004	Internal clock select and divide register46
CRU_CLKSEL_CON47	0x01bc	W	0x00000102	Internal clock select and divide register47
CRU_CLKSEL_CON48	0x01c0	W	0x00000102	Internal clock select and divide register48
CRU_CLKSEL_CON49	0x01c4	W	0x00000001	Internal clock select and divide register49
CRU_CLKSEL_CON50	0x01c8	W	0x00000003	Internal clock select and divide register50
CRU_CLKSEL_CON51	0x01cc	W	0x00000005	Internal clock select and divide register51
CRU_CLKSEL_CON52	0x01d0	W	0x00000005	Internal clock select and divide register52
CRU_CLKSEL_CON53	0x01d4	W	0x00000101	Internal clock select and divide register53
CRU_CLKSEL_CON54	0x01d8	W	0x00000101	Internal clock select and divide register54
CRU_CLKSEL_CON55	0x01dc	W	0x00008181	Internal clock select and divide register55
CRU_CLKSEL_CON56	0x01e0	W	0x00000320	Internal clock select and divide register56
CRU_CLKSEL_CON57	0x01e4	W	0x00000005	Internal clock select and divide register57
CRU_CLKSEL_CON58	0x01e8	W	0x0000071f	Internal clock select and divide register58
CRU_CLKSEL_CON59	0x01ec	W	0x00000707	Internal clock select and divide register59
CRU_CLKSEL_CON60	0x01f0	W	0x00000707	Internal clock select and divide register60

Name	Offset	Size	Reset Value	Description
CRU_CLKSEL_CON61	0x01f4	W	0x00000303	Internal clock select and divide register61
CRU_CLKSEL_CON62	0x01f8	W	0x00000303	Internal clock select and divide register62
CRU_CLKSEL_CON63	0x01fc	W	0x00000303	Internal clock select and divide register63
CRU_CLKSEL_CON64	0x0200	W	0x000000c5	Internal clock select and divide register64
CRU_CLKSEL_CON65	0x0204	W	0x000000c5	Internal clock select and divide register65
CRU_CLKSEL_CON96	0x0280	W	0x0bb8ea60	Internal clock select and divide register80
CRU_CLKSEL_CON97	0x0284	W	0x0bb8ea60	Internal clock select and divide register81
CRU_CLKSEL_CON98	0x0288	W	0x0bb8ea60	Internal clock select and divide register82
CRU_CLKSEL_CON99	0x028c	W	0x0bb8ea60	Internal clock select and divide register83
CRU_CLKSEL_CON100	0x0290	W	0x0bb8ea60	Internal clock select and divide register84
CRU_CLKSEL_CON101	0x0294	W	0x0bb8ea60	Internal clock select and divide register85
CRU_CLKSEL_CON102	0x0298	W	0x0bb8ea60	Internal clock select and divide register86
CRU_CLKSEL_CON103	0x029c	W	0x0bb8ea60	Internal clock select and divide register87
CRU_CLKSEL_CON105	0x02a4	W	0x0bb8ea60	Internal clock select and divide register89
CRU_CLKSEL_CON106	0x02a8	W	0x0bb8ea60	Internal clock select and divide register90
CRU_CLKSEL_CON107	0x02ac	W	0x0bb8ea60	Internal clock select and divide register91
CRU_CLKGATE_CON0	0x0300	W	0x00000000	Internal clock gating register0
CRU_CLKGATE_CON1	0x0304	W	0x00000000	Internal clock gating register1
CRU_CLKGATE_CON2	0x0308	W	0x00000000	Internal clock gating register2
CRU_CLKGATE_CON3	0x030c	W	0x00000000	Internal clock gating register3
CRU_CLKGATE_CON4	0x0310	W	0x00000000	Internal clock gating register4
CRU_CLKGATE_CON5	0x0314	W	0x00000000	Internal clock gating register5
CRU_CLKGATE_CON6	0x0318	W	0x00000000	Internal clock gating register6
CRU_CLKGATE_CON7	0x031c	W	0x00000000	Internal clock gating register7
CRU_CLKGATE_CON8	0x0320	W	0x00000000	Internal clock gating register8
CRU_CLKGATE_CON9	0x0324	W	0x00000000	Internal clock gating register9
CRU_CLKGATE_CON10	0x0328	W	0x00000000	Internal clock gating register10
CRU_CLKGATE_CON11	0x032c	W	0x00000000	Internal clock gating register11

Name	Offset	Size	Reset Value	Description
CRU_CLKGATE_CON12	0x0330	W	0x00000000	Internal clock gating register12
CRU_CLKGATE_CON13	0x0334	W	0x00000000	Internal clock gating register13
CRU_CLKGATE_CON14	0x0338	W	0x00000000	Internal clock gating register14
CRU_CLKGATE_CON15	0x033c	W	0x00000000	Internal clock gating register15
CRU_CLKGATE_CON16	0x0340	W	0x00000000	Internal clock gating register16
CRU_CLKGATE_CON17	0x0344	W	0x00000000	Internal clock gating register17
CRU_CLKGATE_CON18	0x0348	W	0x00000000	Internal clock gating register18
CRU_CLKGATE_CON19	0x034c	W	0x00000000	Internal clock gating register19
CRU_CLKGATE_CON20	0x0350	W	0x00000000	Internal clock gating register20
CRU_CLKGATE_CON21	0x0354	W	0x00000000	Internal clock gating register21
CRU_CLKGATE_CON22	0x0358	W	0x00000000	Internal clock gating register22
CRU_CLKGATE_CON23	0x035c	W	0x00000000	Internal clock gating register23
CRU_CLKGATE_CON24	0x0360	W	0x00000000	Internal clock gating register24
CRU_CLKGATE_CON25	0x0364	W	0x00000000	Internal clock gating register25
CRU_CLKGATE_CON26	0x0368	W	0x00000000	Internal clock gating register26
CRU_CLKGATE_CON27	0x036c	W	0x00000000	Internal clock gating register27
CRU_CLKGATE_CON28	0x0370	W	0x00000000	Internal clock gating register28
CRU_CLKGATE_CON29	0x0374	W	0x00000000	Internal clock gating register29
CRU_CLKGATE_CON30	0x0378	W	0x00000000	Internal clock gating register30
CRU_CLKGATE_CON31	0x037c	W	0x00000000	Internal clock gating register31
CRU_CLKGATE_CON32	0x0380	W	0x00000000	Internal clock gating register32
CRU_CLKGATE_CON33	0x0384	W	0x00000000	Internal clock gating register33
CRU_CLKGATE_CON34	0x0388	W	0x00000000	Internal clock gating register34
CRU_SOFTRST_CON0	0x0400	W	0x00000000	Internal software reset control register0
CRU_SOFTRST_CON1	0x0404	W	0x00000000	Internal software reset control register1
CRU_SOFTRST_CON2	0x0408	W	0x00000000	Internal software reset control register2
CRU_SOFTRST_CON3	0x040c	W	0x00000010	Internal software reset control register3
CRU_SOFTRST_CON4	0x0410	W	0x00000000	Internal software reset control register4
CRU_SOFTRST_CON5	0x0414	W	0x00000000	Internal software reset control register5
CRU_SOFTRST_CON6	0x0418	W	0x00000000	Internal software reset control register6
CRU_SOFTRST_CON7	0x041c	W	0x00000000	Internal software reset control register7
CRU_SOFTRST_CON8	0x0420	W	0x000000bc	Internal software reset control register8
CRU_SOFTRST_CON9	0x0424	W	0x00000000	Internal software reset control register9

Name	Offset	Size	Reset Value	Description
CRU_SOFTRST_CON10	0x0428	W	0x00000000	Internal software reset control register10
CRU_SOFTRST_CON11	0x042c	W	0x00000014	Internal software reset control register11
CRU_SOFTRST_CON12	0x0430	W	0x00000000	Internal software reset control register12
CRU_SOFTRST_CON13	0x0434	W	0x00000000	Internal software reset control register13
CRU_SOFTRST_CON14	0x0438	W	0x00000000	Internal software reset control register14
CRU_SOFTRST_CON15	0x043c	W	0x00000000	Internal software reset control register15
CRU_SOFTRST_CON16	0x0440	W	0x00000000	Internal software reset control register16
CRU_SOFTRST_CON17	0x0444	W	0x00000000	Internal software reset control register17
CRU_SOFTRST_CON18	0x0448	W	0x00000000	Internal software reset control register18
CRU_SOFTRST_CON19	0x044c	W	0x00000000	Internal software reset control register19
CRU_SOFTRST_CON20	0x0450	W	0x00000000	Internal software reset control register20
CRU_GLB_SRST_FST_VALUE	0x0500	W	0x00000000	The first global software reset config value
CRU_GLB_SRST_SND_VALUE	0x0504	W	0x00000000	The second global software reset config value
CRU_GLB_CNT_TH	0x0508	W	0x00000000	Global soft reset counter threshold
CRU_MISC_CON	0x050c	W	0x00000000	Output clock selection for test
CRU_GLB_RST_CON	0x0510	W	0x00000000	Global reset trigger select
CRU_GLB_RST_ST	0x0514	W	0x00000000	Global reset status
CRU_SDMMC_CON0	0x0580	W	0x00000004	sdmmc control0
CRU_SDMMC_CON1	0x0584	W	0x00000000	sdmmc control1
CRU_SDIO0_CON0	0x0588	W	0x00000004	sdio0 control0
CRU_SDIO0_CON1	0x058c	W	0x00000000	sdio0 control1

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

3.7.4 Detail Register Description

CRU_LPLL_CON0

Address: Operational Base + offset (0x0000)

LPLL configuration register0

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit

Bit	Attr	Reset Value	Description
15:12	RO	0x0	reserved
11:0	RW	0x096	fbdiv Feedback Divide Value Valid divider settings are: [16, 3200] in integer mode [20, 320] in fractional mode Tips: no plus one operation

CRU_LPLL_CON1
Address: Operational Base + offset (0x0004)
LPLL configuration register1

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14:12	RW	0x1	postdiv2 Second Post Divide Value (1-7)
11	RO	0x0	reserved
10:8	RW	0x2	postdiv1 First Post Divide Value (1-7)
7:6	RO	0x0	reserved
5:0	RW	0x02	refdiv Reference Clock Divide Value (1-63)

CRU_LPLL_CON2
Address: Operational Base + offset (0x0008)
LPLL configuration register2

Bit	Attr	Reset Value	Description
31	RO	0x0	pll_lock PLL lock status 1'b0: unlock 1'b1: lock
30:24	RO	0x0	reserved
23:0	RW	0x00031f	fracdiv Fractional part of feedback divide (fraction = FRAC/2^24)

CRU_LPLL_CON3
Address: Operational Base + offset (0x000c)
LPLL configuration register3

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:10	RO	0x0	reserved
9:8	RW	0x0	pll_work_mode PLL work mode select 2'b00: Slow mode, clock from external 24MHz/26MHz OSC (default) 2'b01: Normal mode, clock from PLL output 2'b10: Deep slow mode, clock from external 32.768kHz
7	RO	0x0	reserved
6	RW	0x0	fout4phasepd Power down 4-phase clocks and 2X, 3X, 4X clocks 1'b0: no power down 1'b1: power down
5	RW	0x0	foutvcopd Power down buffered VCO clock 1'b0: no power down 1'b1: power down
4	RW	0x0	foutpostdivpd Power down all outputs except for buffered VCO clock 1'b0: no power down 1'b1: power down
3	RW	0x1	dsmpd PLL saturation behavior enable 1'b0: no power down 1'b1: power down DSMPD = 1'b1 (modulator is disabled, "integer mode")
2	RW	0x0	dacpd Power down quantization noise cancellation DAC 1'b0: no power down 1'b1: power down
1	RW	0x0	bypass PLL Bypass. FREF bypasses PLL to FOUTPOSTDIV 1'b0: no bypass 1'b1: bypass
0	RW	0x0	power_down Global power down 1'b0: no power down 1'b1: power down

CRU_LPLL_CON4
Address: Operational Base + offset (0x0010)
LPLL configuration register4

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:13	RO	0x0	reserved
12:8	RW	0x00	ssmod_spread spread amplitude % = 0.1 * SPREAD[4:0]
7:4	RW	0x0	ssmod_divval Divider required to set the modulation frequency Divider required to set the modulation frequency
3	RW	0x0	ssmod_downspread Selects center spread or downs pread 1'b0: center spread 1'b1: down spread
2	RW	0x1	ssmod_reset Reset modulator state 1'b0: no reset 1'b1: reset
1	RW	0x1	ssmod_disable_sscg Bypass SSMOD by module 1'b0: no bypass 1'b1: bypass
0	RW	0x1	ssmod_bp Bypass SSMOD by integration 1'b0: no bypass 1'b1: bypass

CRU_LPLL_CON5
Address: Operational Base + offset (0x0014)
LPLL configuration register5

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:8	RW	0x7f	ssmod_ext_maxaddr External wave table data inputs (0-255)
7:1	RO	0x0	reserved
0	RW	0x0	ssmod_sel_ext_wave select external wave 1'b0: no select ext_wave 1'b1: select ext_wave

CRU_BPLL_CON0
Address: Operational Base + offset (0x0020)
BPLL configuration register0

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:12	RO	0x0	reserved
11:0	RW	0x064	fbdiv Feedback Divide Value Valid divider settings are: [16, 3200] in integer mode [20, 320] in fractional mode Tips: no plus one operation

CRU_BPLL_CON1
Address: Operational Base + offset (0x0024)
BPLL configuration register1

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14:12	RW	0x1	postdiv2 Second Post Divide Value (1-7)
11	RO	0x0	reserved
10:8	RW	0x2	postdiv1 First Post Divide Value (1-7)
7:6	RO	0x0	reserved
5:0	RW	0x01	refdiv Reference Clock Divide Value (1-63)

CRU_BPLL_CON2
Address: Operational Base + offset (0x0028)
BPLL configuration register2

Bit	Attr	Reset Value	Description
31	RO	0x0	pll_lock PLL lock status 1'b0: unlock 1'b1: lock
30:24	RO	0x0	reserved

Bit	Attr	Reset Value	Description
23:0	RW	0x00031f	fracdiv Fractional part of feedback divide (fraction = FRAC/2^24)

CRU_BPLL_CON3
Address: Operational Base + offset (0x002c)
BPLL configuration register3

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:10	RO	0x0	reserved
9:8	RW	0x0	pll_work_mode PLL work mode select 2'b00: Slow mode, clock from external 24MHz/26MHz OSC (default) 2'b01: Normal mode, clock from PLL output 2'b10: Deep slow mode, clock from external 32.768kHz
7	RO	0x0	reserved
6	RW	0x0	fout4phasepd Power down 4-phase clocks and 2X, 3X, 4X clocks 1'b0: no power down 1'b1: power down
5	RW	0x0	foutvcopd Power down buffered VCO clock 1'b0: no power down 1'b1: power down
4	RW	0x0	foutpostdivpd Power down all outputs except for buffered VCO clock 1'b0: no power down 1'b1: power down
3	RW	0x1	dsmpd PLL saturation behavior enable 1'b0: no power down 1'b1: power down DSMPD = 1'b1 (modulator is disabled, "integer mode")
2	RW	0x0	dacpd Power down quantization noise cancellation DAC 1'b0: no power down 1'b1: power down
1	RW	0x0	bypass PLL Bypass. FREF bypasses PLL to FOUTPOSTDIV 1'b0: no bypass 1'b1: bypass

Bit	Attr	Reset Value	Description
0	RW	0x0	power_down Global power down 1'b0: no power down 1'b1: power down

CRU_BPLL_CON4
Address: Operational Base + offset (0x0030)
BPLL configuration register4

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:13	RO	0x0	reserved
12:8	RW	0x00	ssmod_spread spread amplitude % = 0.1 * SPREAD[4:0]
7:4	RW	0x0	ssmod_divval Divider required to set the modulation frequency Divider required to set the modulation frequency
3	RW	0x0	ssmod_downspread Selects center spread or downs pread 1'b0: center spread 1'b1: down spread
2	RW	0x1	ssmod_reset Reset modulator state 1'b0: no reset 1'b1: reset
1	RW	0x1	ssmod_disable_sscg Bypass SSMOD by module 1'b0: no bypass 1'b1: bypass
0	RW	0x1	ssmod_bp Bypass SSMOD by integration 1'b0: no bypass 1'b1: bypass

CRU_BPLL_CON5
Address: Operational Base + offset (0x0034)
BPLL configuration register5

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit

Bit	Attr	Reset Value	Description
15:8	RW	0x7f	ssmod_ext_maxaddr External wave table data inputs (0-255)
7:1	RO	0x0	reserved
0	RW	0x0	ssmod_sel_ext_wave select external wave 1'b0: no select ext_wave 1'b1: select ext_wave

CRU_DPLL_CON0
Address: Operational Base + offset (0x0040)
DPLL configuration register0

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:12	RO	0x0	reserved
11:0	RW	0x064	fbdiv Feedback Divide Value Valid divider settings are: [16, 3200] in integer mode [20, 320] in fractional mode Tips: no plus one operation

CRU_DPLL_CON1
Address: Operational Base + offset (0x0044)
DPLL configuration register1

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14:12	RW	0x1	postdiv2 Second Post Divide Value (1-7)
11	RO	0x0	reserved
10:8	RW	0x3	postdiv1 First Post Divide Value (1-7)
7:6	RO	0x0	reserved
5:0	RW	0x01	refdiv Reference Clock Divide Value (1-63)

CRU_DPLL_CON2
Address: Operational Base + offset (0x0048)
DPLL configuration register2

Bit	Attr	Reset Value	Description
31	RO	0x0	pll_lock PLL lock status 1'b0: unlock 1'b1: lock
30:24	RO	0x0	reserved
23:0	RW	0x00031f	fracdiv Fractional part of feedback divide (fraction = FRAC/2^24)

CRU_DPLL_CON3
Address: Operational Base + offset (0x004c)
DPLL configuration register3

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:10	RO	0x0	reserved
9:8	RW	0x0	pll_work_mode PLL work mode select 2'b00: Slow mode, clock from external 24MHz/26MHz OSC (default) 2'b01: Normal mode, clock from PLL output 2'b10: Deep slow mode, clock from external 32.768kHz
7	RO	0x0	reserved
6	RW	0x0	fout4phasepd Power down 4-phase clocks and 2X, 3X, 4X clocks 1'b0: no power down 1'b1: power down
5	RW	0x0	foutvcopd Power down buffered VCO clock 1'b0: no power down 1'b1: power down
4	RW	0x0	foutpostdivpd Power down all outputs except for buffered VCO clock 1'b0: no power down 1'b1: power down

Bit	Attr	Reset Value	Description
3	RW	0x1	dsmpd PLL saturation behavior enable 1'b0: no power down 1'b1: power down DSMPD = 1'b1 (modulator is disabled, "integer mode")
2	RW	0x0	dacpd Power down quantization noise cancellation DAC 1'b0: no power down 1'b1: power down
1	RW	0x0	bypass PLL Bypass. FREF bypasses PLL to FOUTPOSTDIV 1'b0: no bypass 1'b1: bypass
0	RW	0x0	power_down Global power down 1'b0: no power down 1'b1: power down

CRU_DPLL_CON4
Address: Operational Base + offset (0x0050)
DPLL configuration register4

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:13	RO	0x0	reserved
12:8	RW	0x00	ssmod_spread spread amplitude % = 0.1 * SPREAD[4:0]
7:4	RW	0x0	ssmod_divval Divider required to set the modulation frequency Divider required to set the modulation frequency
3	RW	0x0	ssmod_downspread Selects center spread or downs pread 1'b0: center spread 1'b1: down spread
2	RW	0x1	ssmod_reset Reset modulator state 1'b0: no reset 1'b1: reset
1	RW	0x1	ssmod_disable_sscg Bypass SSMOD by module 1'b0: no bypass 1'b1: bypass

Bit	Attr	Reset Value	Description
0	RW	0x1	ssmod_bp Bypass SSMOD by integration 1'b0: no bypass 1'b1: bypass

CRU_DPLL_CON5
Address: Operational Base + offset (0x0054)
DPLL configuration register5

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:8	RW	0x7f	ssmod_ext_maxaddr External wave table data inputs (0-255)
7:1	RO	0x0	reserved
0	RW	0x0	ssmod_sel_ext_wave select external wave 1'b0: no select ext_wave 1'b1: select ext_wave

CRU_CPLL_CON0
Address: Operational Base + offset (0x0060)
CPLL configuration register0

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:12	RO	0x0	reserved
11:0	RW	0x0c0	fbdiv Feedback Divide Value Valid divider settings are: [16, 3200] in integer mode [20, 320] in fractional mode Tips: no plus one operation

CRU_CPLL_CON1
Address: Operational Base + offset (0x0064)
CPLL configuration register1

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14:12	RW	0x1	postdiv2 Second Post Divide Value (1-7)
11	RO	0x0	reserved
10:8	RW	0x3	postdiv1 First Post Divide Value (1-7)
7:6	RO	0x0	reserved
5:0	RW	0x02	refdiv Reference Clock Divide Value (1-63)

CRU_CPLL_CON2
Address: Operational Base + offset (0x0068)
CPLL configuration register2

Bit	Attr	Reset Value	Description
31	RO	0x0	pll_lock PLL lock status 1'b0: unlock 1'b1: lock
30:24	RO	0x0	reserved
23:0	RW	0x00031f	fracdiv Fractional part of feedback divide (fraction = FRAC/2^24)

CRU_CPLL_CON3
Address: Operational Base + offset (0x006c)
CPLL configuration register3

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:10	RO	0x0	reserved
9:8	RW	0x0	pll_work_mode PLL work mode select 2'b00: Slow mode, clock from external 24MHz/26MHz OSC (default) 2'b01: Normal mode, clock from PLL output 2'b10: Deep slow mode, clock from external 32.768kHz

Bit	Attr	Reset Value	Description
7	RO	0x0	reserved
6	RW	0x0	fout4phasepd Power down 4-phase clocks and 2X, 3X, 4X clocks 1'b0: no power down 1'b1: power down
5	RW	0x0	foutvcopd Power down buffered VCO clock 1'b0: no power down 1'b1: power down
4	RW	0x0	foutpostdivpd Power down all outputs except for buffered VCO clock 1'b0: no power down 1'b1: power down
3	RW	0x1	dsmpd PLL saturation behavior enable 1'b0: no power down 1'b1: power down DSMPD = 1'b1 (modulator is disabled, "integer mode")
2	RW	0x0	dacpd Power down quantization noise cancellation DAC 1'b0: no power down 1'b1: power down
1	RW	0x0	bypass PLL Bypass. FREF bypasses PLL to FOUTPOSTDIV 1'b0: no bypass 1'b1: bypass
0	RW	0x0	power_down Global power down 1'b0: no power down 1'b1: power down

CRU_CPLL_CON4
Address: Operational Base + offset (0x0070)
CPLL configuration register4

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:13	RO	0x0	reserved
12:8	RW	0x00	ssmod_spread spread amplitude % = 0.1 * SPREAD[4:0]

Bit	Attr	Reset Value	Description
7:4	RW	0x0	ssmod_divval Divider required to set the modulation frequency Divider required to set the modulation frequency
3	RW	0x0	ssmod_downspread Selects center spread or downs pread 1'b0: center spread 1'b1: down spread
2	RW	0x1	ssmod_reset Reset modulator state 1'b0: no reset 1'b1: reset
1	RW	0x1	ssmod_disable_sscg Bypass SSMOD by module 1'b0: no bypass 1'b1: bypass
0	RW	0x1	ssmod_bp Bypass SSMOD by integration 1'b0: no bypass 1'b1: bypass

CRU_CPLL_CON5
Address: Operational Base + offset (0x0074)
CPLL configuration register5

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:8	RW	0x7f	ssmod_ext_maxaddr External wave table data inputs (0-255)
7:1	RO	0x0	reserved
0	RW	0x0	ssmod_sel_ext_wave select external wave 1'b0: no select ext_wave 1'b1: select ext_wave

CRU_GPLL_CON0
Address: Operational Base + offset (0x0080)
GPLL configuration register0

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit

Bit	Attr	Reset Value	Description
15:12	RO	0x0	reserved
11:0	RW	0x0c6	fbdiv Feedback Divide Value Valid divider settings are: [16, 3200] in integer mode [20, 320] in fractional mode Tips: no plus one operation

CRU_GPLL_CON1
Address: Operational Base + offset (0x0084)
GPLL configuration register1

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14:12	RW	0x2	postdiv2 Second Post Divide Value (1-7)
11	RO	0x0	reserved
10:8	RW	0x2	postdiv1 First Post Divide Value (1-7)
7:6	RO	0x0	reserved
5:0	RW	0x02	refdiv Reference Clock Divide Value (1-63)

CRU_GPLL_CON2
Address: Operational Base + offset (0x0088)
GPLL configuration register2

Bit	Attr	Reset Value	Description
31	RO	0x0	pll_lock PLL lock status 1'b0: unlock 1'b1: lock
30:24	RO	0x0	reserved
23:0	RW	0x00031f	fracdiv Fractional part of feedback divide (fraction = FRAC/2^24)

CRU_GPLL_CON3
Address: Operational Base + offset (0x008c)
GPLL configuration register3

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:10	RO	0x0	reserved
9:8	RW	0x0	pll_work_mode PLL work mode select 2'b00: Slow mode, clock from external 24MHz/26MHz OSC (default) 2'b01: Normal mode, clock from PLL output 2'b10: Deep slow mode, clock from external 32.768kHz
7	RO	0x0	reserved
6	RW	0x0	fout4phasepd Power down 4-phase clocks and 2X, 3X, 4X clocks 1'b0: no power down 1'b1: power down
5	RW	0x0	foutvcopd Power down buffered VCO clock 1'b0: no power down 1'b1: power down
4	RW	0x0	foutpostdivpd Power down all outputs except for buffered VCO clock 1'b0: no power down 1'b1: power down
3	RW	0x1	dsmpd PLL saturation behavior enable 1'b0: no power down 1'b1: power down DSMPD = 1'b1 (modulator is disabled, "integer mode")
2	RW	0x0	dacpd Power down quantization noise cancellation DAC 1'b0: no power down 1'b1: power down
1	RW	0x0	bypass PLL Bypass. FREF bypasses PLL to FOUTPOSTDIV 1'b0: no bypass 1'b1: bypass
0	RW	0x0	power_down Global power down 1'b0: no power down 1'b1: power down

CRU_GPLL_CON4
Address: Operational Base + offset (0x0090)
GPLL configuration register4

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:13	RO	0x0	reserved
12:8	RW	0x00	ssmod_spread spread amplitude % = 0.1 * SPREAD[4:0]
7:4	RW	0x0	ssmod_divval Divider required to set the modulation frequency Divider required to set the modulation frequency
3	RW	0x0	ssmod_downspread Selects center spread or downs pread 1'b0: center spread 1'b1: down spread
2	RW	0x1	ssmod_reset Reset modulator state 1'b0: no reset 1'b1: reset
1	RW	0x1	ssmod_disable_sscg Bypass SSMOD by module 1'b0: no bypass 1'b1: bypass
0	RW	0x1	ssmod_bp Bypass SSMOD by integration 1'b0: no bypass 1'b1: bypass

CRU_GPLL_CON5
Address: Operational Base + offset (0x0094)
GPLL configuration register5

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:8	RW	0x7f	ssmod_ext_maxaddr External wave table data inputs (0-255)
7:1	RO	0x0	reserved
0	RW	0x0	ssmod_sel_ext_wave select external wave 1'b0: no select ext_wave 1'b1: select ext_wave

CRU_NPLL_CON0
Address: Operational Base + offset (0x00a0)
NPLL configuration register0

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:12	RO	0x0	reserved
11:0	RW	0x0fa	fbdiv Feedback Divide Value Valid divider settings are: [16, 3200] in integer mode [20, 320] in fractional mode Tips: no plus one operation

CRU_NPLL_CON1
Address: Operational Base + offset (0x00a4)
NPLL configuration register1

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14:12	RW	0x1	postdiv2 Second Post Divide Value (1-7)
11	RO	0x0	reserved
10:8	RW	0x2	postdiv1 First Post Divide Value (1-7)
7:6	RO	0x0	reserved
5:0	RW	0x03	refdiv Reference Clock Divide Value (1-63)

CRU_NPLL_CON2
Address: Operational Base + offset (0x00a8)
NPLL configuration register2

Bit	Attr	Reset Value	Description
31	RO	0x0	pll_lock PLL lock status 1'b0: unlock 1'b1: lock
30:24	RO	0x0	reserved

Bit	Attr	Reset Value	Description
23:0	RW	0x00031f	fracdiv Fractional part of feedback divide (fraction = FRAC/2^24)

CRU_NPLL_CON3
Address: Operational Base + offset (0x00ac)
NPLL configuration register3

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:10	RO	0x0	reserved
9:8	RW	0x0	pll_work_mode PLL work mode select 2'b00: Slow mode, clock from external 24MHz/26MHz OSC (default) 2'b01: Normal mode, clock from PLL output 2'b10: Deep slow mode, clock from external 32.768kHz
7	RO	0x0	reserved
6	RW	0x0	fout4phasepd Power down 4-phase clocks and 2X, 3X, 4X clocks 1'b0: no power down 1'b1: power down
5	RW	0x0	foutvcopd Power down buffered VCO clock 1'b0: no power down 1'b1: power down
4	RW	0x0	foutpostdivpd Power down all outputs except for buffered VCO clock 1'b0: no power down 1'b1: power down
3	RW	0x1	dsmpd PLL saturation behavior enable 1'b0: no power down 1'b1: power down DSMPD = 1'b1 (modulator is disabled, "integer mode")
2	RW	0x0	dacpd Power down quantization noise cancellation DAC 1'b0: no power down 1'b1: power down
1	RW	0x0	bypass PLL Bypass. FREF bypasses PLL to FOUTPOSTDIV 1'b0: no bypass 1'b1: bypass

Bit	Attr	Reset Value	Description
0	RW	0x0	power_down Global power down 1'b0: no power down 1'b1: power down

CRU_NPLL_CON4
Address: Operational Base + offset (0x00b0)
NPLL configuration register4

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:13	RO	0x0	reserved
12:8	RW	0x00	ssmod_spread spread amplitude % = 0.1 * SPREAD[4:0]
7:4	RW	0x0	ssmod_divval Divider required to set the modulation frequency Divider required to set the modulation frequency
3	RW	0x0	ssmod_downspread Selects center spread or downs pread 1'b0: center spread 1'b1: down spread
2	RW	0x1	ssmod_reset Reset modulator state 1'b0: no reset 1'b1: reset
1	RW	0x1	ssmod_disable_sscg Bypass SSMOD by module 1'b0: no bypass 1'b1: bypass
0	RW	0x1	ssmod_bp Bypass SSMOD by integration 1'b0: no bypass 1'b1: bypass

CRU_NPLL_CON5
Address: Operational Base + offset (0x00b4)
NPLL configuration register5

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit

Bit	Attr	Reset Value	Description
15:8	RW	0x7f	ssmod_ext_maxaddr External wave table data inputs (0-255)
7:1	RO	0x0	reserved
0	RW	0x0	ssmod_sel_ext_wave select external wave 1'b0: no select ext_wave 1'b1: select ext_wave

CRU_VPLL_CON0
Address: Operational Base + offset (0x00c0)
VPLL configuration register0

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:12	RO	0x0	reserved
11:0	RW	0x0c6	fbdiv Feedback Divide Value Valid divider settings are: [16, 3200] in integer mode [20, 320] in fractional mode Tips: no plus one operation

CRU_VPLL_CON1
Address: Operational Base + offset (0x00c4)
VPLL configuration register1

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14:12	RW	0x1	postdiv2 Second Post Divide Value (1-7)
11	RO	0x0	reserved
10:8	RW	0x2	postdiv1 First Post Divide Value (1-7)
7:6	RO	0x0	reserved
5:0	RW	0x02	refdiv Reference Clock Divide Value (1-63)

CRU_VPLL_CON2
Address: Operational Base + offset (0x00c8)
VPLL configuration register2

Bit	Attr	Reset Value	Description
31	RO	0x0	pll_lock PLL lock status 1'b0: unlock 1'b1: lock
30:24	RO	0x0	reserved
23:0	RW	0x00031f	fracdiv Fractional part of feedback divide (fraction = FRAC/2^24)

CRU_VPLL_CON3
Address: Operational Base + offset (0x00cc)
VPLL configuration register3

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:10	RO	0x0	reserved
9:8	RW	0x0	pll_work_mode PLL work mode select 2'b00: Slow mode, clock from external 24MHz/26MHz OSC (default) 2'b01: Normal mode, clock from PLL output 2'b10: Deep slow mode, clock from external 32.768kHz
7	RO	0x0	reserved
6	RW	0x0	fout4phasepd Power down 4-phase clocks and 2X, 3X, 4X clocks 1'b0: no power down 1'b1: power down
5	RW	0x0	foutvcopd Power down buffered VCO clock 1'b0: no power down 1'b1: power down
4	RW	0x0	foutpostdivpd Power down all outputs except for buffered VCO clock 1'b0: no power down 1'b1: power down

Bit	Attr	Reset Value	Description
3	RW	0x1	dsmpd PLL saturation behavior enable 1'b0: no power down 1'b1: power down DSMPD = 1'b1 (modulator is disabled, "integer mode")
2	RW	0x0	dacpd Power down quantization noise cancellation DAC 1'b0: no power down 1'b1: power down
1	RW	0x0	bypass PLL Bypass. FREF bypasses PLL to FOUTPOSTDIV 1'b0: no bypass 1'b1: bypass
0	RW	0x0	power_down Global power down 1'b0: no power down 1'b1: power down

CRU_VPLL_CON4
Address: Operational Base + offset (0x00d0)
VPLL configuration register4

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:13	RO	0x0	reserved
12:8	RW	0x00	ssmod_spread spread amplitude % = 0.1 * SPREAD[4:0]
7:4	RW	0x0	ssmod_divval Divider required to set the modulation frequency Divider required to set the modulation frequency
3	RW	0x0	ssmod_downspread Selects center spread or downs pread 1'b0: center spread 1'b1: down spread
2	RW	0x1	ssmod_reset Reset modulator state 1'b0: no reset 1'b1: reset
1	RW	0x1	ssmod_disable_sscg Bypass SSMOD by module 1'b0: no bypass 1'b1: bypass

Bit	Attr	Reset Value	Description
0	RW	0x1	ssmod_bp Bypass SSMOD by integration 1'b0: no bypass 1'b1: bypass

CRU_VPLL_CON5
Address: Operational Base + offset (0x00d4)
VPLL configuration register5

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:8	RW	0x7f	ssmod_ext_maxaddr External wave table data inputs (0-255)
7:1	RO	0x0	reserved
0	RW	0x0	ssmod_sel_ext_wave select external wave 1'b0: no select ext_wave 1'b1: select ext_wave

CRU_CLKSEL_CON0
Address: Operational Base + offset (0x0100)
Internal clock select and divide register0

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:13	RO	0x0	reserved
12:8	RW	0x01	aclkm_core_l_div_con aclkm_core_l divider control register clk=clk_src/(div_con+1)
7:6	RW	0x0	clk_core_l_pll_sel clk_core_l clock source select control register 2'b00:LPLL 2'b01:BPLL 2'b10:DPLL 2'b11:GPLL
5	RO	0x0	reserved
4:0	RW	0x01	clk_core_l_div_con clk_core_l divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON1
Address: Operational Base + offset (0x0104)
Internal clock select and divide register1

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:13	RO	0x0	reserved
12:8	RW	0x03	pclk_dbg_l_div_con pclk_dbg_l divider control register clk=clk_src/(div_con+1)
7:5	RO	0x0	reserved
4:0	RW	0x03	atclk_core_l_div_con atclk_core_l divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON2
Address: Operational Base + offset (0x0108)
Internal clock select and divide register2

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:13	RO	0x0	reserved
12:8	RW	0x01	aclkm_core_b_div_con aclkm_core_b divider control register clk=clk_src/(div_con+1)
7:6	RW	0x1	clk_core_b_pll_sel clk_core_b clock source select control register 2'b00:LPLL 2'b01:BPLL 2'b10:DPLL 2'b11:GPLL
5	RO	0x0	reserved
4:0	RW	0x01	clk_core_b_div_con clk_core_b divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON3
Address: Operational Base + offset (0x010c)
Internal clock select and divide register3

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14:13	RW	0x3	pclken_dbg_b_div_con pclken_dbg_b divider control register clk=clk_src/(div_con+1)
12:8	RW	0x03	pclk_dbg_b_div_con pclk_dbg_b divider control register clk=clk_src/(div_con+1)
7:5	RO	0x0	reserved
4:0	RW	0x03	atclk_core_b_div_con atclk_core_b divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON4
Address: Operational Base + offset (0x0110)
Internal clock select and divide register4

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:8	RO	0x0	reserved
7:6	RW	0x1	clk_cs_pll_sel clk_cs clock source select control register 2'b00:CPLL 2'b01:GPLL 2'b1x:NPLL
5	RO	0x0	reserved
4:0	RW	0x01	clk_cs_div_con clk_cs divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON5
Address: Operational Base + offset (0x0114)
Internal clock select and divide register5

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit

Bit	Attr	Reset Value	Description
15	RW	0x1	clk_cci_trace_pll_sel clk_cci_trace clock source select control register 1'b0:CPLL 1'b1:GPLL
14:13	RO	0x0	reserved
12:8	RW	0x03	clk_cci_trace_div_con clk_cci_trace divider control register clk=clk_src/(div_con+1)
7:6	RW	0x1	aclk_cci_pll_sel aclk_cci clock source select control register 2'b00:CPLL 2'b01:GPLL 2'b10:NPLL 2'b11:VPLL
5	RO	0x0	reserved
4:0	RW	0x01	aclk_cci_div_con aclk_cci divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON6
Address: Operational Base + offset (0x0118)
Internal clock select and divide register6

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	pclk_ddr_pll_sel pclk_ddr clock source select control register 1'b0:CPLL 1'b1:GPLL
14:13	RO	0x0	reserved
12:8	RW	0x03	pclk_ddr_div_con pclk_ddr divider control register clk=clk_src/(div_con+1)
7:6	RO	0x0	reserved
5:4	RW	0x2	clk_ddrc_pll_sel clk_ddrc clock source select control register 2'b00:LPLL 2'b01:BPLL 2'b10:DPLL 2'b11:GPLL
3	RO	0x0	reserved

Bit	Attr	Reset Value	Description
2:0	RW	0x0	clk_ddrc_div_con clk_ddrc divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON7
Address: Operational Base + offset (0x011c)
Internal clock select and divide register7

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:13	RO	0x0	reserved
12:8	RW	0x01	hclk_vcodec_div_con hclk_vcodec divider control register clk=clk_src/(div_con+1)
7:6	RW	0x0	aclk_vcodec_pll_sel aclk_vcodec clock source select control register 2'b00:CPLL 2'b01:GPLL 2'b10:NPLL 2'b11:PPLL
5	RO	0x0	reserved
4:0	RW	0x01	aclk_vcodec_div_con aclk_vcodec divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON8
Address: Operational Base + offset (0x0120)
Internal clock select and divide register8

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:13	RO	0x0	reserved
12:8	RW	0x01	hclk_vdu_div_con hclk_vdu divider control register clk=clk_src/(div_con+1)
7:6	RW	0x0	aclk_vdu_pll_sel aclk_vdu clock source select control register 2'b00:CPLL 2'b01:GPLL 2'b10:NPLL 2'b11:PPLL

Bit	Attr	Reset Value	Description
5	RO	0x0	reserved
4:0	RW	0x01	aclk_vdu_div_con aclk_vdu divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON9
Address: Operational Base + offset (0x0124)
Internal clock select and divide register9

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RW	0x1	clk_vdu_ca_pll_sel clk_vdu_ca clock source select control register 2'b00:CPLL 2'b01:GPLL 2'b1x:NPLL
13	RO	0x0	reserved
12:8	RW	0x01	clk_vdu_ca_div_con clk_vdu_ca divider control register clk=clk_src/(div_con+1)
7:6	RW	0x1	clk_vdu_core_pll_sel clk_vdu_core clock source select control register 2'b00:CPLL 2'b01:GPLL 2'b1x:NPLL
5	RO	0x0	reserved
4:0	RW	0x01	clk_vdu_core_div_con clk_vdu_core divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON10
Address: Operational Base + offset (0x0128)
Internal clock select and divide register10

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:13	RO	0x0	reserved
12:8	RW	0x01	hclk_iep_div_con hclk_iep divider control register clk=clk_src/(div_con+1)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	aclk_iep_pll_sel aclk_iep clock source select control register 2'b00:CPLL 2'b01:GPLL 2'b10:NPLL 2'b11:PPLL
5	RO	0x0	reserved
4:0	RW	0x01	aclk_iep_div_con aclk_iep divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON11
Address: Operational Base + offset (0x012c)
Internal clock select and divide register11

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:13	RO	0x0	reserved
12:8	RW	0x01	hclk_rga_div_con hclk_rga divider control register clk=clk_src/(div_con+1)
7:6	RW	0x0	aclk_rga_pll_sel aclk_rga clock source select control register 2'b00:CPLL 2'b01:GPLL 2'b10:NPLL 2'b11:PPLL
5	RO	0x0	reserved
4:0	RW	0x01	aclk_rga_div_con aclk_rga divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON12
Address: Operational Base + offset (0x0130)
Internal clock select and divide register12

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit

Bit	Attr	Reset Value	Description
15:14	RW	0x0	aclk_center_pll_sel aclk_center clock source select control register 2'b00:CPLL 2'b01:GPLL 2'b1x:NPLL
13	RO	0x0	reserved
12:8	RW	0x01	aclk_center_div_con aclk_center divider control register clk=clk_src/(div_con+1)
7:6	RW	0x0	clk_rga_core_pll_sel clk_rga_core clock source select control register 2'b00:CPLL 2'b01:GPLL 2'b10:NPLL 2'b11:PPLL
5	RO	0x0	reserved
4:0	RW	0x00	clk_rga_core_div_con clk_rga_core divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON13
Address: Operational Base + offset (0x0134)
Internal clock select and divide register13

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	hclk_sd_src_sel hclk_sd clock source select control register 1'b0:CPLL 1'b1:GPLL
14:13	RO	0x0	reserved
12:8	RW	0x03	hclk_sd_div_con hclk_sd divider control register clk=clk_src/(div_con+1)
7:5	RW	0x3	aclk_gpu_pll_sel aclk_gpu clock source select control register 3'b000:PPLL 3'b001:CPLL 3'b010:GPLL 3'b011:NPLL 3'b100:USB_480M

Bit	Attr	Reset Value	Description
4:0	RW	0x01	aclk_gpu_div_con aclk_gpu divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON14
Address: Operational Base + offset (0x0138)
Internal clock select and divide register14

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	clk_usbpll_480m_sel clk_usbpll_480m_sel clock select control register 1'b0:xin_24m 1'b1:clk_usbphy_480m
14:12	RW	0x3	pclk_perihp_div_con pclk_perihp divider control register clk=aclk_perihp/(div_con+1)
11:10	RO	0x0	reserved
9:8	RW	0x1	hclk_perihp_div_con hclk_perihp divider control register clk=aclk_perihp/(div_con+1)
7	RW	0x1	aclk_perihp_pll_sel aclk_perihp clock source select control register 1'b0:CPLL 1'b1:GPLL
6	RW	0x0	clk_usbphy_480m_ch_sel clk_usbphy_480m clock channel select control register 1'b0:usb_phy0_480m 1'b1:usb_phy1_480m
5	RO	0x0	reserved
4:0	RW	0x01	aclk_perihp_div_con aclk_perihp divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON15
Address: Operational Base + offset (0x013c)
Internal clock select and divide register15

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:11	RO	0x0	reserved

Bit	Attr	Reset Value	Description
10:8	RW	0x5	clk_sdio_pll_sel clk_sdio clock source select control register 3'b000:CPLL 3'b001:GPLL 3'b010:NPLL 3'b011:PPLL 3'b100:USB_480M 3'b101:xin_24m
7	RO	0x0	reserved
6:0	RW	0x00	clk_sdio_div_con clk_sdio divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON16
Address: Operational Base + offset (0x0140)
Internal clock select and divide register16

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:11	RO	0x0	reserved
10:8	RW	0x5	clk_sdmmc_pll_sel clk_sdmmc clock source select control register 3'b000:CPLL 3'b001:GPLL 3'b010:NPLL 3'b011:PPLL 3'b100:USB_480M 3'b101:xin_24m
7	RO	0x0	reserved
6:0	RW	0x00	clk_sdmmc_div_con clk_sdmmc divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON17
Address: Operational Base + offset (0x0144)
Internal clock select and divide register17

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:11	RO	0x0	reserved

Bit	Attr	Reset Value	Description
10:8	RW	0x3	clk_pcie_pm_pll_sel clk_pcie_pm clock source select control register 3'b000:CPLL 3'b001:GPLL 3'b010:NPLL 3'b011:xin_24m 3'b1xx:reserved
7	RO	0x0	reserved
6:0	RW	0x00	clk_pcie_pm_div_con clk_pcie_pm divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON18
Address: Operational Base + offset (0x0148)
Internal clock select and divide register18

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:11	RW	0x09	clk_pciephy_ref100m_div_con clk_pciephy_ref100m divider control register clk=clk_src/(div_con+1)
10	RW	0x0	clk_pciephy_ref_sel clk_pciephy_ref clock select control register 1'b0:clk_pcie_ref24m 1'b1:clk_pcie_ref100m
9:8	RW	0x2	clk_pcie_core_pll_sel clk_pcie_core clock source select control register 2'b00:CPLL 2'b01:GPLL 2'b1x:NPLL
7	RW	0x1	clk_pcie_core_clk_sel clk_pcie_core clock select control register 1'b0:clk_pcie_core 1'b1:pipe_clk_pcie from PCIE PHY
6:0	RW	0x07	clk_pcie_core_div_con clk_pcie_core divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON19
Address: Operational Base + offset (0x014c)
Internal clock select and divide register19

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:11	RO	0x0	reserved
10:8	RW	0x1	pclk_gmac_div_con pclk_gmac divider control register clk=clk_src/(div_con+1)
7:5	RO	0x0	reserved
4	RW	0x0	clk_rmii_src_sel clk_rmii_src clock select control register 1'b0:clk_mac_divout 1'b1:rmii_clkin from IO
3:2	RO	0x0	reserved
1:0	RW	0x0	clk_hsicphy_pll_sel clk_hsicphy clock source select control register 2'b00:CPLL 2'b01:GPLL 2'b10:NPLL 2'b11:USB_480M

CRU_CLKSEL_CON20
Address: Operational Base + offset (0x0150)
Internal clock select and divide register20

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RW	0x2	clk_gmac_pll_sel clk_gmac clock source select control register 2'b00:CPLL 2'b01:GPLL 2'b1x:NPLL
13	RO	0x0	reserved
12:8	RW	0x13	clk_gmac_div_con clk_gmac divider control register clk=clk_src/(div_con+1)
7	RW	0x0	aclk_gmac_pll_sel aclk_gmac clock source select control register 1'b0:CPLL 1'b1:GPLL
6:5	RO	0x0	reserved

Bit	Attr	Reset Value	Description
4:0	RW	0x03	aclk_gmac_div_con aclk_gmac divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON21
Address: Operational Base + offset (0x0154)
Internal clock select and divide register21

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:8	RO	0x0	reserved
7	RW	0x0	aclk_emmc_pll_sel aclk_emmc clock source select control register 1'b0:CPLL 1'b1:GPLL
6:5	RO	0x0	reserved
4:0	RW	0x03	aclk_emmc_div_con aclk_emmc divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON22
Address: Operational Base + offset (0x0158)
Internal clock select and divide register22

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:11	RO	0x0	reserved
10:8	RW	0x4	clk_emmc_pll_sel clk_emmc clock source select control register 3'b000:CPLL 3'b001:GPLL 3'b010:NPLL 3'b011:USB_480M 3'b1xx:xin_24m
7	RO	0x0	reserved
6:0	RW	0x00	clk_emmc_div_con clk_emmc divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON23
Address: Operational Base + offset (0x015c)

Internal clock select and divide register23

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14:12	RW	0x3	pclk_perilp0_div_con perilp0_pclk divider control register clk=aclk_perilp0/(div_con+1)
11:10	RO	0x0	reserved
9:8	RW	0x1	hclk_perilp0_div_con perilp0_hclk divider control register clk=aclk_perilp0/(div_con+1)
7	RW	0x1	aclk_perilp0_pll_sel aclk_perilp0 clock source select control register 1'b0:CPLL 1'b1:GPLL
6:5	RO	0x0	reserved
4:0	RW	0x01	aclk_perilp0_div_con aclk_perilp0 divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON24

Address: Operational Base + offset (0x0160)

Internal clock select and divide register24

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x1	fclk_cm0s_pll_sel fclk_cm0s clock source select control register 1'b0:CPLL 1'b1:GPLL
14:13	RO	0x0	reserved
12:8	RW	0x01	fclk_cm0s_div_con fclk_cm0s divider control register clk=clk_src/(div_con+1)
7:6	RW	0x0	clk_crypto0_pll_sel clk_crypto0 clock source select control register 2'b00:CPLL 2'b01:GPLL 2'b10:PPLL
5	RO	0x0	reserved

Bit	Attr	Reset Value	Description
4:0	RW	0x03	clk_crypto0_div_con clk_crypto0 divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON25
Address: Operational Base + offset (0x0164)
Internal clock select and divide register25

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:11	RO	0x0	reserved
10:8	RW	0x1	pclk_perilp1_div_con pclk_perilp1 divider control register clk=hclk_perilp1/(div_con+1)
7	RW	0x1	hclk_perilp1_pll_sel hclk_perilp1 clock source select control register 1'b0:CPLL 1'b1:GPLL
6:5	RO	0x0	reserved
4:0	RW	0x03	hclk_perilp1_div_con hclk_perilp1 divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON26
Address: Operational Base + offset (0x0168)
Internal clock select and divide register26

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:8	RW	0x01	clk_saradc_div_con clk_saradc divider control register clk=clk_src/(div_con+1)
7:6	RW	0x0	clk_crypto1_pll_sel clk_crypto1 clock source select control register 2'b00:CPLL 2'b01:GPLL 2'b10:PPLL
5	RO	0x0	reserved
4:0	RW	0x03	clk_crypto1_div_con clk_crypto1 divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON27
Address: Operational Base + offset (0x016c)
Internal clock select and divide register27

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	clk_tsadc_sel clk tsadc clock select control register 1'b0:xin_24m 1'b1:clk_32k
14:10	RO	0x0	reserved
9:0	RW	0x2dc	clk_tsadc_div_con clk tsadc divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON28
Address: Operational Base + offset (0x0170)
Internal clock select and divide register28

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:10	RO	0x0	reserved
9:8	RW	0x3	clk_i2s0_sel clk_i2s0 clock select control register 2'b00:clk_i2s0_divout 2'b01:clk_i2s0_frac 2'b10:clkin_i2s from IO 2'b11:clk_12m
7	RW	0x0	clk_i2s0_pll_sel clk_i2s0 clock source select control register 1'b0:CPLL 1'b1:GPLL
6:0	RW	0x00	clk_i2s0_div_con clk_i2s0 divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON29
Address: Operational Base + offset (0x0174)
Internal clock select and divide register29

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:10	RO	0x0	reserved
9:8	RW	0x3	clk_i2s1_sel clk_i2s1 clock select control register 2'b00:clk_i2s1_divout 2'b01:clk_i2s1_frac 2'b10:clkin_i2s from IO 2'b11:clk_12m
7	RW	0x0	clk_i2s1_pll_sel clk_i2s1 clock source select control register 1'b0:CPLL 1'b1:GPLL
6:0	RW	0x00	clk_i2s1_div_con clk_i2s1 divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON30
Address: Operational Base + offset (0x0178)
Internal clock select and divide register30

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:10	RO	0x0	reserved
9:8	RW	0x3	clk_i2s2_sel clk_i2s2 clock select control register 2'b00:clk_i2s2_divout 2'b01:clk_i2s2_frac 2'b10:clkin_i2s2 from IO 2'b11:clk_12m
7	RW	0x0	clk_i2s2_pll_sel clk_i2s2 clock source select control register 1'b0:CPLL 1'b1:GPLL
6:0	RW	0x00	clk_i2s2_div_con clk_i2s2 divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON31
Address: Operational Base + offset (0x017c)
Internal clock select and divide register31

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:3	RO	0x0	reserved
2	RW	0x0	clk_i2sout_sel clk_i2sout clock select control register 1'b0:clk_i2s 1'b1:clk_12m
1:0	RW	0x0	clk_i2s_ch_sel clk_i2s_ch clock select control register 2'b00:clk_i2s0 2'b01:clk_i2s1 2'b10:clk_i2s2

CRU_CLKSEL_CON32
Address: Operational Base + offset (0x0180)
Internal clock select and divide register32

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	clk_dptx_spdif_rec_pll_sel clk_dptx_spdif_rec clock source select control register 1'b0:CPLL 1'b1:GPLL
14:13	RW	0x3	clk_spdif_8ch_clk_sel clk_spdif_8ch clock select control register 2'b00:clk_spdif_divout 2'b01:clk_spdif_frac 2'b10:clkin_spdif from IO SAME AS clkin_i2s 2'b11:clk_12m
12:8	RW	0x03	clk_dptx_spdif_rec_div_con clk_dptx_spdif_rec divider control register clk=clk_src/(div_con+1)
7	RW	0x0	clk_spdif_8ch_pll_sel clk_spdif_8ch clock source select control register 1'b0:CPLL 1'b1:GPLL
6:0	RW	0x00	clk_spdif_8ch_pll_div_con clk_spdif_8ch_pll divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON33

Address: Operational Base + offset (0x0184)
Internal clock select and divide register33

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	clk_uart_pll_sel clk_uart clock source select control register 1'b0:CPLL 1'b1:GPLL
14	RO	0x0	reserved
13:12	RW	0x0	clk_uart0_src_sel clk_uart0_src clock select control register 2'b00:CPLL 2'b01:GPLL 2'b1x:USB_480M
11:10	RO	0x0	reserved
9:8	RW	0x2	clk_uart0_sel clk_uart0 clock select control register 2'b00:clk_uart0_divout 2'b01:clk_uart0_frac 2'b10:xin_24m
7	RO	0x0	reserved
6:0	RW	0x00	clk_uart0_div_con clk_uart0 divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON34
Address: Operational Base + offset (0x0188)
Internal clock select and divide register34

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	clk_write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:10	RO	0x0	reserved
9:8	RW	0x2	clk_uart1_sel clk_uart1 clock select control register 2'b00:clk_uart1_divout 2'b01:clk_uart1_frac 2'b10:xin_24m
7	RO	0x0	reserved
6:0	RW	0x00	clk_uart1_div_con clk_uart1 divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON35
Address: Operational Base + offset (0x018c)
Internal clock select and divide register35

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:10	RO	0x0	reserved
9:8	RW	0x2	clk_uart2_sel clk_uart2 clock select control register 2'b00:clk_uart2_divout 2'b01:clk_uart2_frac 2'b10:xin_24m
7	RO	0x0	reserved
6:0	RW	0x00	clk_uart2_div_con clk_uart2 divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON36
Address: Operational Base + offset (0x0190)
Internal clock select and divide register36

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:10	RO	0x0	reserved
9:8	RW	0x2	clk_uart3_sel clk_uart3 clock select control register 2'b00:clk_uart3_divout 2'b01:clk_uart3_frac 2'b10:xin_24m
7	RO	0x0	reserved
6:0	RW	0x00	clk_uart3_div_con clk_uart3 divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON38
Address: Operational Base + offset (0x0198)
Internal clock select and divide register38

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit

Bit	Attr	Reset Value	Description
15:14	RW	0x0	clk_testout2_pll_sel clk_testout2 clock source select control register 2'b00:CPLL 2'b01:GPLL 2'b1x:NPLL
13	RW	0x1	clk_testout2_clk_sel clk_testout2 clock select control register 1'b0:clk_testout_src 1'b1:xin_24m
12:8	RW	0x1f	clk_testout2_div_con clk_testout2 divider control register clk=clk_src/(div_con+1)
7:6	RW	0x0	clk_testout1_pll_sel clk_testout1 clock source select control register 2'b00:CPLL 2'b01:GPLL 2'b1x:NPLL
5	RW	0x1	clk_testout1_clk_sel clk_testout1 clock select control register 1'b0:clk_testout_src 1'b1:xin_24m
4:0	RW	0x1f	clk_testout1_div_con clk_testout1 divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON39
Address: Operational Base + offset (0x019c)
Internal clock select and divide register39

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:8	RO	0x0	reserved
7:6	RW	0x1	aclk_usb3_pll_sel aclk_usb3 clock source select control register 2'b00:CPLL 2'b01:GPLL 2'b1x:NPLL
5	RO	0x0	reserved
4:0	RW	0x01	aclk_usb3_div_con aclk_usb3 divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON40

Address: Operational Base + offset (0x01a0)
Internal clock select and divide register40

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	clk_usb3_otg0_suspend_src_sel clk_usb3_otg0_suspend_src clock select control register 1'b0:xin_24m 1'b1:clk_32k
14:10	RO	0x0	reserved
9:0	RW	0x000	clk_usb3_otg0_suspend_div_con clk_usb3_otg0_suspend divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON41
Address: Operational Base + offset (0x01a4)
Internal clock select and divide register41

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	clk_usb3_otg1_suspend_src_sel clk_usb3_otg1_suspend_src clock select control register 1'b0:xin_24m 1'b1:clk_32k
14:10	RO	0x0	reserved
9:0	RW	0x000	clk_usb3_otg1_suspend_div_con clk_usb3_otg1_suspend divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON42
Address: Operational Base + offset (0x01a8)
Internal clock select and divide register42

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RW	0x0	aclk_hdcp_pll_sel aclk_hdcp clock source select control register 2'b00:CPLL 2'b01:GPLL 2'b10:PPLL

Bit	Attr	Reset Value	Description
13	RO	0x0	reserved
12:8	RW	0x01	aclk_hdcp_div_con aclk_hdcp divider control register clk=clk_src/(div_con+1)
7:6	RW	0x0	aclk_vio_pll_sel aclk_vio clock source select control register 2'b00:CPLL 2'b01:GPLL 2'b10:PPLL
5	RO	0x0	reserved
4:0	RW	0x01	aclk_vio_div_con aclk_vio divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON43
Address: Operational Base + offset (0x01ac)
Internal clock select and divide register43

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14:10	RW	0x01	pclk_hdcp_div_con pclk_hdcp divider control register clk=clk_src/(div_con+1)
9:5	RW	0x01	hclk_hdcp_div_con hclk_hdcp divider control register clk=clk_src/(div_con+1)
4:0	RW	0x01	pclk_vio_div_con pclk_vio divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON44
Address: Operational Base + offset (0x01b0)
Internal clock select and divide register44

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	pclk_edp_pll_sel pclk_edp clock source select control register 1'b0:CPLL 1'b1:GPLL

Bit	Attr	Reset Value	Description
14	RO	0x0	reserved
13:8	RW	0x07	pclk_edp_div_con pclk_edp divider control register clk=clk_src/(div_con+1)
7:0	RO	0x0	reserved

CRU_CLKSEL_CON45
Address: Operational Base + offset (0x01b4)
Internal clock select and divide register45

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	clk_hdmi_cec_src_sel clk_hdmi_cec_src clock select control register 1'b0:clk_32k 1'b1:xin_24m
14:10	RO	0x0	reserved
9:0	RW	0x2dc	clk_hdmi_cec_div_con clk_hdmi_cec divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON46
Address: Operational Base + offset (0x01b8)
Internal clock select and divide register46

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:8	RO	0x0	reserved
7:6	RW	0x0	clk_dp_core_pll_sel clk_dp_core clock source select control register 2'b00:NPLL 2'b01:CPLL 2'b10:GPLL
5	RO	0x0	reserved
4:0	RW	0x04	clk_dp_core_div_con clk_dp_core divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON47
Address: Operational Base + offset (0x01bc)
Internal clock select and divide register47

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:13	RO	0x0	reserved
12:8	RW	0x01	hclk_vop0_div_con hclk_vop0 divider control register clk=clk_src/(div_con+1)
7:6	RW	0x0	aclk_vop0_pll_sel aclk_vop0 clock source select control register 2'b00:VPLL 2'b01:CPLL 2'b10:GPLL 2'b11:NPLL
5	RO	0x0	reserved
4:0	RW	0x02	aclk_vop0_div_con aclk_vop0 divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON48
Address: Operational Base + offset (0x01c0)
Internal clock select and divide register48

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:13	RO	0x0	reserved
12:8	RW	0x01	hclk_vop1_div_con hclk_vop1 divider control register clk=clk_src/(div_con+1)
7:6	RW	0x0	aclk_vop1_pll_sel aclk_vop1 clock source select control register 2'b00:VPLL 2'b01:CPLL 2'b10:GPLL 2'b11:NPLL
5	RO	0x0	reserved
4:0	RW	0x02	aclk_vop1_div_con aclk_vop1 divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON49
Address: Operational Base + offset (0x01c4)
Internal clock select and divide register49

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:12	RO	0x0	reserved
11	RW	0x0	dclk_vop0_dclk_sel dclk_vop0 clock select control register 1'b0:dclk_vop_divout 1'b1:dclk_vop_frac
10	RO	0x0	reserved
9:8	RW	0x0	dclk_vop0_pll_sel dclk_vop0 clock source select control register 2'b00:VPLL 2'b01:CPLL 2'b1x:GPLL
7:0	RW	0x01	dclk_vop0_div_con dclk_vop0 divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON50
Address: Operational Base + offset (0x01c8)
Internal clock select and divide register50

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:12	RO	0x0	reserved
11	RW	0x0	dclk_vop1_dclk_sel dclk_vop1 clock select control register 1'b0:dclk_vop_divout 1'b1:dclk_vop_frac
10	RO	0x0	reserved
9:8	RW	0x0	dclk_vop1_pll_sel dclk_vop1 clock source select control register 2'b00:VPLL 2'b01:CPLL 2'b1x:GPLL
7:0	RW	0x03	dclk_vop1_div_con vop1 divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON51
Address: Operational Base + offset (0x01cc)
Internal clock select and divide register51

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:8	RO	0x0	reserved
7:6	RW	0x0	clk_vop0_pwm_src_sel vop0_pwm_src clock select control register 2'b00:VPLL 2'b01:CPLL 2'b1x:GPLL
5	RO	0x0	reserved
4:0	RW	0x05	clk_vop0_pwm_div_con vop0_pwm divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON52
Address: Operational Base + offset (0x01d0)
Internal clock select and divide register52

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:8	RO	0x0	reserved
7:6	RW	0x0	clk_vop1_pwm_src_sel vop1_pwm_src clock select control register 2'b00:VPLL 2'b01:CPLL 2'b1x:GPLL
5	RO	0x0	reserved
4:0	RW	0x05	clk_vop1_pwm_div_con vop1_pwm divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON53
Address: Operational Base + offset (0x01d4)
Internal clock select and divide register53

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:13	RO	0x0	reserved

Bit	Attr	Reset Value	Description
12:8	RW	0x01	hclk_isp0_div_con hclk_isp0 divider control register clk=clk_src/(div_con+1)
7:6	RW	0x0	aclk_isp0_pll_sel aclk_isp0 clock source select control register 2'b00:CPLL 2'b01:GPLL 2'b10:PPLL
5	RO	0x0	reserved
4:0	RW	0x01	aclk_isp0_div_con aclk_isp0 divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON54
Address: Operational Base + offset (0x01d8)
Internal clock select and divide register54

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:13	RO	0x0	reserved
12:8	RW	0x01	hclk_isp1_div_con hclk_isp1 divider control register clk=clk_src/(div_con+1)
7:6	RW	0x0	aclk_isp1_pll_sel aclk_isp1 clock source select control register 2'b00:CPLL 2'b01:GPLL 2'b10:PPLL
5	RO	0x0	reserved
4:0	RW	0x01	aclk_isp1_div_con aclk_isp1 divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON55
Address: Operational Base + offset (0x01dc)
Internal clock select and divide register55

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit

Bit	Attr	Reset Value	Description
15:14	RW	0x2	clk_isp1_pll_sel clk_isp1 clock source select control register 2'b00:CPLL 2'b01:GPLL 2'b1x:NPLL
13	RO	0x0	reserved
12:8	RW	0x01	clk_isp1_div_con clk_isp1 divider control register clk=clk_src/(div_con+1)
7:6	RW	0x2	clk_isp0_pll_sel clk_isp0 clock source select control register 2'b00:CPLL 2'b01:GPLL 2'b1x:NPLL
5	RO	0x0	reserved
4:0	RW	0x01	clk_isp0_div_con clk_isp0 divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON56
Address: Operational Base + offset (0x01e0)
Internal clock select and divide register56

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	aclk_gic_pll_sel aclk_gic source select control register 1'b0:CPLL 1'b1:GPLL
14:13	RO	0x0	reserved
12:8	RW	0x03	aclk_gic_div_con aclk_gic divider control register clk=clk_src/(div_con+1)
7:6	RW	0x0	clk_cif_pll_sel clk_cif clock source select control register 2'b00:CPLL 2'b01:GPLL 2'b1x:NPLL
5	RW	0x1	clk_cif_clk_sel clk_cif clock select control register 1'b0:clk_cif_src 1'b1:xin_24m

Bit	Attr	Reset Value	Description
4:0	RW	0x00	clk_cif_div_con clk_cif divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON57
Address: Operational Base + offset (0x01e4)
Internal clock select and divide register57

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:6	RW	0x000	clkout_24m_div_con clkout_24m divider control register clk=clk_src/(div_con+1)
5	RO	0x0	reserved
4:0	RW	0x05	pclk_alive_div_con pclk_alive divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON58
Address: Operational Base + offset (0x01e8)
Internal clock select and divide register58

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	clk_spi5_pll_sel clk_spi5 clock source select control register 1'b0:CPLL 1'b1:GPLL
14:8	RW	0x07	clk_spi5_div_con spi5 divider control register clk=clk_src/(div_con+1)
7	RW	0x0	clk_testfrac_pll_sel clk_frac clock source select control register 1'b0:CPLL 1'b1:GPLL
6:5	RO	0x0	reserved
4:0	RW	0x1f	clk_test_div_con test divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON59
Address: Operational Base + offset (0x01ec)
Internal clock select and divide register59

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	clk_spi1_pll_sel clk_spi1 clock source select control register 1'b0:CPLL 1'b1:GPLL
14:8	RW	0x07	clk_spi1_div_con spi1 divider control register clk=clk_src/(div_con+1)
7	RW	0x0	clk_spi0_pll_sel clk_spi0 clock source select control register 1'b0:CPLL 1'b1:GPLL
6:0	RW	0x07	clk_spi0_div_con spi0 divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON60
Address: Operational Base + offset (0x01f0)
Internal clock select and divide register60

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	clk_spi4_pll_sel clk_spi4 clock source select control register 1'b0:CPLL 1'b1:GPLL
14:8	RW	0x07	clk_spi4_div_con spi4 divider control register clk=clk_src/(div_con+1)
7	RW	0x0	clk_spi2_pll_sel clk_spi2 clock source select control register 1'b0:CPLL 1'b1:GPLL
6:0	RW	0x07	clk_spi2_div_con spi2 divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON61
Address: Operational Base + offset (0x01f4)
Internal clock select and divide register61

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	clk_i2c5_pll_sel clk_i2c5 clock source select control register 1'b0:CPLL 1'b1:GPLL
14:8	RW	0x03	clk_i2c5_div_con i2c5 divider control register clk=clk_src/(div_con+1)
7	RW	0x0	clk_i2c1_pll_sel clk_i2c1 clock source select control register 1'b0:CPLL 1'b1:GPLL
6:0	RW	0x03	clk_i2c1_div_con i2c1 divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON62
Address: Operational Base + offset (0x01f8)
Internal clock select and divide register62

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	clk_i2c6_pll_sel clk_i2c6 clock source select control register 1'b0:CPLL 1'b1:GPLL
14:8	RW	0x03	clk_i2c6_div_con i2c6 divider control register clk=clk_src/(div_con+1)
7	RW	0x0	clk_i2c2_pll_sel clk_i2c2 clock source select control register 1'b0:CPLL 1'b1:GPLL
6:0	RW	0x03	clk_i2c2_div_con i2c2 divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON63
Address: Operational Base + offset (0x01fc)
Internal clock select and divide register63

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	clk_i2c7_pll_sel clk_i2c7 clock source select control register 1'b0:CPLL 1'b1:GPLL
14:8	RW	0x03	clk_i2c7_div_con i2c7 divider control register clk=clk_src/(div_con+1)
7	RW	0x0	clk_i2c3_pll_sel clk_i2c3 clock source select control register 1'b0:CPLL 1'b1:GPLL
6:0	RW	0x03	clk_i2c3_div_con i2c3 divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON64
Address: Operational Base + offset (0x0200)
Internal clock select and divide register64

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	clk_uphy0_tcpdphy_ref_clk_sel clk_uphy0_tcpdphy_ref clock select control register 1'b0:xin_24m 1'b1:clk_32k
14:13	RO	0x0	reserved
12:8	RW	0x00	clk_uphy0_tcpdphy_ref_div_con clk_uphy0_tcpdphy_ref divider control register clk=clk_src/(div_con+1)
7:6	RW	0x3	clk_uphy0_tcpdcore_clk_sel clk_uphy0_tcpdcore clock select control register 2'b00:xin_24m 2'b01:clk_32k 2'b10:cpll 2'b11:gpll
5	RO	0x0	reserved

Bit	Attr	Reset Value	Description
4:0	RW	0x05	clk_uphy0_tcpdcore_div_con clk_uphy0_tcpdcore divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON65
Address: Operational Base + offset (0x0204)
Internal clock select and divide register65

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	clk_uphy1_tcpdphy_ref_clk_sel clk_uphy1_tcpdphy_ref clock select control register 1'b0:xin_24m 1'b1:clk_32k
14:13	RO	0x0	reserved
12:8	RW	0x00	clk_uphy1_tcpdphy_ref_div_con clk_uphy1_tcpdphy_ref divider control register clk=clk_src/(div_con+1)
7:6	RW	0x3	clk_uphy1_tcpdcore_clk_sel clk_uphy1_tcpdcore clock select control register 2'b00:xin_24m 2'b01:clk_32k 2'b10:cpll 2'b11:gpll
5	RO	0x0	reserved
4:0	RW	0x05	clk_uphy1_tcpdcore_div_con clk_uphy1_tcpdcore divider control register clk=clk_src/(div_con+1)

CRU_CLKSEL_CON96
Address: Operational Base + offset (0x0280)
Internal clock select and divide register80

Bit	Attr	Reset Value	Description
31:0	RW	0x0bb8ea60	clk_i2s0_frac_div_con clk_i2s0_frac divider control register Fout = Fsrc*numerator/denominator High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL_CON97
Address: Operational Base + offset (0x0284)
Internal clock select and divide register81

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x0bb8ea60	clk_i2s1_frac_div_con clk_i2s1_frac divider control register Fout = Fsrc*numerator/denominator High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL_CON98
Address: Operational Base + offset (0x0288)
Internal clock select and divide register82

Bit	Attr	Reset Value	Description
31:0	RW	0x0bb8ea60	clk_i2s2_frac_div_con clk_i2s2_frac divider control register Fout = Fsrc*numerator/denominator High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL_CON99
Address: Operational Base + offset (0x028c)
Internal clock select and divide register83

Bit	Attr	Reset Value	Description
31:0	RW	0x0bb8ea60	clk_spdif_8ch_frac_div_con spdif_8ch_frac divider control register Fout = Fsrc*numerator/denominator High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL_CON100
Address: Operational Base + offset (0x0290)
Internal clock select and divide register84

Bit	Attr	Reset Value	Description
31:0	RW	0x0bb8ea60	clk_uart0_frac_div_con uart0_frac divider control register Fout = Fsrc*numerator/denominator High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL_CON101
Address: Operational Base + offset (0x0294)
Internal clock select and divide register85

Bit	Attr	Reset Value	Description
31:0	RW	0x0bb8ea60	clk_uart1_frac_div_con uart1_frac divider control register Fout = Fsrc*numerator/denominator High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL_CON102
Address: Operational Base + offset (0x0298)
Internal clock select and divide register86

Bit	Attr	Reset Value	Description
31:0	RW	0x0bb8ea60	clk_uart2_frac_div_con uart2_frac divider control register Fout = Fsrc*numerator/denominator High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL_CON103
Address: Operational Base + offset (0x029c)
Internal clock select and divide register87

Bit	Attr	Reset Value	Description
31:0	RW	0x0bb8ea60	clk_uart3_frac_div_con uart3_frac divider control register Fout = Fsrc*numerator/denominator High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL_CON105
Address: Operational Base + offset (0x02a4)
Internal clock select and divide register89

Bit	Attr	Reset Value	Description
31:0	RW	0x0bb8ea60	clk_testfrac_frac_div_con clk_testfrac frac divider control register Fout = Fsrc*numerator/denominator High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL_CON106
Address: Operational Base + offset (0x02a8)
Internal clock select and divide register90

Bit	Attr	Reset Value	Description
31:0	RW	0x0bb8ea60	dclk_vop0_frac_div_con dclk_vop0_frac divider control register Fout = Fsrc*numerator/denominator High 16-bit for numerator Low 16-bit for denominator

CRU_CLKSEL_CON107
Address: Operational Base + offset (0x02ac)
Internal clock select and divide register91

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x0bb8ea60	dclk_vop1_frac_div_con dclk_vop1_frac divider control register Fout = Fsrc*numerator/denominator High 16-bit for numerator Low 16-bit for denominator

CRU_CLKGATE_CON0

Address: Operational Base + offset (0x0300)

Internal clock gating register0

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:8	RO	0x0	reserved
7	RW	0x0	clk_pvtm_core_l_en clk_pvtm_core_l clock disable bit When HIGH, disable clock
6	RW	0x0	pclk_coredbg_l_en pclk_coredbg_l clock disable bit When HIGH, disable clock
5	RW	0x0	atclk_core_l_en atclk_core_l clock disable bit When HIGH, disable clock
4	RW	0x0	aclkm_core_l_en aclkm_core_l clock disable bit When HIGH, disable clock
3	RW	0x0	clk_core_l_gpll_src_en clk_core_l_gpll clock disable bit When HIGH, disable clock
2	RW	0x0	clk_core_l_dpll_src_en clk_core_l_dpll clock disable bit When HIGH, disable clock
1	RW	0x0	clk_core_l_bpll_src_en clk_core_l_bpll clock disable bit When HIGH, disable clock
0	RW	0x0	clk_core_l_lpll_src_en clk_core_l_lpll clock disable bit When HIGH, disable clock

CRU_CLKGATE_CON1

Address: Operational Base + offset (0x0304)

Internal clock gating register1

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:8	RO	0x0	reserved
7	RW	0x0	clk_pvtm_core_b_en clk_pvtm_core_b clock disable bit When HIGH, disable clock
6	RW	0x0	pclk_coredbg_b_en pclk_coredbg_b clock disable bit When HIGH, disable clock
5	RW	0x0	atclk_core_b_en atclk_core_b clock disable bit When HIGH, disable clock
4	RW	0x0	aclkm_core_b_en aclkm_core_b clock disable bit When HIGH, disable clock
3	RW	0x0	clk_core_b_gpll_src_en clk_core_b_gpll clock disable bit When HIGH, disable clock
2	RW	0x0	clk_core_b_dpll_src_en clk_core_b_dpll clock disable bit When HIGH, disable clock
1	RW	0x0	clk_core_b_bpll_src_en clk_core_b_bpll clock disable bit When HIGH, disable clock
0	RW	0x0	clk_core_b_lpll_src_en clk_core_b_lpll clock disable bit When HIGH, disable clock

CRU_CLKGATE_CON2

Address: Operational Base + offset (0x0308)

Internal clock gating register2

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:11	RO	0x0	reserved
10	RW	0x0	cs_npll_clk_en cs_npll_clk clock disable bit When HIGH, disable clock
9	RW	0x0	cs_gpll_clk_en cs_gpll_clk clock disable bit When HIGH, disable clock

Bit	Attr	Reset Value	Description
8	RW	0x0	cs_cpll_clk_en cs_cpll_clk clock disable bit When HIGH, disable clock
7	RW	0x0	clk_cci_trace_en clk_cci_trace clock disable bit When HIGH, disable clock
6	RW	0x0	clk_cci_trace_gpll_src_en clk_cci_trace_gpll clock disable bit When HIGH, disable clock
5	RW	0x0	clk_cci_trace_cpll_src_en clk_cci_trace_cpll clock disable bit When HIGH, disable clock
4	RW	0x0	aclk_cci_src_en aclk_cci_src clock disable bit When HIGH, disable clock
3	RW	0x0	aclk_cci_vpll_src_en aclk_cci_vpll clock disable bit When HIGH, disable clock
2	RW	0x0	aclk_cci_npll_src_en aclk_cci_npll clock disable bit When HIGH, disable clock
1	RW	0x0	aclk_cci_gpll_src_en aclk_cci_gpll clock disable bit When HIGH, disable clock
0	RW	0x0	aclk_cci_cpll_src_en aclk_cci_cpll clock disable bit When HIGH, disable clock

CRU_CLKGATE_CON3

Address: Operational Base + offset (0x030c)

Internal clock gating register3

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:8	RO	0x0	reserved
7	RW	0x0	aclk_center_src_en aclk_center_src clock disable bit When HIGH, disable clock
6	RW	0x0	reserved
5	RW	0x0	reserved
4	RW	0x0	pclk_ddr_en pclk_ddr clock disable bit When HIGH, disable clock

Bit	Attr	Reset Value	Description
3	RW	0x0	clk_ddrc_gpll_src_en clk_ddrc_gpll clock disable bit When HIGH, disable clock
2	RW	0x0	clk_ddrc_dpll_src_en clk_ddrc_dpll clock disable bit When HIGH, disable clock
1	RW	0x0	clk_ddrc_bpll_src_en clk_ddrc_bpll clock disable bit When HIGH, disable clock
0	RW	0x0	clk_ddrc_lpll_src_en clk_ddrc_lpll clock disable bit When HIGH, disable clock

CRU_CLKGATE_CON4
Address: Operational Base + offset (0x0310)
Internal clock gating register4

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:12	RO	0x0	reserved
11	RW	0x0	clk_pvtm_ddr_en clk_pvtm_ddr clock disable bit When HIGH, disable clock
10	RW	0x0	clk_rga_core_src_en clk_rga_core_src clock disable bit When HIGH, disable clock
9	RW	0x0	hclk_rga_src_en hclk_rga_src clock disable bit When HIGH, disable clock
8	RW	0x0	aclk_rga_src_en aclk_rga_src clock disable bit When HIGH, disable clock
7	RW	0x0	hclk_iep_src_en hclk_iep_src clock disable bit When HIGH, disable clock
6	RW	0x0	aclk_iep_src_en aclk_iep_src clock disable bit When HIGH, disable clock
5	RW	0x0	clk_vdu_ca_src_en clk_vdu_ca_src clock disable bit When HIGH, disable clock

Bit	Attr	Reset Value	Description
4	RW	0x0	clk_vdu_core_src_en clk_vdu_core_src clock disable bit When HIGH, disable clock
3	RW	0x0	hclk_vdu_src_en hclk_vdu_src clock disable bit When HIGH, disable clock
2	RW	0x0	aclk_vdu_src_en aclk_vdu_src clock disable bit When HIGH, disable clock
1	RW	0x0	hclk_vcodec_src_en hclk_vcodec_src clock disable bit When HIGH, disable clock
0	RW	0x0	aclk_vcodec_src_en aclk_vcodec_src clock disable bit When HIGH, disable clock

CRU_CLKGATE_CON5

Address: Operational Base + offset (0x0314)

Internal clock gating register5

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:10	RO	0x0	reserved
9	RW	0x0	clk_mac_tx_en clk_mac_tx clock disable bit When HIGH, disable clock
8	RW	0x0	clk_mac_rx_en clk_mac_rx clock disable bit When HIGH, disable clock
7	RW	0x0	clk_mac_refout_en clk_mac_refout clock disable bit When HIGH, disable clock
6	RW	0x0	clk_mac_ref_en clk_mac_ref clock disable bit When HIGH, disable clock
5	RW	0x0	clk_gmac_src_en clk_gmac_src clock disable bit When HIGH, disable clock
4	RW	0x0	pclk_perihp_en pclk_perihp clock disable bit When HIGH, disable clock

Bit	Attr	Reset Value	Description
3	RW	0x0	hclk_perihp_en hclk_perihp clock disable bit When HIGH, disable clock
2	RW	0x0	aclk_perihp_en aclk_perihp clock disable bit When HIGH, disable clock
1	RW	0x0	aclk_perihp_cpll_src_en aclk_perihp_cpll clock disable bit When HIGH, disable clock
0	RW	0x0	aclk_perihp_gpll_src_en aclk_perihp_gpll clock disable bit When HIGH, disable clock

CRU_CLKGATE_CON6
Address: Operational Base + offset (0x0318)
Internal clock gating register6

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14	RW	0x0	clk_emmc_src_en clk_emmc_src clock disable bit When HIGH, disable clock
13	RW	0x0	aclk_emmc_cpll_src_en aclk_emmc_cpll clock disable bit When HIGH, disable clock
12	RW	0x0	aclk_emmc_gpll_src_en aclk_emmc_gpll clock disable bit When HIGH, disable clock
11	RW	0x0	pclk_gmac_en pclk_gmac clock disable bit When HIGH, disable clock
10	RW	0x0	aclk_gmac_en aclk_gmac clock disable bit When HIGH, disable clock
9	RW	0x0	aclk_gmac_cpll_src_en aclk_gmac_cpll clock disable bit When HIGH, disable clock
8	RW	0x0	aclk_gmac_gpll_src_en aclk_gmac_gpll clock disable bit When HIGH, disable clock
7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6	RW	0x0	clk_usb2phy1_ref_en clk_usb2phy1_ref clock disable bit When HIGH, disable clock
5	RW	0x0	clk_usb2phy0_ref_en clk_usb2phy0_ref clock disable bit When HIGH, disable clock
4	RW	0x0	clk_hsicphy_en clk_hsicphy clock disable bit When HIGH, disable clock
3	RW	0x0	clk_pcie_core_src_en clk_pcie_core_src clock disable bit When HIGH, disable clock
2	RW	0x0	clk_pcie_pm_src_en clk_pcie_pm_src clock disable bit When HIGH, disable clock
1	RW	0x0	clk_sdmmc_src_en clk_sdmmc_src clock disable bit When HIGH, disable clock
0	RW	0x0	clk_sdio_src_en clk_sdio_src clock disable bit When HIGH, disable clock

CRU_CLKGATE_CON7
Address: Operational Base + offset (0x031c)
Internal clock gating register7

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:10	RO	0x0	reserved
9	RW	0x0	fclk_cm0s_en fclk_cm0s clock disable bit When HIGH, disable clock
8	RW	0x0	clk_crypto1_en clk_crypto1 clock disable bit When HIGH, disable clock
7	RW	0x0	clk_crypto0_en clk_crypto0 clock disable bit When HIGH, disable clock
6	RW	0x0	clk_cm0s_cpll_src_en clk_cm0s_cpll clock disable bit When HIGH, disable clock

Bit	Attr	Reset Value	Description
5	RW	0x0	clk_cm0s_gpll_src_en clk_cm0s_gpll clock disable bit When HIGH, disable clock
4	RW	0x0	pclk_perilp0_en pclk_perilp0 clock disable bit When HIGH, disable clock
3	RW	0x0	hclk_perilp0_en hclk_perilp0 clock disable bit When HIGH, disable clock
2	RW	0x0	aclk_perilp0_en aclk_perilp0 clock disable bit When HIGH, disable clock
1	RW	0x0	aclk_perilp0_cpll_src_en aclk_perilp0_cpll clock disable bit When HIGH, disable clock
0	RW	0x0	aclk_perilp0_gpll_src_en aclk_perilp0_gpll clock disable bit When HIGH, disable clock

CRU_CLKGATE_CON8
Address: Operational Base + offset (0x0320)
Internal clock gating register8

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	clk_spdif_8ch_en clk_spdif_8ch clock disable bit When HIGH, disable clock
14	RW	0x0	clk_spdif_8ch_frac_src_en clk_spdif_8ch_frac_src clock disable bit When HIGH, disable clock
13	RW	0x0	clk_spdif_8ch_src_en clk_spdif_8ch_src clock disable bit When HIGH, disable clock
12	RW	0x0	clk_i2s_out_en clk_i2s_out clock disable bit When HIGH, disable clock
11	RW	0x0	clk_i2s2_en clk_i2s2 clock disable bit When HIGH, disable clock
10	RW	0x0	clk_i2s2_frac_src_en clk_i2s2_frac_src clock disable bit When HIGH, disable clock

Bit	Attr	Reset Value	Description
9	RW	0x0	clk_i2s2_src_en clk_i2s2_src clock disable bit When HIGH, disable clock
8	RW	0x0	clk_i2s1_en clk_i2s1 clock disable bit When HIGH, disable clock
7	RW	0x0	clk_i2s1_frac_src_en clk_i2s1_frac_src clock disable bit When HIGH, disable clock
6	RW	0x0	clk_i2s1_src_en clk_i2s1_src clock disable bit When HIGH, disable clock
5	RW	0x0	clk_i2s0_en clk_i2s0 clock disable bit When HIGH, disable clock
4	RW	0x0	clk_i2s0_frac_src_en clk_i2s0_frac_src clock disable bit When HIGH, disable clock
3	RW	0x0	clk_i2s0_src_en clk_i2s0_src clock disable bit When HIGH, disable clock
2	RW	0x0	pclk_perilp1_en pclk_perilp1 clock disable bit When HIGH, disable clock
1	RW	0x0	hclk_perilp1_cpll_src_en hclk_perilp1_cpll clock disable bit When HIGH, disable clock
0	RW	0x0	hclk_perilp1_gpll_src_en hclk_perilp1_gpll clock disable bit When HIGH, disable clock

CRU_CLKGATE_CON9

Address: Operational Base + offset (0x0324)

Internal clock gating register9

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	clk_spi4_src_en clk_spi4_src clock disable bit When HIGH, disable clock
14	RW	0x0	clk_spi2_src_en clk_spi2_src clock disable bit When HIGH, disable clock

Bit	Attr	Reset Value	Description
13	RW	0x0	clk_spi1_src_en clk_spi1_src clock disable bit When HIGH, disable clock
12	RW	0x0	clk_spi0_src_en clk_spi0_src clock disable bit When HIGH, disable clock
11	RW	0x0	clk_saradc_src_en clk_saradc_src clock disable bit When HIGH, disable clock
10	RW	0x0	clk_tsadc_src_en clk_tsadc_src clock disable bit When HIGH, disable clock
9:8	RO	0x0	reserved
7	RW	0x0	clk_uart3_frac_src_en clk_uart3_frac_src clock disable bit When HIGH, disable clock
6	RW	0x0	clk_uart3_src_en clk_uart3_src clock disable bit When HIGH, disable clock
5	RW	0x0	clk_uart2_frac_src_en clk_uart2_frac_src clock disable bit When HIGH, disable clock
4	RW	0x0	clk_uart2_src_en clk_uart2_src clock disable bit When HIGH, disable clock
3	RW	0x0	clk_uart1_frac_src_en clk_uart1_frac_src clock disable bit When HIGH, disable clock
2	RW	0x0	clk_uart1_src_en clk_uart1_src clock disable bit When HIGH, disable clock
1	RW	0x0	clk_uart0_frac_src_en clk_uart0_frac_src clock disable bit When HIGH, disable clock
0	RW	0x0	clk_uart0_src_en clk_uart0_src clock disable bit When HIGH, disable clock

CRU_CLKGATE_CON10

Address: Operational Base + offset (0x0328)

Internal clock gating register10

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	clk_vop1_pwm_en clk_vop1_pwm clock disable bit When HIGH, disable clock
14	RW	0x0	clk_vop0_pwm_en clk_vop0_pwm clock disable bit When HIGH, disable clock
13	RW	0x0	dclk_vop1_src_en dclk_vop1_src clock disable bit When HIGH, disable clock
12	RW	0x0	dclk_vop0_src_en dclk_vop0_src clock disable bit When HIGH, disable clock
11	RW	0x0	hclk_vop1_pre_en hclk_vop1_pre clock disable bit When HIGH, disable clock
10	RW	0x0	aclk_vop1_pre_src_en aclk_vop1_pre_src clock disable bit When HIGH, disable clock
9	RW	0x0	hclk_vop0_pre_en hclk_vop0_pre clock disable bit When HIGH, disable clock
8	RW	0x0	aclk_vop0_pre_src_en aclk_vop0_pre_src clock disable bit When HIGH, disable clock
7	RW	0x0	clk_cif_out_src_en clk_cif_out_src clock disable bit When HIGH, disable clock
6	RW	0x0	clk_dptx_spdif_rec_src_en clk_dptx_spdif_rec_src clock disable bit When HIGH, disable clock
5	RW	0x0	clk_i2c7_src_en clk_i2c7_src clock disable bit When HIGH, disable clock
4	RW	0x0	clk_i2c3_src_en clk_i2c3_src clock disable bit When HIGH, disable clock
3	RW	0x0	clk_i2c6_src_en clk_i2c6_src clock disable bit When HIGH, disable clock

Bit	Attr	Reset Value	Description
2	RW	0x0	clk_i2c2_src_en clk_i2c2_src clock disable bit When HIGH, disable clock
1	RW	0x0	clk_i2c5_src_en clk_i2c5_src clock disable bit When HIGH, disable clock
0	RW	0x0	clk_i2c1_src_en clk_i2c1_src clock disable bit When HIGH, disable clock

CRU_CLKGATE_CON11

Address: Operational Base + offset (0x032c)

Internal clock gating register11

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	clk_mipidphy_cfg_en clk_mipidphy_cfg clock disable bit When HIGH, disable clock
14	RW	0x0	clk_mipidphy_ref_en clk_mipidphy_ref clock disable bit When HIGH, disable clock
13:12	RO	0x0	reserved
11	RW	0x0	pclk_edp_en pclk_edp clock disable bit When HIGH, disable clock
10	RW	0x0	pclk_hdcp_en pclk_hdcp clock disable bit When HIGH, disable clock
9	RO	0x0	reserved
8	RW	0x0	clk_dp_core_src_en clk_dp_core_src clock disable bit When HIGH, disable clock
7	RW	0x0	clk_hdmi_cec_en clk_hdmi_cec clock disable bit When HIGH, disable clock
6	RW	0x0	clk_hdmi_sfr_en clk_hdmi_sfr clock disable bit When HIGH, disable clock
5	RW	0x0	clk_isp1_en clk_isp1 clock disable bit When HIGH, disable clock

Bit	Attr	Reset Value	Description
4	RW	0x0	clk_isp0_en clk_isp0 clock disable bit When HIGH, disable clock
3	RW	0x0	hclk_hdcp_en hclk_hdcp clock disable bit When HIGH, disable clock
2	RW	0x0	aclk_hdcp_src_en aclk_hdcp_src clock disable bit When HIGH, disable clock
1	RW	0x0	pclk_vio_en pclk_vio clock disable bit When HIGH, disable clock
0	RW	0x0	aclk_vio_src_en aclk_vio_src clock disable bit When HIGH, disable clock

CRU_CLKGATE_CON12

Address: Operational Base + offset (0x0330)

Internal clock gating register12

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RO	0x0	reserved
13	RW	0x0	hclk_sd_src_en hclk_sd_src clock disable bit When HIGH, disable clock
12	RW	0x0	aclk_gic_src_en aclk_gic_src clock disable bit When HIGH, disable clock
11	RW	0x0	hclk_isp1_en hclk_isp1 clock disable bit When HIGH, disable clock
10	RW	0x0	aclk_isp1_src_en aclk_isp1_src clock disable bit When HIGH, disable clock
9	RW	0x0	hclk_isp0_en hclk_isp0 clock disable bit When HIGH, disable clock
8	RW	0x0	aclk_isp0_src_en aclk_isp0_src clock disable bit When HIGH, disable clock
7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6	RW	0x0	clk_pciephy_ref100m_en clk_pciephy_ref100m clock disable bit When HIGH, disable clock
5	RO	0x0	reserved
4	RW	0x0	clk_usb3_otg1_suspend_en clk_usb3_otg1_suspend clock disable bit When HIGH, disable clock
3	RW	0x0	clk_usb3_otg0_suspend_en clk_usb3_otg0_suspend clock disable bit When HIGH, disable clock
2	RW	0x0	clk_usb3_otg1_ref_en clk_usb3_otg1_ref clock disable bit When HIGH, disable clock
1	RW	0x0	clk_usb3_otg0_ref_en clk_usb3_otg0_ref clock disable bit When HIGH, disable clock
0	RW	0x0	aclk_usb3_src_en aclk_usb3_src clock disable bit When HIGH, disable clock

CRU_CLKGATE_CON13
Address: Operational Base + offset (0x0334)
Internal clock gating register13

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	clk_testout2_src_en clk_testout2_src clock disable bit When HIGH, disable clock
14	RW	0x0	clk_testout1_src_en clk_testout1_src clock disable bit When HIGH, disable clock
13	RW	0x0	clk_spi5_src_en clk_spi5_src clock disable bit When HIGH, disable clock
12	RW	0x0	clk_usb480m_en clk_usb480m clock disable bit When HIGH, disable clock
11	RW	0x0	testclk_en testclk clock disable bit When HIGH, disable clock
10	RO	0x0	reserved

Bit	Attr	Reset Value	Description
9	RW	0x0	clk_wifi_en clk_wifi clock disable bit When HIGH, disable clock
8	RO	0x0	reserved
7	RW	0x0	clk_uphy1_tcpdcore_en clk_uphy1_tcpdcore clock disable bit When HIGH, disable clock
6	RW	0x0	clk_uphy1_tcpdphyref_en clk_uphy1_tcpdphyref clock disable bit When HIGH, disable clock
5	RW	0x0	clk_uphy0_tcpdcore_en clk_uphy0_tcpdcore clock disable bit When HIGH, disable clock
4	RW	0x0	clk_uphy0_tcpdphyref_en clk_uphy0_tcpdphyref clock disable bit When HIGH, disable clock
3:2	RO	0x0	reserved
1	RW	0x0	clk_pvtm_gpu_en clk_pvtm_gpu clock disable bit When HIGH, disable clock
0	RW	0x0	aclk_gpu_pll_src_en aclk_gpu_pll_src clock disable bit When HIGH, disable clock

CRU_CLKGATE_CON14

Address: Operational Base + offset (0x0338)

Internal clock gating register14

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RO	0x0	reserved
13	RW	0x0	aclk_perf_core_l_en aclk_perf_core_l clock disable bit When HIGH, disable clock
12	RW	0x0	aclk_core_adb400_core_l_2_cci500_en aclk_core_adb400_core_l_2_cci500 clock disable bit When HIGH, disable clock
11	RW	0x0	aclk_core_adb400_core_l_2_gic_en aclk_core_adb400_core_l_2_gic clock disable bit When HIGH, disable clock
10	RW	0x0	aclk_core_adb400_gic_2_core_l_en aclk_core_adb400_gic_2_core_l clock disable bit When HIGH, disable clock

Bit	Attr	Reset Value	Description
9	RW	0x0	clk_dbg_pd_core_l_en clk_dbg_pd_core_l clock disable bit When HIGH, disable clock
8:7	RO	0x0	reserved
6	RW	0x0	aclk_perf_core_b_en aclk_perf_core_b clock disable bit When HIGH, disable clock
5	RW	0x0	aclk_core_adb400_core_b_2_cci500_en aclk_core_adb400_core_b_2_cci500 clock disable bit When HIGH, disable clock
4	RW	0x0	aclk_core_adb400_core_b_2_gic_en aclk_core_adb400_core_b_2_gic clock disable bit When HIGH, disable clock
3	RW	0x0	aclk_core_adb400_gic_2_core_b_en aclk_core_adb400_gic_2_core_b clock disable bit When HIGH, disable clock
2	RW	0x0	pclk_dbg_cxcs_pd_core_b_en pclk_dbg_cxcs_pd_core_b clock disable bit When HIGH, disable clock
1	RW	0x0	clk_dbg_pd_core_b_en clk_dbg_pd_core_b clock disable bit When HIGH, disable clock
0	RO	0x0	reserved

CRU_CLKGATE_CON15

Address: Operational Base + offset (0x033c)

Internal clock gating register15

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:8	RO	0x0	reserved
7	RW	0x0	aclk_cci_grf_en aclk_cci_grf clock disable bit When HIGH, disable clock Suggest always on
6	RW	0x0	clk_dbg_noc_en clk_dbg_noc clock disable bit When HIGH, disable clock Suggest always on
5	RW	0x0	clk_dbg_cxcs_en clk_dbg_cxcs clock disable bit When HIGH, disable clock

Bit	Attr	Reset Value	Description
4	RW	0x0	aclk_cci_noc1_en aclk_cci_noc1 clock disable bit When HIGH, disable clock Suggest always on
3	RW	0x0	aclk_cci_noc0_en aclk_cci_noc0 clock disable bit When HIGH, disable clock Suggest always on
2	RW	0x0	aclk_cci_en aclk_cci clock disable bit When HIGH, disable clock
1	RW	0x0	aclk_adb400m_pd_core_b_en aclk_adb400m_pd_core_b clock disable bit When HIGH, disable clock
0	RW	0x0	aclk_adb400m_pd_core_l_en aclk_adb400m_pd_core_l clock disable bit When HIGH, disable clock

CRU_CLKGATE_CON16

Address: Operational Base + offset (0x0340)

Internal clock gating register16

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:12	RO	0x0	reserved
11	RW	0x0	hclk_rga_noc_en hclk_rga_noc clock disable bit When HIGH, disable clock Suggest always on
10	RW	0x0	hclk_rga_en hclk_rga clock disable bit When HIGH, disable clock
9	RW	0x0	aclk_rga_noc_en aclk_rga_noc clock disable bit When HIGH, disable clock Suggest always on
8	RW	0x0	aclk_rga_en aclk_rga clock disable bit When HIGH, disable clock
7:4	RO	0x0	reserved

Bit	Attr	Reset Value	Description
3	RW	0x0	hclk_iep_noc_en hclk_iep_noc clock disable bit When HIGH, disable clock Suggest always on
2	RW	0x0	hclk_iep_en hclk_iep clock disable bit When HIGH, disable clock
1	RW	0x0	aclk_iep_noc_en aclk_iep_noc clock disable bit When HIGH, disable clock Suggest always on
0	RW	0x0	aclk_iep_en aclk_iep clock disable bit When HIGH, disable clock

CRU_CLKGATE_CON17
Address: Operational Base + offset (0x0344)
Internal clock gating register17

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:12	RO	0x0	reserved
11	RW	0x0	hclk_vdu_noc_en hclk_vdu_noc clock disable bit When HIGH, disable clock Suggest always on
10	RW	0x0	hclk_vdu_en hclk_vdu clock disable bit When HIGH, disable clock
9	RW	0x0	aclk_vdu_noc_en aclk_vdu_noc clock disable bit When HIGH, disable clock Suggest always on
8	RW	0x0	aclk_vdu_en aclk_vdu clock disable bit When HIGH, disable clock
7:4	RO	0x0	reserved
3	RW	0x0	hclk_vcodec_noc_en hclk_vcodec_noc clock disable bit When HIGH, disable clock Suggest always on

Bit	Attr	Reset Value	Description
2	RW	0x0	hclk_vcodec_en hclk_vcodec clock disable bit When HIGH, disable clock
1	RW	0x0	aclk_vcodec_noc_en aclk_vcodec_noc clock disable bit When HIGH, disable clock Suggest always on
0	RW	0x0	aclk_vcodec_en aclk_vcodec clock disable bit When HIGH, disable clock

CRU_CLKGATE_CON18
Address: Operational Base + offset (0x0348)
Internal clock gating register18

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	pclk_cic_en pclk_cic clock disable bit When HIGH, disable clock
14	RW	0x0	clk_ddr_mon_timer_en clk_ddr_mon_timer clock disable bit When HIGH, disable clock
13	RW	0x0	clk_ddr_mon_en clk_ddr_mon clock disable bit When HIGH, disable clock
12	RW	0x0	pclk_ddr_mon_en pclk_ddr_mon clock disable bit When HIGH, disable clock
11	RW	0x0	clk_ddr_cic_en clk_ddr_cic clock disable bit When HIGH, disable clock
10	RW	0x0	pclk_center_main_noc_en pclk_center_main_noc clock disable bit When HIGH, disable clock Suggest always on
9	RW	0x0	clk_ddrcfg_msch1_en clk_ddrcfg_msch1 clock disable bit When HIGH, disable clock
8	RW	0x0	clk_ddrphy1_en clk_ddrphy1 clock disable bit When HIGH, disable clock

Bit	Attr	Reset Value	Description
7	RW	0x0	clk_ddrphy_ctrl1_en clk_ddrphy_ctrl1 clock disable bit When HIGH, disable clock
6	RW	0x0	clk_ddrc1_en clk_ddrc1 clock disable bit When HIGH, disable clock
5	RW	0x0	clk_ddr1_msch_en clk_ddr1_msch clock disable bit When HIGH, disable clock
4	RW	0x0	clk_ddrcfg_msch0_en clk_ddrcfg_msch0 clock disable bit When HIGH, disable clock
3	RW	0x0	clk_ddrphy0_en clk_ddrphy0 clock disable bit When HIGH, disable clock
2	RW	0x0	clk_ddrphy_ctrl0_en clk_ddrphy_ctrl0 clock disable bit When HIGH, disable clock
1	RW	0x0	clk_ddrc0_en clk_ddrc0 clock disable bit When HIGH, disable clock
0	RW	0x0	clk_ddr0_msch_en clk_ddr0_msch clock disable bit When HIGH, disable clock

CRU_CLKGATE_CON19

Address: Operational Base + offset (0x034c)

Internal clock gating register19

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:3	RO	0x0	reserved
2	RW	0x0	pclk_ddr_sgrf_en pclk_ddr_sgrf clock disable bit When HIGH, disable clock Suggest always on
1	RW	0x0	aclk_center_peri_noc_en aclk_center_peri_noc clock disable bit When HIGH, disable clock Suggest always on

Bit	Attr	Reset Value	Description
0	RW	0x0	aclk_center_main_noc_en aclk_center_main_noc clock disable bit When HIGH, disable clock Suggest always on

CRU_CLKGATE_CON20
Address: Operational Base + offset (0x0350)
Internal clock gating register20

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	hclk_ahb1tom_en hclk_ahb1tom clock disable bit When HIGH, disable clock
14	RW	0x0	pclk_perihp_noc_en pclk_perihp_noc clock disable bit When HIGH, disable clock Suggest always on
13	RW	0x0	hclk_perihp_noc_en hclk_perihp_noc clock disable bit When HIGH, disable clock Suggest always on
12	RW	0x0	aclk_perihp_noc_en aclk_perihp_noc clock disable bit When HIGH, disable clock Suggest always on
11	RW	0x0	pclk_pcie_en pclk_pcie clock disable bit When HIGH, disable clock
10	RW	0x0	aclk_pcie_en aclk_pcie clock disable bit When HIGH, disable clock
9	RW	0x0	hclk_hsic_en hclk_hsic clock disable bit When HIGH, disable clock
8	RW	0x0	hclk_host1_arb_en hclk_host1_arb clock disable bit When HIGH, disable clock
7	RW	0x0	hclk_host1_en hclk_host1 clock disable bit When HIGH, disable clock

Bit	Attr	Reset Value	Description
6	RW	0x0	hclk_host0_arb_en hclk_host0_arb clock disable bit When HIGH, disable clock
5	RW	0x0	hclk_host0_en hclk_host0 clock disable bit When HIGH, disable clock
4	RW	0x0	pclk_perihp_grf_en pclk_perihp_grf clock disable bit When HIGH, disable clock Suggest always on
3	RO	0x0	reserved
2	RW	0x0	aclk_perf_pcie_en aclk_perf_pcie clock disable bit When HIGH, disable clock
1:0	RO	0x0	reserved

CRU_CLKGATE_CON21
Address: Operational Base + offset (0x0354)
Internal clock gating register21

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:10	RO	0x0	reserved
9	RW	0x0	uphy1_pclk_tcpd_gate_en uphy1_pclk_tcpd disable bit When HIGH, disable clock
8	RW	0x0	uphy1_pclk_tcphy_gate_en uphy1_pclk_tcphy clock disable bit When HIGH, disable clock
7	RO	0x0	reserved
6	RW	0x0	uphy0_pclk_tcpd_gate_en uphy0_pclk_tcpd clock disable bit When HIGH, disable clock
5	RW	0x0	uphy0_pclk_tcphy_gate_en uphy0_pclk_tcphy clock disable bit When HIGH, disable clock
4	RW	0x0	uphy_pclk_mux_gate_en uphy_pclk_mux clock disable bit When HIGH, disable clock
3	RW	0x0	dphy_rx0_cfgclk_en dphy_rx0_cfg clock disable bit When HIGH, disable clock

Bit	Attr	Reset Value	Description
2	RW	0x0	dphy_tx1rx1_cfgclk_en dphy_tx1rx1_cfg clock disable bit When HIGH, disable clock
1	RW	0x0	dphy_tx0_cfgclk_en dphy_tx0_cfg clock disable bit When HIGH, disable clock
0	RW	0x0	dphy_pllclk_en dphy_pll clock disable bit When HIGH, disable clock

CRU_CLKGATE_CON22

Address: Operational Base + offset (0x0358)

Internal clock gating register22

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	pclk_efuse1024s_en pclk_efuse1024s clock disable bit When HIGH, disable clock
14	RW	0x0	pclk_efuse1024ns_en pclk_efuse1024ns clock disable bit When HIGH, disable clock
13	RW	0x0	pclk_tsadc_en pclk_tsadc clock disable bit When HIGH, disable clock
12	RW	0x0	pclk_saradc_en pclk_saradc clock disable bit When HIGH, disable clock
11	RW	0x0	pclk_mailbox0_en pclk_mailbox0 clock disable bit When HIGH, disable clock
10	RW	0x0	pclk_rki2c3_en pclk_rki2c3 clock disable bit When HIGH, disable clock
9	RW	0x0	pclk_rki2c2_en pclk_rki2c2 clock disable bit When HIGH, disable clock
8	RW	0x0	pclk_rki2c6_en pclk_rki2c6 clock disable bit When HIGH, disable clock
7	RW	0x0	pclk_rki2c5pad_en pclk_rki2c5pad clock disable bit When HIGH, disable clock

Bit	Attr	Reset Value	Description
6	RW	0x0	pclk_rki2c1cam_en pclk_rki2c1cam clock disable bit When HIGH, disable clock
5	RW	0x0	pclk_rki2c7_en pclk_rki2c7 clock disable bit When HIGH, disable clock
4	RO	0x0	reserved
3	RW	0x0	pclk_uart3_en pclk_uart3 clock disable bit When HIGH, disable clock
2	RW	0x0	pclk_uart2_en pclk_uart2 clock disable bit When HIGH, disable clock
1	RW	0x0	pclk_uart1_en pclk_uart1 clock disable bit When HIGH, disable clock
0	RW	0x0	pclk_uart0_en pclk_uart0 clock disable bit When HIGH, disable clock

CRU_CLKGATE_CON23
Address: Operational Base + offset (0x035c)
Internal clock gating register23

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RO	0x0	reserved
13	RW	0x0	pclk_spi4_en pclk_spi4 clock disable bit When HIGH, disable clock
12	RW	0x0	pclk_spi2_en pclk_spi2 clock disable bit When HIGH, disable clock
11	RW	0x0	pclk_spi1_en pclk_spi1 clock disable bit When HIGH, disable clock
10	RW	0x0	pclk_spi0codec_en pclk_spi0codec clock disable bit When HIGH, disable clock
9	RW	0x0	pclk_dcf_en pclk_dcf clock disable bit When HIGH, disable clock

Bit	Attr	Reset Value	Description
8	RW	0x0	aclk_dcf_en aclk_dcf clock disable bit When HIGH, disable clock
7	RW	0x0	clk_intmem5_en clk_intmem5 clock disable bit When HIGH, disable clock
6	RW	0x0	clk_intmem4_en clk_intmem4 clock disable bit When HIGH, disable clock
5	RW	0x0	clk_intmem3_en clk_intmem3 clock disable bit When HIGH, disable clock
4	RW	0x0	clk_intmem2_en clk_intmem2 clock disable bit When HIGH, disable clock
3	RW	0x0	clk_intmem1_en clk_intmem1 clock disable bit When HIGH, disable clock
2	RW	0x0	clk_intmem0_en clk_intmem0 clock disable bit When HIGH, disable clock
1	RW	0x0	aclk_tzma_en aclk_tzma clock disable bit When HIGH, disable clock
0	RW	0x0	aclk_intmem_en aclk_intmem clock disable bit When HIGH, disable clock

CRU_CLKGATE_CON24

Address: Operational Base + offset (0x0360)

Internal clock gating register24

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	hclk_s_crypto1_en hclk_s_crypto1 clock disable bit When HIGH, disable clock
14	RW	0x0	hclk_m_crypto1_en hclk_m_crypto1 clock disable bit When HIGH, disable clock

Bit	Attr	Reset Value	Description
13	RW	0x0	pclk_perilp_sgrf_en pclk_perilp_sgrf clock disable bit When HIGH, disable clock Suggest always on
12	RO	0x0	reserved
11	RW	0x0	clk_m0_perilp_dec_en clk_m0_perilp_dec clock disable bit When HIGH, disable clock
10	RW	0x0	dclk_m0_perilp_en dclk_m0_perilp clock disable bit When HIGH, disable clock
9	RW	0x0	hclk_m0_perilp_en hclk_m0_perilp clock disable bit When HIGH, disable clock
8	RW	0x0	sclk_m0_perilp_en sclk_m0_perilp clock disable bit When HIGH, disable clock
7	RO	0x0	reserved
6	RW	0x0	hclk_s_crypto0_en hclk_s_crypto0 clock disable bit When HIGH, disable clock
5	RW	0x0	hclk_m_crypto0_en hclk_m_crypto0 clock disable bit When HIGH, disable clock
4	RW	0x0	hclk_rom_en hclk_rom clock disable bit When HIGH, disable clock
3:0	RO	0x0	reserved

CRU_CLKGATE_CON25

Address: Operational Base + offset (0x0364)

Internal clock gating register25

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:13	RO	0x0	reserved
12	RW	0x0	hclk_sdio_noc_en hclk_sdio_noc clock disable bit When HIGH, disable clock Suggest always on

Bit	Attr	Reset Value	Description
11	RW	0x0	hclk_m0_perilp_noc_en hclk_m0_perilp_noc clock disable bit When HIGH, disable clock Suggest always on
10	RW	0x0	pclk_perilp1_noc_en pclk_perilp1_noc clock disable bit When HIGH, disable clock Suggest always on
9	RW	0x0	hclk_perilp1_noc_en hclk_perilp1_noc clock disable bit When HIGH, disable clock Suggest always on
8	RW	0x0	hclk_perilp0_noc_en hclk_perilp0_noc clock disable bit When HIGH, disable clock Suggest always on
7	RW	0x0	aclk_perilp0_noc_en aclk_perilp0_noc clock disable bit When HIGH, disable clock Suggest always on
6	RW	0x0	aclk_dmac1_perilp_en aclk_dmac1_perilp clock disable bit When HIGH, disable clock
5	RW	0x0	aclk_dmac0_perilp_en aclk_dmac0_perilp clock disable bit When HIGH, disable clock
4:0	RO	0x0	reserved

CRU_CLKGATE_CON26
Address: Operational Base + offset (0x0368)
Internal clock gating register26

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:12	RO	0x0	reserved
11	RW	0x0	clk_timer11_en clk_timer11 clock disable bit When HIGH, disable clock
10	RW	0x0	clk_timer10_en clk_timer10 clock disable bit When HIGH, disable clock

Bit	Attr	Reset Value	Description
9	RW	0x0	clk_timer9_en clk_timer9 clock disable bit When HIGH, disable clock
8	RW	0x0	clk_timer8_en clk_timer8 clock disable bit When HIGH, disable clock
7	RW	0x0	clk_timer7_en clk_timer7 clock disable bit When HIGH, disable clock
6	RW	0x0	clk_timer6_en clk_timer6 clock disable bit When HIGH, disable clock
5	RW	0x0	clk_timer5_en clk_timer5 clock disable bit When HIGH, disable clock
4	RW	0x0	clk_timer4_en clk_timer4 clock disable bit When HIGH, disable clock
3	RW	0x0	clk_timer3_en clk_timer3 clock disable bit When HIGH, disable clock
2	RW	0x0	clk_timer2_en clk_timer2 clock disable bit When HIGH, disable clock
1	RW	0x0	clk_timer1_en clk_timer1 clock disable bit When HIGH, disable clock
0	RW	0x0	clk_timer0_en clk_timer0 clock disable bit When HIGH, disable clock

CRU_CLKGATE_CON27

Address: Operational Base + offset (0x036c)

Internal clock gating register27

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:9	RO	0x0	reserved
8	RW	0x0	aclk_isp1_wrapper_en aclk_isp1_wrapper clock disable bit When HIGH, disable clock

Bit	Attr	Reset Value	Description
7	RW	0x0	hclk_isp1_wrapper_en hclk_isp1_wrapper clock disable bit When HIGH, disable clock
6	RW	0x0	pclkin_isp1_wrapper_en pclkin_isp1_wrapper clock disable bit When HIGH, disable clock
5	RW	0x0	aclk_isp0_wrapper_en aclk_isp0_wrapper clock disable bit When HIGH, disable clock
4	RW	0x0	hclk_isp0_wrapper_en hclk_isp0_wrapper clock disable bit When HIGH, disable clock
3	RW	0x0	aclk_isp1_noc_en aclk_isp1_noc clock disable bit When HIGH, disable clock Suggest always on
2	RW	0x0	hclk_isp1_noc_en hclk_isp1_noc clock disable bit When HIGH, disable clock Suggest always on
1	RW	0x0	aclk_isp0_noc_en aclk_isp0_noc clock disable bit When HIGH, disable clock Suggest always on
0	RW	0x0	hclk_isp0_noc_en hclk_isp0_noc clock disable bit When HIGH, disable clock Suggest always on

CRU_CLKGATE_CON28
Address: Operational Base + offset (0x0370)
Internal clock gating register28

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:8	RO	0x0	reserved
7	RW	0x0	aclk_vopb_en aclk_vopb clock disable bit When HIGH, disable clock
6	RW	0x0	hclk_vopb_en hclk_vopb clock disable bit When HIGH, disable clock

Bit	Attr	Reset Value	Description
5	RW	0x0	aclk_vopb_noc_en aclk_vopb_noc clock disable bit When HIGH, disable clock Suggest always on
4	RW	0x0	hclk_vopb_noc_en hclk_vopb_noc clock disable bit When HIGH, disable clock Suggest always on
3	RW	0x0	aclk_vop0_en aclk_vop0 clock disable bit When HIGH, disable clock
2	RW	0x0	hclk_vop0_en hclk_vop0 clock disable bit When HIGH, disable clock
1	RW	0x0	aclk_vop0_noc_en aclk_vop0_noc clock disable bit When HIGH, disable clock Suggest always on
0	RW	0x0	hclk_vop0_noc_en hclk_vop0_noc clock disable bit When HIGH, disable clock Suggest always on

CRU_CLKGATE_CON29
Address: Operational Base + offset (0x0374)
Internal clock gating register29

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:13	RO	0x0	reserved
12	RW	0x0	pclk_vio_grf_en pclk_vio_grf clock disable bit When HIGH, disable clock Suggest always on
11	RW	0x0	pclk_gasket_en pclk_gasket clock disable bit When HIGH, disable clock
10	RW	0x0	aclk_hdcp22_en aclk_hdcp22 clock disable bit When HIGH, disable clock
9	RW	0x0	hclk_hdcp22_en hclk_hdcp22 clock disable bit When HIGH, disable clock

Bit	Attr	Reset Value	Description
8	RW	0x0	pclk_hdcp22_en pclk_hdcp22 clock disable bit When HIGH, disable clock
7	RW	0x0	pclk_dp_ctrl_en pclk_dp_ctrl clock disable bit When HIGH, disable clock
6	RW	0x0	pclk_hdmi_ctrl_en pclk_hdmi_ctrl clock disable bit When HIGH, disable clock
5	RW	0x0	hclk_hdcpnoc_en hclk_hdcpnoc clock disable bit When HIGH, disable clock Suggest always on
4	RW	0x0	aclk_hdcpnoc_en aclk_hdcpnoc clock disable bit When HIGH, disable clock Suggest always on
3	RW	0x0	pclk_hdcpnoc_en pclk_hdcpnoc clock disable bit When HIGH, disable clock Suggest always on
2	RW	0x0	pclk_mipi_dsi1_en pclk_mipi_dsi1 clock disable bit When HIGH, disable clock
1	RW	0x0	pclk_mipi_dsi0_en pclk_mipi_dsi0 clock disable bit When HIGH, disable clock
0	RW	0x0	aclk_vio_noc_en aclk_vio_noc clock disable bit When HIGH, disable clock Suggest always on

CRU_CLKGATE_CON30
Address: Operational Base + offset (0x0378)
Internal clock gating register30

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:12	RO	0x0	reserved
11	RW	0x0	aclk_gpu_grf_en aclk_gpu_grf clock disable bit When HIGH, disable clock Suggest always on

Bit	Attr	Reset Value	Description
10	RW	0x0	aclk_perf_gpu_en aclk_perf_gpu clock disable bit When HIGH, disable clock
9	RO	0x0	reserved
8	RW	0x0	aclk_gpu_en aclk_gpu clock disable bit When HIGH, disable clock
7:5	RO	0x0	reserved
4	RW	0x0	aclk_usb3_grf_en aclk_usb3_grf clock disable bit When HIGH, disable clock Suggest always on
3	RW	0x0	aclk_usb3_rksoc_axi_perf_en aclk_usb3_rksoc_axi_perf clock disable bit When HIGH, disable clock
2	RW	0x0	aclk_usb3otg1_en aclk_usb3otg1 clock disable bit When HIGH, disable clock
1	RW	0x0	aclk_usb3otg0_en aclk_usb3otg0 clock disable bit When HIGH, disable clock
0	RW	0x0	aclk_usb3_noc_en aclk_usb3_noc clock disable bit When HIGH, disable clock Suggest always on

CRU_CLKGATE_CON31

Address: Operational Base + offset (0x037c)

Internal clock gating register31

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:11	RO	0x0	reserved
10	RW	0x0	pclk_sgrf_en pclk_sgrf clock disable bit When HIGH, disable clock Suggest always on
9	RW	0x0	pclk_pmu_intr_arb_en pclk_pmu_intr_arb clock disable bit When HIGH, disable clock
8	RW	0x0	pclk_hsicphy_en pclk_hsicphy clock disable bit When HIGH, disable clock

Bit	Attr	Reset Value	Description
7	RW	0x0	pclk_timer1_en pclk_timer1 clock disable bit When HIGH, disable clock
6	RW	0x0	pclk_timer0_en pclk_timer0 clock disable bit When HIGH, disable clock
5	RW	0x0	pclk_gpio4_en pclk_gpio4 clock disable bit When HIGH, disable clock
4	RW	0x0	pclk_gpio3_en pclk_gpio3 clock disable bit When HIGH, disable clock
3	RW	0x0	pclk_gpio2_en pclk_gpio2 clock disable bit When HIGH, disable clock
2	RW	0x0	pclk_intr_arb_en pclk_intr_arb clock disable bit When HIGH, disable clock
1	RW	0x0	pclk_grf_en pclk_grf clock disable bit When HIGH, disable clock Suggest always on
0	RO	0x0	reserved

CRU_CLKGATE_CON32

Address: Operational Base + offset (0x0380)

Internal clock gating register32

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RO	0x0	reserved
13	RW	0x0	pclk_edp_ctrl_en pclk_edp_ctrl clock disable bit When HIGH, disable clock
12	RW	0x0	pclk_edp_noc_en pclk_edp_noc clock disable bit When HIGH, disable clock Suggest always on
11	RO	0x0	reserved
10	RW	0x0	aclk_emmc_grf_en aclk_emmc_grf clock disable bit When HIGH, disable clock Suggest always on

Bit	Attr	Reset Value	Description
9	RW	0x0	aclk_emmc_noc_en aclk_emmc_noc clock disable bit When HIGH, disable clock Suggest always on
8	RW	0x0	aclk_emmc_core_en aclk_emmc_core clock disable bit When HIGH, disable clock
7:5	RO	0x0	reserved
4	RW	0x0	aclk_perf_gmac_en aclk_perf_gmac clock disable bit When HIGH, disable clock
3	RW	0x0	pclk_gmac_noc_en pclk_gmac_noc clock disable bit When HIGH, disable clock Suggest always on
2	RW	0x0	pclk_gmac_en pclk_gmac clock disable bit When HIGH, disable clock
1	RW	0x0	aclk_gmac_noc_en aclk_gmac_noc clock disable bit When HIGH, disable clock Suggest always on
0	RW	0x0	aclk_gmac_en aclk_gmac clock disable bit When HIGH, disable clock

CRU_CLKGATE_CON33
Address: Operational Base + offset (0x0384)
Internal clock gating register33

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:10	RO	0x0	reserved
9	RW	0x0	hclk_sd_noc_en hclk_sd_noc clock disable bit When HIGH, disable clock Suggest always on
8	RW	0x0	hclk_sdmmc_en hclk_sdmmc clock disable bit When HIGH, disable clock
7:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5	RW	0x0	aclk_gic_adb400_gic_2_core_b_en aclk_gic_adb400_gic_2_core_b clock disable bit When HIGH, disable clock
4	RW	0x0	aclk_gic_adb400_gic_2_core_l_en aclk_gic_adb400_gic_2_core_l clock disable bit When HIGH, disable clock
3	RW	0x0	aclk_gic_adb400_core_b_2_gic_en aclk_gic_adb400_core_b_2_gic clock disable bit When HIGH, disable clock
2	RW	0x0	aclk_gic_adb400_core_l_2_gic_en aclk_gic_adb400_core_l_2_gic clock disable bit When HIGH, disable clock
1	RW	0x0	aclk_gic_noc_en aclk_gic_noc clock disable bit When HIGH, disable clock Suggest always on
0	RW	0x0	aclk_gic_en aclk_gic clock disable bit When HIGH, disable clock

CRU_CLKGATE_CON34
Address: Operational Base + offset (0x0388)
Internal clock gating register34

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:7	RO	0x0	reserved
6	RW	0x0	hclk_sdioaudio_noc_en hclk_sdioaudio_noc clock disable bit When HIGH, disable clock Suggest always on
5	RW	0x0	pclk_spi5_en pclk_spi5 clock disable bit When HIGH, disable clock
4	RW	0x0	hclk_sdio_en hclk_sdio clock disable bit When HIGH, disable clock
3	RW	0x0	hclk_spdif_en hclk_spdif clock disable bit When HIGH, disable clock
2	RW	0x0	hclk_i2s2_en hclk_i2s2 clock disable bit When HIGH, disable clock

Bit	Attr	Reset Value	Description
1	RW	0x0	hclk_i2s1_en hclk_i2s1 clock disable bit When HIGH, disable clock
0	RW	0x0	hclk_i2s0_en hclk_i2s0 clock disable bit When HIGH, disable clock

CRU_SOFTRST_CON0
Address: Operational Base + offset (0x0400)
Internal software reset control register0

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:12	RO	0x0	reserved
11	R/W SC	0x0	resetn_dbg_noc_req resetn_dbg_noc request bit When HIGH, reset relative logic
10	R/W SC	0x0	aresetn_ccim1_noc_req aresetn_ccim1_noc request bit When HIGH, reset relative logic
9	R/W SC	0x0	aresetn_ccim0_noc_req aresetn_ccim0_noc request bit When HIGH, reset relative logic
8	R/W SC	0x0	aresetn_cci_req aresetn_cci request bit When HIGH, reset relative logic
7	R/W SC	0x0	adb_b_srstn_req adb_b_srstn request bit When HIGH, reset relative logic
6	R/W SC	0x0	adb_l_srstn_req adb_l_srstn request bit When HIGH, reset relative logic
5	R/W SC	0x0	l2_b_srstn_req l2_b_srstn request bit When HIGH, reset relative logic
4	R/W SC	0x0	l2_l_srstn_req l2_l_srstn request bit When HIGH, reset relative logic
3	R/W SC	0x0	corepo0_b_srstn_req corepo0_b_srstn request bit When HIGH, reset relative logic

Bit	Attr	Reset Value	Description
2	R/W SC	0x0	corepo0_l_srstn_req corepo0_l_srstn request bit When HIGH, reset relative logic
1	R/W SC	0x0	core0_b_srstn_req core0_b_srstn request bit When HIGH, reset relative logic
0	R/W SC	0x0	core0_l_srstn_req core0_l_srstn request bit When HIGH, reset relative logic

CRU_SOFTRST_CON1

Address: Operational Base + offset (0x0404)

Internal software reset control register1

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	pvtm_core_l_srstn_req pvtm_core_l_srstn request bit When HIGH, reset relative logic
14	RW	0x0	rkperf_l_arstn_req rkperf_l_arstn request bit When HIGH, reset relative logic
13	RW	0x0	adb_l_srstn_req_t adb_l_srstn request bit When HIGH, reset relative logic
12	RW	0x0	l2_l_srstn_req_t l2_l_srstn request bit When HIGH, reset relative logic
11	RO	0x0	reserved
10	RW	0x0	prstn_dbg_l_req prstn_dbg_l request bit When HIGH, reset relative logic
9	RW	0x0	arstn_adb400_corel2gic_req arstn_adb400_corel2gic request bit When HIGH, reset relative logic
8	RW	0x0	arstn_adb400_gic2corel_req arstn_adb400_gic2corel request bit When HIGH, reset relative logic
7	RW	0x0	corepo3_l_srstn_req corepo3_l_srstn request bit When HIGH, reset relative logic

Bit	Attr	Reset Value	Description
6	RW	0x0	corepo2_l_srstn_req corepo2_l_srstn request bit When HIGH, reset relative logic
5	RW	0x0	corepo1_l_srstn_req corepo1_l_srstn request bit When HIGH, reset relative logic
4	RW	0x0	corepo0_l_srstn_req_t corepo0_l_srstn request bit When HIGH, reset relative logic
3	RW	0x0	core3_l_srstn_req core3_l_srstn request bit When HIGH, reset relative logic
2	RW	0x0	core2_l_srstn_req core2_l_srstn request bit When HIGH, reset relative logic
1	RW	0x0	core1_l_srstn_req core1_l_srstn request bit When HIGH, reset relative logic
0	RW	0x0	core0_l_srstn_req_t core0_l_srstn request bit When HIGH, reset relative logic

CRU_SOFTRST_CON2
Address: Operational Base + offset (0x0408)
Internal software reset control register2

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	pvtm_core_b_srstn_req pvtm_core_b_srstn request bit When HIGH, reset relative logic
14	RW	0x0	rkperf_b_arstn_req rkperf_b_arstn request bit When HIGH, reset relative logic
13	RW	0x0	adb_b_srstn_req_t adb_b_srstn request bit When HIGH, reset relative logic
12	RW	0x0	l2_b_srstn_req_t l2_b_srstn request bit When HIGH, reset relative logic
11	RO	0x0	reserved

Bit	Attr	Reset Value	Description
10	RW	0x0	prstn_dbg_b_req prstn_dbg_b request bit When HIGH, reset relative logic
9	RW	0x0	arstn_adb400_coreb2gic_req arstn_adb400_coreb2gic request bit When HIGH, reset relative logic
8	RW	0x0	arstn_adb400_gic2coreb_req arstn_adb400_gic2coreb request bit When HIGH, reset relative logic
7:6	RO	0x0	reserved
5	RW	0x0	corepo1_b_srstn_req corepo1_b_srstn request bit When HIGH, reset relative logic
4	RW	0x0	corepo0_b_srstn_req_t corepo0_b_srstn request bit When HIGH, reset relative logic
3:2	RO	0x0	reserved
1	RW	0x0	core1_b_srstn_req core1_b_srstn request bit When HIGH, reset relative logic
0	RW	0x0	core0_b_srstn_req_t core0_b_srstn request bit When HIGH, reset relative logic

CRU_SOFTRST_CON3

Address: Operational Base + offset (0x040c)

Internal software reset control register3

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:11	RO	0x0	reserved
10	RW	0x0	presetn_cci_grf_req presetn_cci_grf request bit When HIGH, reset relative logic
9	RW	0x0	resetn_cci_trace_req resetn_cci_trace request bit When HIGH, reset relative logic
8	RW	0x0	resetn_dbg_cxcs_req resetn_dbg_cxcs request bit When HIGH, reset relative logic
7	RW	0x0	resetn_dbg_noc_req_t resetn_dbg_noc request bit When HIGH, reset relative logic

Bit	Attr	Reset Value	Description
6	RW	0x0	aresetn_adb400m_pd_core_l_req_t aresetn_adb400m_pd_core_l request bit When HIGH, reset relative logic
5	RW	0x0	aresetn_adb400m_pd_core_b_req_t aresetn_adb400m_pd_core_b request bit When HIGH, reset relative logic
4	RO	0x1	aresetn_ccim1_noc_req_t aresetn_ccim1_noc request bit When HIGH, reset relative logic
3	RW	0x0	aresetn_ccim0_noc_req_t aresetn_ccim0_noc request bit When HIGH, reset relative logic
2	RW	0x0	aresetn_cci_req_t aresetn_cci request bit When HIGH, reset relative logic
1:0	RO	0x0	reserved

CRU_SOFTRST_CON4
Address: Operational Base + offset (0x0410)
Internal software reset control register4

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	resetn_pvtm_ddr_req resetn_pvtm_ddr request bit When HIGH, reset relative logic
14	RW	0x0	resetn_ddr_cic_req resetn_ddr_cic request bit When HIGH, reset relative logic
13	RW	0x0	resetn_ddrphy1_req resetn_ddrphy1 request bit When HIGH, reset relative logic
12	RW	0x0	resetn_ddr1_req resetn_ddr1 request bit When HIGH, reset relative logic
11	RW	0x0	resetn_ddrcfg1_msch_req resetn_ddrcfg1_msch request bit When HIGH, reset relative logic
10	RW	0x0	resetn_ddr1_msch_req resetn_ddr1_msch request bit When HIGH, reset relative logic

Bit	Attr	Reset Value	Description
9	RW	0x0	resetn_ddrphy0_req resetn_ddrphy0 request bit When HIGH, reset relative logic
8	RW	0x0	resetn_ddr0_req resetn_ddr0 request bit When HIGH, reset relative logic
7	RW	0x0	resetn_ddrcfg0_msch_req resetn_ddrcfg0_msch request bit When HIGH, reset relative logic
6	RW	0x0	resetn_ddr0_msch_req resetn_ddr0_msch request bit When HIGH, reset relative logic
5	RW	0x0	presetn_center_sgrf_req presetn_center_sgrf request bit When HIGH, reset relative logic
4	RW	0x0	presetn_cic_req presetn_cic request bit When HIGH, reset relative logic
3	RW	0x0	presetn_ddrmon_req presetn_ddrmon request bit When HIGH, reset relative logic
2	RW	0x0	presetn_center_main_req presetn_center_main request bit When HIGH, reset relative logic
1	RW	0x0	aresetn_center_peri_noc_req aresetn_center_peri_noc request bit When HIGH, reset relative logic
0	RW	0x0	aresetn_center_main_noc_req aresetn_center_main_noc request bit When HIGH, reset relative logic

CRU_SOFTRST_CON5

Address: Operational Base + offset (0x0414)

Internal software reset control register5

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RO	0x0	reserved
13	RW	0x0	resetn_vdu_ca_req resetn_vdu_ca request bit When HIGH, reset relative logic

Bit	Attr	Reset Value	Description
12	RW	0x0	resetn_vdu_core_req resetn_vdu_core request bit When HIGH, reset relative logic
11	RW	0x0	hresetn_vdu_req hresetn_vdu request bit When HIGH, reset relative logic
10	RW	0x0	hresetn_vdu_noc_req hresetn_vdu_noc request bit When HIGH, reset relative logic
9	RW	0x0	aresetn_vdu_req aresetn_vdu request bit When HIGH, reset relative logic
8	RW	0x0	aresetn_vdu_noc_req aresetn_vdu_noc request bit When HIGH, reset relative logic
7:4	RO	0x0	reserved
3	RW	0x0	hresetn_vcodec_req hresetn_vcodec request bit When HIGH, reset relative logic
2	RW	0x0	hresetn_vcodec_noc_req hresetn_vcodec_noc request bit When HIGH, reset relative logic
1	RW	0x0	aresetn_vcodec_req aresetn_vcodec request bit When HIGH, reset relative logic
0	RW	0x0	aresetn_vcodec_noc_req aresetn_vcodec_noc request bit When HIGH, reset relative logic

CRU_SOFTRST_CON6

Address: Operational Base + offset (0x0418)

Internal software reset control register6

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14	RW	0x0	aresetn_emmc_grf_req aresetn_emmc_grf request bit When HIGH, reset relative logic
13	RW	0x0	aresetn_emmc_req aresetn_emmc request bit When HIGH, reset relative logic

Bit	Attr	Reset Value	Description
12	RW	0x0	aresetn_emmc_noc_req aresetn_emmc_noc request bit When HIGH, reset relative logic
11	RO	0x0	reserved
10	RW	0x0	resetn_rga_core_req resetn_rga_core request bit When HIGH, reset relative logic
9	RW	0x0	hresetn_rga_req hresetn_rga request bit When HIGH, reset relative logic
8	RW	0x0	hresetn_rga_noc_req hresetn_rga_noc request bit When HIGH, reset relative logic
7	RW	0x0	aresetn_rga_req aresetn_rga request bit When HIGH, reset relative logic
6	RW	0x0	aresetn_rga_noc_req aresetn_rga_noc request bit When HIGH, reset relative logic
5	RO	0x0	reserved
4	RW	0x0	hresetn_iep_req hresetn_iep request bit When HIGH, reset relative logic
3	RW	0x0	hresetn_iep_noc_req hresetn_iep_noc request bit When HIGH, reset relative logic
2	RW	0x0	aresetn_iep_req aresetn_iep request bit When HIGH, reset relative logic
1	RW	0x0	aresetn_vop_iep_req aresetn_vop_iep request bit When HIGH, reset relative logic
0	RW	0x0	aresetn_iep_noc_req aresetn_iep_noc request bit When HIGH, reset relative logic

CRU_SOFTRST_CON7

Address: Operational Base + offset (0x041c)

Internal software reset control register7

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit

Bit	Attr	Reset Value	Description
15	RW	0x0	presetn_hsicphy_req presetn_hsicphy request bit When HIGH, reset relative logic
14	RW	0x0	presetn_perihp_noc_req presetn_perihp_noc request bit When HIGH, reset relative logic
13	RW	0x0	hresetn_ahb1tom_req hresetn_ahb1tom request bit When HIGH, reset relative logic
12	RW	0x0	hresetn_hsic_aux_req hresetn_hsic_aux request bit When HIGH, reset relative logic
11	RW	0x0	hresetn_hsic_req hresetn_hsic request bit When HIGH, reset relative logic
10	RW	0x0	hresetn_sdmmc_req hresetn_sdmmc request bit When HIGH, reset relative logic
9	RW	0x0	hresetn_sdio0_req hresetn_sdio0 request bit When HIGH, reset relative logic
8	RW	0x0	hresetn_host1_arb_req hresetn_host1_arb request bit When HIGH, reset relative logic
7	RW	0x0	hresetn_hostc1_aux_req hresetn_hostc1_aux request bit When HIGH, reset relative logic
6	RW	0x0	hresetn_usbhost1_req hresetn_usbhost1 request bit When HIGH, reset relative logic
5	RW	0x0	hresetn_host0_arb_req hresetn_host0_arb request bit When HIGH, reset relative logic
4	RW	0x0	hresetn_hostc0_aux_req hresetn_hostc0_aux request bit When HIGH, reset relative logic
3	RW	0x0	hresetn_usbhost0_req hresetn_usbhost0 request bit When HIGH, reset relative logic
2	RW	0x0	hresetn_perihp_noc_req hresetn_perihp_noc request bit When HIGH, reset relative logic
1	RW	0x0	presetn_perihp_grf_req presetn_perihp_grf request bit When HIGH, reset relative logic

Bit	Attr	Reset Value	Description
0	RW	0x0	aresetn_perihp_noc_req aresetn_perihp_noc request bit When HIGH, reset relative logic

CRU_SOFTRST_CON8
Address: Operational Base + offset (0x0420)
Internal software reset control register8

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	hsicphy_utmi_rstn_req hsicphy_utmi_rstn request bit When HIGH, reset relative logic
14	RW	0x0	hsicphy_por_rstn_req hsicphy_por_rstn request bit When HIGH, reset relative logic
13	RO	0x0	reserved
12	RW	0x0	presetn_gmac_grf_req presetn_gmac_grf request bit When HIGH, reset relative logic
11	RO	0x0	reserved
10	RW	0x0	presetn_gmac_noc_req presetn_gmac_noc request bit When HIGH, reset relative logic
9	RW	0x0	aresetn_gmac_req aresetn_gmac request bit When HIGH, reset relative logic
8	RW	0x0	aresetn_gmac_noc_req aresetn_gmac_noc request bit When HIGH, reset relative logic
7	RW	0x1	resetn_pciephy_req resetn_pciephy request bit When HIGH, reset relative logic
6	RW	0x0	resetn_pcie_pm_req resetn_pcie_pm request bit When HIGH, reset relative logic
5	RW	0x1	resetn_pcie_pipe_req resetn_pcie_pipe request bit When HIGH, reset relative logic
4	RW	0x1	resetn_pcie_mgmt_sticky_req resetn_pcie_mgmt_sticky request bit When HIGH, reset relative logic

Bit	Attr	Reset Value	Description
3	RW	0x1	resetn_pcie_mgmt_req resetn_pcie_mgmt request bit When HIGH, reset relative logic
2	RW	0x1	resetn_pcie_core_req resetn_pcie_core request bit When HIGH, reset relative logic
1	RW	0x0	presetn_pcie_req presetn_pcie request bit When HIGH, reset relative logic
0	RW	0x0	aresetn_pcie_req aresetn_pcie request bit When HIGH, reset relative logic

CRU_SOFTRST_CON9

Address: Operational Base + offset (0x0424)

Internal software reset control register9

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved
14	RW	0x0	resetn_uphy1_tcpdpwrup_req resetn_uphy1_tcpdpwrup request bit When HIGH, reset relative logic
13	RW	0x0	resetn_uphy1_req resetn_uphy1 request bit When HIGH, reset relative logic
12	RW	0x0	resetn_uphy1_pipe_l00_req resetn_uphy1_pipe_l00 request bit When HIGH, reset relative logic
11	RW	0x0	resetn_usb2phy1_ehciphy_req resetn_usb2phy1_ehciphy request bit When HIGH, reset relative logic
10	RW	0x0	resetn_usb2phy1_utmi_port1_req resetn_usb2phy1_utmi_port1 request bit When HIGH, reset relative logic
9	RW	0x0	resetn_usb2phy1_utmi_port0_req resetn_usb2phy1_utmi_port0 request bit When HIGH, reset relative logic
8	RW	0x0	resetn_usb2phy1_por_req resetn_usb2phy1_por request bit When HIGH, reset relative logic
7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6	RW	0x0	resetn_uphy0_tcpdpwrup_req resetn_uphy0_tcpdpwrup request bit When HIGH, reset relative logic
5	RW	0x0	resetn_uphy0_req resetn_uphy0 request bit When HIGH, reset relative logic
4	RW	0x0	resetn_uphy0_pipe_l00_req resetn_uphy0_pipe_l00 request bit When HIGH, reset relative logic
3	RW	0x0	resetn_usb2phy0_ehciphy_req resetn_usb2phy0_ehciphy request bit When HIGH, reset relative logic
2	RW	0x0	resetn_usb2phy0_utmi_port1_req resetn_usb2phy0_utmi_port1 request bit When HIGH, reset relative logic
1	RW	0x0	resetn_usb2phy0_utmi_port0_req resetn_usb2phy0_utmi_port0 request bit When HIGH, reset relative logic
0	RW	0x0	resetn_usb2phy0_por_req resetn_usb2phy0_por request bit When HIGH, reset relative logic

CRU_SOFTRST_CON10

Address: Operational Base + offset (0x0428)

Internal software reset control register10

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	hresetn_crypto0_m_req hresetn_crypto0_m request bit When HIGH, reset relative logic
14	RW	0x0	hresetn_crypto0_s_req hresetn_crypto0_s request bit When HIGH, reset relative logic
13	RW	0x0	hresetn_rom_req hresetn_rom request bit When HIGH, reset relative logic
12	RW	0x0	hresetn_perilp0_noc_req hresetn_perilp0_noc request bit When HIGH, reset relative logic
11	RW	0x0	hresetn_perilp0_req hresetn_perilp0 request bit When HIGH, reset relative logic

Bit	Attr	Reset Value	Description
10	RW	0x0	aresetn_adb400_slv1_req aresetn_adb400_slv1 request bit When HIGH, reset relative logic
9	RW	0x0	aresetn_adb400_slv0_req aresetn_adb400_slv0 request bit When HIGH, reset relative logic
8	RW	0x0	aresetn_adb400_mst1_req aresetn_adb400_mst1 request bit When HIGH, reset relative logic
7	RW	0x0	aresetn_adb400_mst0_req aresetn_adb400_mst0 request bit When HIGH, reset relative logic
6	RW	0x0	aresetn_intmem_req aresetn_intmem request bit When HIGH, reset relative logic
5	RW	0x0	aresetn_tzma_req aresetn_tzma request bit When HIGH, reset relative logic
4	RW	0x0	aresetn_dmac1_perilp0_req aresetn_dmac1_perilp0 request bit When HIGH, reset relative logic
3	RW	0x0	aresetn_dmac0_perilp0_req aresetn_dmac0_perilp0 request bit When HIGH, reset relative logic
2	RW	0x0	aresetn_gic500_req aresetn_gic500 request bit When HIGH, reset relative logic
1	RW	0x0	aresetn_dcf_req aresetn_dcf request bit When HIGH, reset relative logic
0	RW	0x0	aresetn_perilp0_noc_req aresetn_perilp0_noc request bit When HIGH, reset relative logic

CRU_SOFTRST_CON11

Address: Operational Base + offset (0x042c)

Internal software reset control register11

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved

Bit	Attr	Reset Value	Description
14	RW	0x0	hresetn_sdioaudio_brg_req hresetn_sdioaudio_brg request bit When HIGH, reset relative logic
13	RW	0x0	hresetn_sd_noc_req hresetn_sd_noc request bit When HIGH, reset relative logic
12	RW	0x0	aresetn_gic_noc_req aresetn_gic_noc request bit When HIGH, reset relative logic
11	RO	0x0	reserved
10	RW	0x0	resetn_crypto1_req resetn_crypto1 request bit When HIGH, reset relative logic
9	RW	0x0	hresetn_crypto1_m_req hresetn_crypto1_m request bit When HIGH, reset relative logic
8	RW	0x0	hresetn_crypto1_s_req hresetn_crypto1_s request bit When HIGH, reset relative logic
7	RW	0x0	presetn_perilp1_grf_req presetn_perilp1_grf request bit When HIGH, reset relative logic
6	RW	0x0	presetn_perilp1_sgrf_req presetn_perilp1_sgrf request bit When HIGH, reset relative logic
5	RW	0x0	resetn_crypto0_req resetn_crypto0 request bit When HIGH, reset relative logic
4	RW	0x1	poresetn_cm0s_req poresetn_cm0s request bit When HIGH, reset relative logic
3	RW	0x0	dbgresetn_cm0s_req dbgresetn_cm0s request bit When HIGH, reset relative logic
2	RW	0x1	hresetn_cm0s_req hresetn_cm0s request bit When HIGH, reset relative logic
1	RW	0x0	hresetn_cm0s_noc_req hresetn_cm0s_noc request bit When HIGH, reset relative logic
0	RW	0x0	presetn_dcf_req presetn_dcf request bit When HIGH, reset relative logic

CRU_SOFTRST_CON12

Address: Operational Base + offset (0x0430)
Internal software reset control register12

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	presetn_mailbox0_req presetn_mailbox0 request bit When HIGH, reset relative logic
14	RW	0x0	presetn_i2c7_req presetn_i2c7 request bit When HIGH, reset relative logic
13	RW	0x0	presetn_i2c3_req presetn_i2c3 request bit When HIGH, reset relative logic
12	RW	0x0	presetn_i2c6_req presetn_i2c6 request bit When HIGH, reset relative logic
11	RW	0x0	presetn_i2c2_req presetn_i2c2 request bit When HIGH, reset relative logic
10	RW	0x0	presetn_i2c5_req presetn_i2c5 request bit When HIGH, reset relative logic
9	RW	0x0	presetn_i2c1_req presetn_i2c1 request bit When HIGH, reset relative logic
8	RW	0x0	presetn_efuse_1024s_req presetn_efuse_1024s request bit When HIGH, reset relative logic
7	RW	0x0	presetn_efuse_1024_req presetn_efuse_1024 request bit When HIGH, reset relative logic
6	RW	0x0	presetn_perilp1_noc_req presetn_perilp1_noc request bit When HIGH, reset relative logic
5	RW	0x0	hresetn_spdif_8ch_req hresetn_spdif_8ch request bit When HIGH, reset relative logic
4	RW	0x0	hresetn_i2s2_req hresetn_i2s2 request bit When HIGH, reset relative logic
3	RW	0x0	hresetn_i2s1_req hresetn_i2s1 request bit When HIGH, reset relative logic

Bit	Attr	Reset Value	Description
2	RW	0x0	hresetn_i2s0_req hresetn_i2s0 request bit When HIGH, reset relative logic
1	RW	0x0	hresetn_perilp1_noc_req hresetn_perilp1_noc request bit When HIGH, reset relative logic
0	RW	0x0	hresetn_perilp1_req hresetn_perilp1 request bit When HIGH, reset relative logic

CRU_SOFTRST_CON13
Address: Operational Base + offset (0x0434)
Internal software reset control register13

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	resetn_spi5_req resetn_spi5 request bit When HIGH, reset relative logic
14	RW	0x0	resetn_spi4_req resetn_spi4 request bit When HIGH, reset relative logic
13	RW	0x0	resetn_spi2_req resetn_spi2 request bit When HIGH, reset relative logic
12	RW	0x0	resetn_spi1_req resetn_spi1 request bit When HIGH, reset relative logic
11	RW	0x0	resetn_spi0_req resetn_spi0 request bit When HIGH, reset relative logic
10	RW	0x0	presetn_spi5_req presetn_spi5 request bit When HIGH, reset relative logic
9	RW	0x0	presetn_spi4_req presetn_spi4 request bit When HIGH, reset relative logic
8	RW	0x0	presetn_spi2_req presetn_spi2 request bit When HIGH, reset relative logic
7	RW	0x0	presetn_spi1_req presetn_spi1 request bit When HIGH, reset relative logic

Bit	Attr	Reset Value	Description
6	RW	0x0	presetn_spi0_req presetn_spi0 request bit When HIGH, reset relative logic
5	RW	0x0	presetn_tsadc_req presetn_tsadc request bit When HIGH, reset relative logic
4	RW	0x0	presetn_saradc_req presetn_saradc request bit When HIGH, reset relative logic
3	RW	0x0	presetn_uart3_req presetn_uart3 request bit When HIGH, reset relative logic
2	RW	0x0	presetn_uart2_req presetn_uart2 request bit When HIGH, reset relative logic
1	RW	0x0	presetn_uart1_req presetn_uart1 request bit When HIGH, reset relative logic
0	RW	0x0	presetn_uart0_req presetn_uart0 request bit When HIGH, reset relative logic

CRU_SOFTRST_CON14
Address: Operational Base + offset (0x0438)
Internal software reset control register14

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	hresetn_sdioaudio_noc_req hresetn_sdioaudio_noc request bit When HIGH, reset relative logic
14	RW	0x0	resetn_i2c7_req resetn_i2c7 request bit When HIGH, reset relative logic
13	RW	0x0	resetn_i2c3_req resetn_i2c3 request bit When HIGH, reset relative logic
12	RW	0x0	resetn_i2c6_req resetn_i2c6 request bit When HIGH, reset relative logic
11	RW	0x0	resetn_i2c2_req resetn_i2c2 request bit When HIGH, reset relative logic

Bit	Attr	Reset Value	Description
10	RW	0x0	resetn_i2c5_req resetn_i2c5 request bit When HIGH, reset relative logic
9	RW	0x0	resetn_i2c1_req resetn_i2c1 request bit When HIGH, reset relative logic
8	RW	0x0	resetn_tsadc_req resetn_tsadc request bit When HIGH, reset relative logic
7	RW	0x0	resetn_uart3_req resetn_uart3 request bit When HIGH, reset relative logic
6	RW	0x0	resetn_uart2_req resetn_uart2 request bit When HIGH, reset relative logic
5	RW	0x0	resetn_uart1_req resetn_uart1 request bit When HIGH, reset relative logic
4	RW	0x0	resetn_uart0_req resetn_uart0 request bit When HIGH, reset relative logic
3	RW	0x0	resetn_spdif_8ch_req resetn_spdif_8ch request bit When HIGH, reset relative logic
2	RW	0x0	resetn_i2s2_req resetn_i2s2 request bit When HIGH, reset relative logic
1	RW	0x0	resetn_i2s1_req resetn_i2s1 request bit When HIGH, reset relative logic
0	RW	0x0	resetn_i2s0_req resetn_i2s0 request bit When HIGH, reset relative logic

CRU_SOFTRST_CON15

Address: Operational Base + offset (0x043c)

Internal software reset control register15

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RO	0x0	reserved

Bit	Attr	Reset Value	Description
14	RW	0x0	resetn_dp_i2s_req resetn_dp_i2s request bit When HIGH, reset relative logic
13	RW	0x0	resetn_dp_core_req resetn_dp_core request bit When HIGH, reset relative logic
12	RW	0x0	presetn_mipi_dsi1_req presetn_mipi_dsi1 request bit When HIGH, reset relative logic
11	RW	0x0	presetn_mipi_dsi0_req presetn_mipi_dsi0 request bit When HIGH, reset relative logic
10	RW	0x0	cresetn_dp_ctrl_req cresetn_dp_ctrl request bit When HIGH, reset relative logic
9	RW	0x0	sresetn_dp_ctrl_req sresetn_dp_ctrl request bit When HIGH, reset relative logic
8	RW	0x0	presetn_dp_ctrl_req presetn_dp_ctrl request bit When HIGH, reset relative logic
7	RW	0x0	presetn_hdmi_ctrl_req presetn_hdmi_ctrl request bit When HIGH, reset relative logic
6	RW	0x0	presetn_hdcp_req presetn_hdcp request bit When HIGH, reset relative logic
5	RW	0x0	presetn_hdcp_noc_req presetn_hdcp_noc request bit When HIGH, reset relative logic
4	RW	0x0	hresetn_hdcp_req hresetn_hdcp request bit When HIGH, reset relative logic
3	RW	0x0	hresetn_hdcp_noc_req hresetn_hdcp_noc request bit When HIGH, reset relative logic
2	RW	0x0	aresetn_hdcp_req aresetn_hdcp request bit When HIGH, reset relative logic
1	RW	0x0	aresetn_hdcp_noc_req aresetn_hdcp_noc request bit When HIGH, reset relative logic
0	RW	0x0	aresetn_vio_noc_req aresetn_vio_noc request bit When HIGH, reset relative logic

CRU_SOFTRST_CON16
Address: Operational Base + offset (0x0440)
Internal software reset control register16

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	resetn_isp1_req resetn_isp1 request bit When HIGH, reset relative logic
14	RW	0x0	resetn_isp0_req resetn_isp0 request bit When HIGH, reset relative logic
13	RW	0x0	hresetn_isp1_req hresetn_isp1 request bit When HIGH, reset relative logic
12	RW	0x0	hresetn_isp0_req hresetn_isp0 request bit When HIGH, reset relative logic
11	RW	0x0	hresetn_isp1_noc_req hresetn_isp1_noc request bit When HIGH, reset relative logic
10	RW	0x0	hresetn_isp0_noc_req hresetn_isp0_noc request bit When HIGH, reset relative logic
9:8	RO	0x0	reserved
7	RW	0x0	aresetn_isp1_noc_req aresetn_isp1_noc request bit When HIGH, reset relative logic
6	RW	0x0	aresetn_isp0_noc_req aresetn_isp0_noc request bit When HIGH, reset relative logic
5	RW	0x0	resetn_hdcp_ctrl_req resetn_hdcp_ctrl request bit When HIGH, reset relative logic
4	RW	0x0	resetn_hdmi_ctrl_req resetn_hdmi_ctrl request bit When HIGH, reset relative logic
3	RW	0x0	resetn_dptx_spdif_rec_req resetn_dptx_spdif_rec request bit When HIGH, reset relative logic
2	RW	0x0	presetn_vio_grf_req presetn_vio_grf request bit When HIGH, reset relative logic

Bit	Attr	Reset Value	Description
1	RO	0x0	reserved
0	RW	0x0	presetn_gasket_req presetn_gasket request bit When HIGH, reset relative logic

CRU_SOFTRST_CON17
Address: Operational Base + offset (0x0444)
Internal software reset control register17

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:14	RO	0x0	reserved
13	RW	0x0	presetn_edp_ctrl_req presetn_edp_ctrl request bit When HIGH, reset relative logic
12	RW	0x0	presetn_edp_noc_req presetn_edp_noc request bit When HIGH, reset relative logic
11	RW	0x0	resetn_vop1_pwm_req resetn_vop1_pwm request bit When HIGH, reset relative logic
10	RW	0x0	resetn_vop0_pwm_req resetn_vop0_pwm request bit When HIGH, reset relative logic
9	RW	0x0	dresetn_vop1_req dresetn_vop1 request bit When HIGH, reset relative logic
8	RW	0x0	dresetn_vop0_req dresetn_vop0 request bit When HIGH, reset relative logic
7	RW	0x0	hresetn_vop1_req hresetn_vop1 request bit When HIGH, reset relative logic
6	RW	0x0	hresetn_vop0_req hresetn_vop0 request bit When HIGH, reset relative logic
5	RW	0x0	hresetn_vop1_noc_req hresetn_vop1_noc request bit When HIGH, reset relative logic
4	RW	0x0	hresetn_vop0_noc_req hresetn_vop0_noc request bit When HIGH, reset relative logic

Bit	Attr	Reset Value	Description
3	RW	0x0	aresetn_vop1_req aresetn_vop1 request bit When HIGH, reset relative logic
2	RW	0x0	aresetn_vop0_req aresetn_vop0 request bit When HIGH, reset relative logic
1	RW	0x0	aresetn_vop1_noc_req aresetn_vop1_noc request bit When HIGH, reset relative logic
0	RW	0x0	aresetn_vop0_noc_req aresetn_vop0_noc request bit When HIGH, reset relative logic

CRU_SOFTRST_CON18
Address: Operational Base + offset (0x0448)
Internal software reset control register18

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:9	RO	0x0	reserved
8	RW	0x0	pmu_srstn_req pmu_srstn request bit When HIGH, reset relative logic
7	RW	0x0	aresetn_usb3_grf_req aresetn_usb3_grf request bit When HIGH, reset relative logic
6	RW	0x0	aresetn_usb3_otg1_req aresetn_usb3_otg1 request bit When HIGH, reset relative logic
5	RW	0x0	aresetn_usb3_otg0_req aresetn_usb3_otg0 request bit When HIGH, reset relative logic
4	RW	0x0	aresetn_usb3_noc_req aresetn_usb3_noc request bit When HIGH, reset relative logic
3	RW	0x0	resetn_pvtm_gpu_req resetn_pvtm_gpu request bit When HIGH, reset relative logic
2	RW	0x0	aresetn_gpu_grf_req aresetn_gpu_grf request bit When HIGH, reset relative logic

Bit	Attr	Reset Value	Description
1	RW	0x0	aresetn_gpu_noc_req aresetn_gpu_noc request bit When HIGH, reset relative logic
0	RW	0x0	aresetn_gpu_req aresetn_gpu request bit When HIGH, reset relative logic

CRU_SOFTRST_CON19
Address: Operational Base + offset (0x044c)
Internal software reset control register19

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	presetn_alive_sgrf_req presetn_alive_sgrf request bit When HIGH, reset relative logic
14	RW	0x0	presetn_intr_arb_pmu_req presetn_intr_arb_pmu request bit When HIGH, reset relative logic
13	RW	0x0	timer11_srstn_req timer11_srstn request bit When HIGH, reset relative logic
12	RW	0x0	timer10_srstn_req timer10_srstn request bit When HIGH, reset relative logic
11	RW	0x0	timer9_srstn_req timer9_srstn request bit When HIGH, reset relative logic
10	RW	0x0	timer8_srstn_req timer8_srstn request bit When HIGH, reset relative logic
9	RW	0x0	timer7_srstn_req timer7_srstn request bit When HIGH, reset relative logic
8	RW	0x0	timer6_srstn_req timer6_srstn request bit When HIGH, reset relative logic
7	RW	0x0	timer_6_11_psrstn_req timer_6_11_psrstn request bit When HIGH, reset relative logic
6	RW	0x0	timer5_srstn_req timer5_srstn request bit When HIGH, reset relative logic

Bit	Attr	Reset Value	Description
5	RW	0x0	timer4_srstn_req timer4_srstn request bit When HIGH, reset relative logic
4	RW	0x0	timer3_srstn_req timer3_srstn request bit When HIGH, reset relative logic
3	RW	0x0	timer2_srstn_req timer2_srstn request bit When HIGH, reset relative logic
2	RW	0x0	timer1_srstn_req timer1_srstn request bit When HIGH, reset relative logic
1	RW	0x0	timer0_srstn_req timer0_srstn request bit When HIGH, reset relative logic
0	RW	0x0	timer_0_5_psrstn_req timer_0_5_psrstn request bit When HIGH, reset relative logic

CRU_SOFTRST_CON20
Address: Operational Base + offset (0x0450)
Internal software reset control register20

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15	RW	0x0	presetn_uphy1_tcpdctrl_req presetn_uphy1_tcpdctrl request bit When HIGH, reset relative logic
14	RW	0x0	presetn_uphy0_tcpdctrl_req presetn_uphy0_tcpdctrl request bit When HIGH, reset relative logic
13	RW	0x0	presetn_uphy1_tcphy_req presetn_uphy1_tcphy request bit When HIGH, reset relative logic
12	RW	0x0	presetn_uphy0_tcphy_req presetn_uphy0_tcphy request bit When HIGH, reset relative logic
11	RO	0x0	reserved
10	RW	0x0	presetn_uphy0_apb_req presetn_uphy0_apb request bit When HIGH, reset relative logic
9	RO	0x0	reserved

Bit	Attr	Reset Value	Description
8	RW	0x0	presetn_uphy0_dptx_req presetn_uphy0_dptx request bit When HIGH, reset relative logic
7	RW	0x0	presetn_intr_arb_req presetn_intr_arb request bit When HIGH, reset relative logic
6	RW	0x0	presetn_wdt1_req presetn_wdt1 request bit When HIGH, reset relative logic
5	RW	0x0	presetn_wdt0_req presetn_wdt0 request bit When HIGH, reset relative logic
4	RW	0x0	presetn_alive_noc_req presetn_alive_noc request bit When HIGH, reset relative logic
3	RW	0x0	presetn_grf_req presetn_grf request bit When HIGH, reset relative logic
2	RW	0x0	presetn_gpio4_req presetn_gpio4 request bit When HIGH, reset relative logic
1	RW	0x0	presetn_gpio3_req presetn_gpio3 request bit When HIGH, reset relative logic
0	RW	0x0	presetn_gpio2_req presetn_gpio2 request bit When HIGH, reset relative logic

CRU_GLB_SRST_FST_VALUE
Address: Operational Base + offset (0x0500)
The first global software reset config value

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	glb_srst_fst_value The first global software reset config value If config 0xfdb9, it will generate first global software reset

CRU_GLB_SRST_SND_VALUE
Address: Operational Base + offset (0x0504)
The second global software reset config value

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	glb_srst_snd_value The second global software reset config value If config 0xeca8, it will generate second global software reset

CRU_GLB_CNT_TH
Address: Operational Base + offset (0x0508)
Global soft reset counter threshold

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RW	0x000	glb_rst_cnt_th global reset wait counter threshold wait cycles n(at xin_24m)

CRU_MISC_CON
Address: Operational Base + offset (0x050c)
Output clock selection for test

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:9	RO	0x0	reserved
8	RW	0x0	core_dbgrst_wfien A53/A72 dbg reset wait for STANDBYWFI enable 1'b0 : A53 dbg reset has no relation to STANDBYWFI status 1'b1 : A53 dgb reset is asserted after STANDBYWFI valid
7	RW	0x0	core_wrst_wifen A53/A72 warm reset wait for STANDBYWFI enable 1'b0 : A53/A72 warm reset has no relation to STANDBYWFI status 1'b1 : A53/A72 warm reset is asserted after STANDBYWFI valid
6	RW	0x0	core_srst_wfien A53/A72 software reset wait for STANDBYWFI enable 1'b0 : A53/A72 software reset has no relation to STANDBYWFI status 1'b1 : A53/A72 software reset is asserted after STANDBYWFI valid
5	RW	0x0	dbgrstn_en A53/A72 DBGRSTN reset enable 1'b0 : disable A53/A72 DBGRSTN reset 1'b1 : enable A53/A72 DBGRSTN reset
4	RW	0x0	warmrstn_en A53/A72 warm reset enable 1'b0 : disable A53/A72 warm reset 1'b1 : enable A53/A72 warm reset

Bit	Attr	Reset Value	Description
3:0	RW	0x0	testclk_sel Output clock selection for test 4'h0: clk_core_b_2wrap 4'h1: clk_core_l_2wrap 4'h2: aclk_cci_2wrap 4'h3: aclk_perihp_2wrap 4'h4: aclk_perilp0_2wrap 4'h5: hclk_perilp1_2wrap 4'h6: aclk_center_2wrap 4'h7: clk_ddrc_2wrap 4'h8: aclk_gpu_2wrap 4'h9: clk_rga_core_2wrap 4'ha: clk_vdu_core_2wrap 4'hb: clk_pciephy_ref100m 4'hc: dclk_vop0_2wrap 4'hd: clk_rtc 4'he: clkout_24m 4'hf: clk_wifi

CRU_GLB_RST_CON
Address: Operational Base + offset (0x0510)
Global reset trigger select

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RW	0x0	pmu_glbrst_wdt_ctrl if pmu reset by wdt resetn src select 1'b0: pmu reset by wdt rstn 1'b1: pmu does not reset by wdt rstn
3:2	RW	0x0	pmu_glb_srst_ctrl pmu reset by global soft reset select 2'b00: pmu reset by first global soft reset 2'b01: pmu reset by second global soft reset 2'b10: pmu not reset by any global soft reset
1	RW	0x0	wdt_glb_srst_ctrl watch_dog trigger global soft reset select 1'b0: watch_dog trigger second global reset 1'b1: watch_dog trigger first global reset
0	RW	0x0	tsadc_glb_srst_ctrl TSADC trigger global soft reset select 1'b0: tsadc trigger second global reset 1'b1: tsadc trigger first global reset

CRU_GLB_RST_ST
Address: Operational Base + offset (0x0514)
Global reset status

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5	W1C	0x0	snd_glb_wdt_rst_st second global watch_dog triggered reset flag 1'b0: last hot reset is not second global watch_dog triggered reset 1'b1: last hot reset is second global watch_dog triggered reset
4	W1C	0x0	fst_glb_wdt_rst_st first global watch_dog triggered reset flag 1'b0: last hot reset is not first global watch_dog triggered reset 1'b1: last hot reset is first global watch_dog triggered reset
3	W1C	0x0	snd_glb_tsadc_rst_st second global TSADC triggered reset flag 1'b0: last hot reset is not second global TSADC triggered reset 1'b1: last hot reset is second global TSADC triggered reset
2	W1C	0x0	fst_glb_tsadc_rst_st first global TSADC triggered reset flag 1'b0: last hot reset is not first global TSADC triggered reset 1'b1: last hot reset is first global TSADC triggered reset
1	W1C	0x0	snd_glb_rst_st second global rst flag 1'b0: last hot reset is not second global reset 1'b1: last hot reset is second global reset
0	W1C	0x0	fst_glb_rst_st first global rst flag 1'b0: last hot reset is not first global reset 1'b1: last hot reset is first global reset

CRU_SDMMC_CON0
Address: Operational Base + offset (0x0580)
sdmmc control0

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:0	WO	0x0004	sdmmc_con0 sdmmc con0 register refer to chapter SDMMC

CRU_SDMMC_CON1
Address: Operational Base + offset (0x0584)
sdmmc control1

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:0	WO	0x0000	sdmmc_con1 sdmmc con1 register refer to chapter SDMMC

CRU_SDIO0_CON0
Address: Operational Base + offset (0x0588)
sdio0 control0

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:0	WO	0x0004	sdio_con0 sdio_con0 register refer to chapter SDIO

CRU_SDIO0_CON1
Address: Operational Base + offset (0x058c)
sdio0 control1

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_mask write mask bits When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit
15:0	WO	0x0000	sdio_con1 sdio_con1 register refer to chapter SDIO

3.8 Timing Diagram

Power on reset timing is shown as follow:

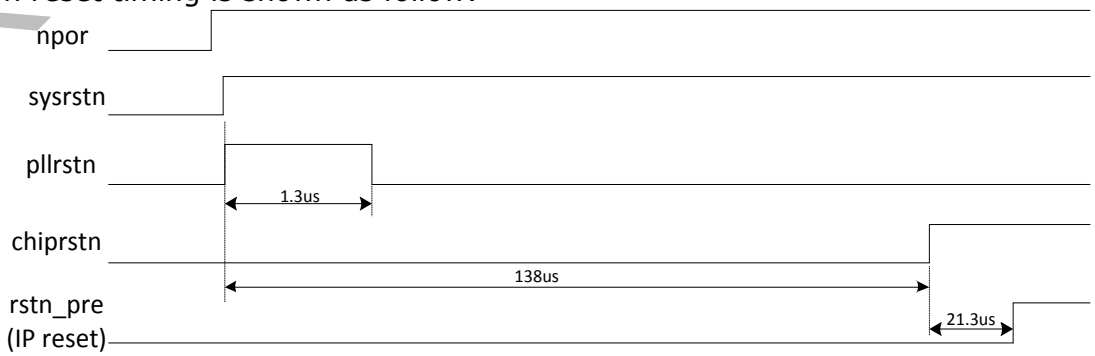


Fig. 3-7 Chip Power On Reset Timing Diagram

NPOR is hardware reset signal from out-chip, which is filtered glitch to obtain signal sysrstn.

To make PLLs work normally, the PLL reset signal (pllrstn) must maintain high for more than 1us, and PLLs start to lock when pllrstn deassert, andthe PLL max lock time is 500 PLL REFCLK cycles. And then the system will wait about 138us, and then deactive reset signal chiprstn. The signal chiprstn is used to generate output clocks in CRU. After CRU start output clocks, the system waits again for 512cycles (21.3us) to deactive signal rstn_pre, which is used to generate power on reset of all IP.

3.9 Application Notes

3.9.1 PLL usage

The chip uses 2.4GHz for all three PLLs (ARM PLL, DDR PLL and GENERAL PLL).

A. PLL output frequency configuration

FBDIV can be configured by programming CRU_*PLL_CON0;
REFDIV, POSTDIV1, POSTDIV2 can be configured by programming CRU_*PLL_CON1.
FRAC can be configured by programming CRU_*PLL_CON2.
BYPASS, PLL_WORK_MODE, POWER_DOWN, DSMPD can be configured by programming CRU_*PLL_CON3

If DSMPD = 1 (DSM is disabled, "integer mode")
FOUTVCO = FREF / REFDIV * FBDIV
FOUTPOSTDIV = FOUTVCO / POSTDIV1 / POSTDIV2
When FREF is 24MHz, and if 700MHz FOUTPOSTDIV is needed. The configuration can be:

DSMPD = 1
REFDIV = 6
FBDIV = 175
POSTDIV1=1
POSTDIV2=1

And then
FOUTVCO = FREF / REFDIV * FBDIV = 24/6*175=700
FOUTPOSTDIV = FOUTVCO / POSTDIV1 / POSTDIV2=700/1/1=700

If DSMPD = 0 (DSM is enabled, "fractional mode")
FOUTVCO = FREF / REFDIV * (FBDIV + FRAC / 224)
FOUTPOSTDIV = FOUTVCO / POSTDIV1 / POSTDIV2
When FREF is 24MHz, and if 491.52MHz FOUTPOSTDIV is needed. The configuration can be:

DSMPD = 0
REFDIV = 1
FBDIV = 40
FRAC = 24'hf5c28f
POSTDIV1=2
POSTDIV2=1

And then
FOUTVCO = FREF / REFDIV * (FBDIV + FRAC / 224) = 24/1*(40+24'hf5c28f /224)= 983.04
FOUTPOSTDIV = FOUTVCO / POSTDIV1 / POSTDIV2=983.04/2/1=491.52

B. PLL frequency range requirement

All the value range requirements are as follow.

FREF(Input Frequency Rangein Integer Mode):	1MHz to 1200MHz
FREF(Input Frequency Rangein Fractional Mode):	10MHz to 1200MHz
FREF/REFDIV(The divided reference frequency Integer Mode):	1 to FVCO/16
FREF/REFDIV(The divided reference frequency Fractional Mode):	10 to FVCO/16
FOUTVCO:	800NHz to 2.4GHz

C. PLL setting consideration

- If the POSTDIV value is changed during operation a short pulse (glitch) may occur on FOUTPOSTDIV. The minimum width of the short pulse will be equal to twice the period of the VCO. Therefore, if the circuitry clocked by the PLL is sensitive to short pulses, the new divide value should be re-timed so that it is synchronous with the rising edge of the output clock (FOUTPOSTDIV). Glitches cannot occur on any of the other outputs.

- For lowest power operation, the minimum VCO and FREF frequencies should be used. For minimum jitter operation, the highest VCO and FREF frequencies should be used. The normal operating range for the VCO is described above in .
- The supply rejection will be worse at the low end of the VCO range so care should be taken to keep the supply clean for low power applications.
- The feedback divider is not capable of dividing by all possible settings due to the use of a power-saving architecture. The following settings are valid for FBDIV:
- DSMPD=1 (Integer Mode):
- 12,13,14,16-4095 (practical value is limited to 3200, 2400, or 1600 (FVCOMAX / FREFMIN))
- DSMPD=0 (Fractional Mode):
- 19-4091 (practical value is limited to 320, 240, or 160 (FVCOMAX / FREFMIN))
- The PD input places the PLL into the lowest power mode. In this case, all analog circuits are turned off and FREF will be "ignored". The FOUTPOSTDIV and FOUTVCO pins are forced to logic low (0V).
- The BYPASS pin controls a mux which selects FREF to be passed to the FOUTPOSTDIV when active high. However, the PLL continues to run as it normally would if bypass were low. This is a useful feature for PLL testing since the clock path can be verified without the PLL being required to work. Also, the effect that the PLL induced supply noise has on the output buffering can be evaluated. It is not recommended to switch between BYPASS mode and normal mode for regular chip operation since this may result in a glitch. Also, FOUTPOSTDIVPD should be set low if the PLL is to be used in BYPASS mode.

3.9.2 PLL frequency change and lock check

The PLL programming support changed on-the-fly and the PLL will simply slew to the new frequency.
PLL lock state can be check in CRU_*PLL_CON2[31] register. The lock state is high when both original hardware PLL lock and PLL counter lock are high. The PLL counter lock initial value is CRU_GLB_CNT_TH[31:16].
The max delay time is 1500 REF_CLK.

Frequency change.
- Assert PD.
- Program the PLL to a valid setting that runs the VCO within the specified ranges.
- Release PD after no less than 1us from the time it was asserted. This will allow the power-down switch enough time to pull the loop filter voltage from rail-to-rail, which ensures the PLL will be completely powered down from any state.

PLL locking consists of three phases.
- Phase 1 is control voltage slewing. During this phase one of the clocks (reference or divide) is much faster than the other, and the PLL frequency adjusts almost continuously. When locking from power down, the divide clock is initially very slow and steadily increases frequency. Slew time is about 2~5s. It will take slightly longer for faster VCO settings when locking from power down, since the PLL must slew further.
- Phase 2 is small signal phase acquisition. During this phase, the internal up/down signals alternate semi-chaotically as the phase slowly adjusts until the two signals are aligned. The duration of this phase depends on the loop bandwidth and is faster with higher bandwidth. Bandwidth can be estimated as FREF / REFDIV / 20 for integer mode and FREF /REFDIV / 40 for fractional mode. The duration of small signal locking is about 1/Bandwidth.
- Phase 3 is the digital cycle count. After the last cycle slip is detected, an internal counter waits 500 FREF / REFDIV cycles before the lock signal goes high. This is frequently the dominant factor in lock time – especially for slower reference clock signals or large reference divide settings. This time can be calculated as 500*REFDIV/FREF.

3.9.3 Fractional divider usage

To get specific frequency, clocks of I2S, SPDIF, UARTcan be generated by fractional divider. Generally you must set that denominator is 20 times larger than numerator to generate

precise clock frequency. So the fractional divider applies only to generate low frequency clock like I2S, UART.

3.9.4 Global software reset

Two global software resets are designed in the chip, you can program CRU_GLB_SRST_FST_VALUE[15:0] as 0xfdb9 to assert the first global software reset glb_srstn_1 and program CRU_GLB_SRST_SND_VALUE[15:0] as 0xeca8 to assert the second global software reset glb_srstn_2. These two software resets are self-deasserted by hardware.
Glb_srstn_1 resets almost all logic.
Glb_srstn_2 resets almost all logic except GRF and GPIOs.

Chapter 4 General Register Files (GRF)

4.1 Overview

The general register file will be used to do static set by software, which is composed of many registers for system control. The GRF is divided into two sections,

- GRF, used for general non-secure system,
- PMUGRF, used for always on sysyem

4.2 Function Description

The function of general register file is：

- IOMUX control
- Control the state of GPIO in power-down mode
- GPIO PAD pull down and pull up control
- Used for common system control
- Used to record the system state

4.3 GRF Register description

4.3.1 Register Summary

Name	Offset	Size	Reset Value	Description
GRF_USB3_PERF_CON0	0x02000	W	0x00000000	usb3 performance monitor control register
GRF_USB3_PERF_CON1	0x02004	W	0x00000000	usb3 performance monitor control register
GRF_USB3_PERF_CON2	0x02008	W	0x00000000	usb3 performance monitor control register
GRF_USB3_PERF_RD_MAX_LATENCY_NUM	0x0200c	W	0x00000000	usb3 performance monitor status register
GRF_USB3_PERF_RD_LATENCY_SAMP_NUM	0x02010	W	0x00000000	usb3 performance monitor status register
GRF_USB3_PERF_RD_LATENCY_ACC_NUM	0x02014	W	0x00000000	usb3 performance monitor status register
GRF_USB3_PERF_RD_AXI_TOTAL_BYTE	0x02018	W	0x00000000	usb3 performance monitor status register
GRF_USB3_PERF_WR_AXI_TOTAL_BYTE	0x0201c	W	0x00000000	usb3 performance monitor status register
GRF_USB3_PERF_WORKING_CNT	0x02020	W	0x00000000	usb3 performance monitor status register
GRF_USB3OTG0_CON0	0x02430	W	0x00002000	USB3 OTG0 GRF Register0
GRF_USB3OTG0_CON1	0x02434	W	0x00001100	USB3 OTG0 GRF Register1
GRF_USB3OTG1_CON0	0x02440	W	0x00002000	USB3 OTG1 GRF Register0
GRF_USB3OTG1_CON1	0x02444	W	0x00001100	USB3 OTG1 GRF Register1
GRF_USB3OTG0_STATUS_LAT0	0x02450	W	0x00000000	USB3 OTG0 status register
GRF_USB3OTG0_STATUS_LAT1	0x02454	W	0x00000000	USB3 OTG1 status register

Name	Offset	Size	Reset Value	Description
GRF_USB3OTG0_STATUS_CB	0x02458	W	0x00000000	USB3 OTG0 status register
GRF_USB3OTG1_STATUS_LAT0	0x02460	W	0x00000000	USB3 OTG1 status register
GRF_USB3OTG1_STATUS_LAT1	0x02464	W	0x00000000	USB3 OTG1 status register
GRF_USB3OTG1_STATUS_CB	0x02468	W	0x00000000	USB3 OTG1 status register
GRF_PCIE_PERF_CON0	0x04000	W	0x00000000	pcie performance monitor control register
GRF_PCIE_PERF_CON1	0x04004	W	0x00000000	pcie performance monitor control register
GRF_PCIE_PERF_CON2	0x04008	W	0x00000000	pcie performance monitor control register
GRF_PCIE_PERF_RD_MAX_LATENCY_NUM	0x0400c	W	0x00000000	pcieperformance monitor status register
GRF_PCIE_PERF_RD_LATENCY_SAMP_NUM	0x04010	W	0x00000000	pcie performance monitor status register
GRF_PCIE_PERF_RD_LATENCY_ACC_NUM	0x04014	W	0x00000000	pcie performance monitor status register
GRF_PCIE_PERF_RD_AXI_TOTAL_BYTE	0x04018	W	0x00000000	pcie performance monitor status register
GRF_PCIE_PERF_WR_AXI_TOTAL_BYTE	0x0401c	W	0x00000000	pcie performance monitor status register
GRF_PCIE_PERF_WORKING_CNT	0x04020	W	0x00000000	pcie performance monitor status register
GRF_USB20_HOST0_CON0	0x04100	W	0x000023e0	USB20 Host0 GRF register0
GRF_USB20_HOST0_CON1	0x04104	W	0x00000820	USB20 Host0 GRF register1
GRF_USB20_HOST1_CON0	0x04110	W	0x000023e0	USB20 Host1 GRF register0
GRF_USB20_HOST1_CON1	0x04114	W	0x00000820	USB20 Host1 GRF register1
GRF_HSIC_CON0	0x04120	W	0x000002f0	HSIC controller GRF register 0
GRF_HSIC_CON1	0x04124	W	0x00000820	HSIC controller GRF register1
GRF_GRF_USBHOST0_STATUS	0x04140	W	0x00000000	usb host0 controller status register
GRF_GRF_USBHOST1_STATUS	0x04144	W	0x00000000	usb host1 controller status register
GRF_GRF_HSIC_STATUS	0x04148	W	0x00000000	hsic controller status register
GRF_HSICPHY_CON0	0x04470	W	0x0000004f	HSICPHY GRF control register
GRF_usbphy0_ctrl0	0x04480	W	0x0000850f	usbphy0_ctrl0
GRF_usbphy0_ctrl1	0x04484	W	0x0000e007	usbphy0_ctrl1
GRF_usbphy0_ctrl2	0x04488	W	0x000082e7	usbphy0_ctrl2
GRF_usbphy0_ctrl3	0x0448c	W	0x000002a2	usbphy0_ctrl3

Name	Offset	Size	Reset Value	Description
GRF_usbphy0_ctrl4	0x04490	W	0x00005554	usbphy0_ctrl4
GRF_usbphy0_ctrl5	0x04494	W	0x00004555	usbphy0_ctrl5
GRF_usbphy0_ctrl6	0x04498	W	0x00000005	usbphy0_ctrl6
GRF_usbphy0_ctrl7	0x0449c	W	0x000068c8	usbphy0_ctrl7
GRF_usbphy0_ctrl8	0x044a0	W	0x00000000	usbphy0_ctrl8
GRF_usbphy0_ctrl9	0x044a4	W	0x00000000	usbphy0_ctrl9
GRF_usbphy0_ctrl10	0x044a8	W	0x00000000	usbphy0_ctrl10
GRF_usbphy0_ctrl11	0x044ac	W	0x00000000	usbphy0_ctrl11
GRF_usbphy0_ctrl12	0x044b0	W	0x000000a1	usbphy0_ctrl12
GRF_usbphy0_ctrl13	0x044b4	W	0x0000850f	usbphy0_ctrl13
GRF_usbphy0_ctrl14	0x044b8	W	0x0000e007	usbphy0_ctrl14
GRF_usbphy0_ctrl15	0x044bc	W	0x000002e7	usbphy0_ctrl15
GRF_usbphy0_ctrl16	0x044c0	W	0x00000200	usbphy0_ctrl16
GRF_usbphy0_ctrl17	0x044c4	W	0x00005554	usbphy0_ctrl17
GRF_usbphy0_ctrl18	0x044c8	W	0x00004555	usbphy0_ctrl18
GRF_usbphy0_ctrl19	0x044cc	W	0x00000005	usbphy0_ctrl19
GRF_usbphy0_ctrl20	0x044d0	W	0x000068c8	usbphy0_ctrl20
GRF_usbphy0_ctrl21	0x044d4	W	0x00000000	usbphy0_ctrl21
GRF_usbphy0_ctrl22	0x044d8	W	0x00000000	usbphy0_ctrl22
GRF_usbphy0_ctrl23	0x044dc	W	0x00000000	usbphy0_ctrl23
GRF_usbphy0_ctrl24	0x044e0	W	0x00000000	usbphy0_ctrl24
GRF_usbphy0_ctrl25	0x044e4	W	0x00000021	usbphy0_ctrl25
GRF_usbphy1_ctrl0	0x04500	W	0x0000850f	usbphy1_ctrl0
GRF_usbphy1_ctrl1	0x04504	W	0x0000e007	usbphy1_ctrl1
GRF_usbphy1_ctrl2	0x04508	W	0x000082e7	usbphy1_ctrl2
GRF_usbphy1_ctrl3	0x0450c	W	0x000002a2	usbphy1_ctrl3
GRF_usbphy1_ctrl4	0x04510	W	0x00005554	usbphy1_ctrl4
GRF_usbphy1_ctrl5	0x04514	W	0x00004555	usbphy1_ctrl5
GRF_usbphy1_ctrl6	0x04518	W	0x00000005	usbphy1_ctrl6
GRF_usbphy1_ctrl7	0x0451c	W	0x000068c8	usbphy1_ctrl7
GRF_usbphy1_ctrl8	0x04520	W	0x00000000	usbphy1_ctrl8
GRF_usbphy1_ctrl9	0x04524	W	0x00000000	usbphy1_ctrl9
GRF_usbphy1_ctrl10	0x04528	W	0x00000000	usbphy1_ctrl10
GRF_usbphy1_ctrl11	0x0452c	W	0x00000000	usbphy1_ctrl11
GRF_usbphy1_ctrl12	0x04530	W	0x000000a1	usbphy1_ctrl12
GRF_usbphy1_ctrl13	0x04534	W	0x0000850f	usbphy1_ctrl13
GRF_usbphy1_ctrl14	0x04538	W	0x0000e007	usbphy1_ctrl14
GRF_usbphy1_ctrl15	0x0453c	W	0x000002e7	usbphy1_ctrl15
GRF_usbphy1_ctrl16	0x04540	W	0x00000200	usbphy1_ctrl16
GRF_usbphy1_ctrl17	0x04544	W	0x00005554	usbphy1_ctrl17
GRF_usbphy1_ctrl18	0x04548	W	0x00004555	usbphy1_ctrl18
GRF_usbphy1_ctrl19	0x0454c	W	0x00000005	usbphy1_ctrl19
GRF_usbphy1_ctrl20	0x04550	W	0x000068c8	usbphy1_ctrl20
GRF_usbphy1_ctrl21	0x04554	W	0x00000000	usbphy1_ctrl21

Name	Offset	Size	Reset Value	Description
GRF_usbphy1_ctrl22	0x04558	W	0x00000000	usbphy1_ctrl22
GRF_usbphy1_ctrl23	0x0455c	W	0x00000000	usbphy1_ctrl23
GRF_usbphy1_ctrl24	0x04560	W	0x00000000	usbphy1_ctrl24
GRF_usbphy1_ctrl25	0x04564	W	0x00000021	usbphy1_ctrl25
GRF_HDCP22_PERF_CON0	0x06000	W	0x00000000	hdcp performance monitor control register
GRF_HDCP22_PERF_CON1	0x06004	W	0x00000000	hdcp performance monitor control register
GRF_HDCP22_PERF_CON2	0x06008	W	0x00000000	hdcp performance monitor control register
GRF_HDCP22_PERF_RD_MAX_LATENCY_NUM	0x0600c	W	0x00000000	hdcp performance monitor status register
GRF_HDCP22_PERF_RD_LATENCY_SAMP_NUM	0x06010	W	0x00000000	hdcp performance monitor status register
GRF_HDCP22_PERF_RD_LATENCY_ACC_NUM	0x06014	W	0x00000000	hdcp performance monitor status register
GRF_HDCP22_PERF_RD_AXI_TOTAL_BYTE	0x06018	W	0x00000000	hdcp performance monitor status register
GRF_HDCP22_PERF_WR_AXI_TOTAL_BYTE	0x0601c	W	0x00000000	hdcp performance monitor status register
GRF_HDCP22_PERF_WORKING_CNT	0x06020	W	0x00000000	hdcp performance monitor status register
GRF_SOC_CON9	0x06224	W	0x00000000	SoC control register 9
GRF_SOC_CON20	0x06250	W	0x00000249	SoC control register 20
GRF_SOC_CON21	0x06254	W	0x000002cb	SoC control register 21
GRF_SOC_CON22	0x06258	W	0x000010cb	SoC control register 22
GRF_SOC_CON23	0x0625c	W	0x00000021	SoC control register 23
GRF_SOC_CON24	0x06260	W	0x000039f0	SoC control register 24
GRF_SOC_CON25	0x06264	W	0x0000d45b	SoC control register 25
GRF_SOC_CON26	0x06268	W	0x00000110	SoC control register 26
GRF_GPU_PERF_CON0	0x08000	W	0x00000000	gpu performance monitor control register
GRF_GPU_PERF_CON1	0x08004	W	0x00000000	gpu performance monitor control register
GRF_GPU_PERF_CON2	0x08008	W	0x00000000	gpu performance monitor control register
GRF_GPU_PERF_RD_MAX_LATENCY_NUM	0x0800c	W	0x00000000	gpu performance monitor status register
GRF_GPU_PERF_RD_LATENCY_SAMP_NUM	0x08010	W	0x00000000	gpu performance monitor status register
GRF_GPU_PERF_RD_LATENCY_ACC_NUM	0x08014	W	0x00000000	gpu performance monitor status register
GRF_GPU_PERF_RD_AXI_TOTAL_BYTE	0x08018	W	0x00000000	gpu performance monitor status register

Name	Offset	Size	Reset Value	Description
GRF_GPU_PERF_WR_AXI_TOTAL_BYTE	0x0801c	W	0x00000000	gpu performance monitor status register
GRF_GPU_PERF_WORKING_CNT	0x08020	W	0x00000000	gpu performance monitor status register
GRF_CPU_CON0	0x0a000	W	0x0000000b	cpu control register 0
GRF_CPU_CON1	0x0a004	W	0x0000f000	cpu control register 1
GRF_CPU_CON2	0x0a008	W	0x0000000b	cpu control register 2
GRF_CPU_CON3	0x0a00c	W	0x00003110	cpu control register 3
GRF_CPU_STATUS0	0x0a080	W	0x00000000	cpu status register 0
GRF_CPU_STATUS1	0x0a084	W	0x00000000	cpu status register 1
GRF_CPU_STATUS2	0x0a088	W	0x00000000	cpu status register 2
GRF_CPU_STATUS3	0x0a08c	W	0x00000000	cpu status register 3
GRF_CPU_STATUS4	0x0a090	W	0x00000000	cpu status register 4
GRF_CPU_STATUS5	0x0a094	W	0x00000000	cpu status register 5
GRF_A53_PERF_CON0	0x0a100	W	0x00000000	a53 performance monitor control register
GRF_A53_PERF_CON1	0x0a104	W	0x00000000	a53 performance monitor control register
GRF_A53_PERF_CON2	0x0a108	W	0x00000000	a53 performance monitor control register
GRF_A53_PERF_CON3	0x0a10c	W	0x00000000	a53 performance monitor control register
GRF_A53_PERF_RD_MON_ST	0x0a110	W	0x00000000	performance monitor read start address
GRF_A53_PERF_RD_MON_END	0x0a114	W	0x00000000	performance monitor end address
GRF_A53_PERF_WR_MON_ST	0x0a118	W	0x00000000	performance write monitor start address
GRF_A53_PERF_WR_MON_END	0x0a11c	W	0x00000000	performance monitor write end address
GRF_A53_PERF_RD_MAX_LATENCY_NUM	0x0a120	W	0x00000000	a53 performance monitor status register
GRF_A53_PERF_RD_LATENCY_SAMP_NUM	0x0a124	W	0x00000000	a53 performance monitor status register
GRF_A53_PERF_RD_LATENCY_ACC_NUM	0x0a128	W	0x00000000	a53 performance monitor status register
GRF_A53_PERF_RD_AXI_TOTAL_BYTE	0x0a12c	W	0x00000000	a53 performance monitor status register
GRF_A53_PERF_WR_AXI_TOTAL_BYTE	0x0a130	W	0x00000000	a53 performance monitor status register
GRF_A53_PERF_WORKING_CNT	0x0a134	W	0x00000000	a53 performance monitor status register
GRF_A53_PERF_INT_STATUS	0x0a138	W	0x00000000	a53 performance monitor status register

Name	Offset	Size	Reset Value	Description
GRF_A72_PERF_CON0	0x0a200	W	0x00000000	a72 performance monitor control register
GRF_A72_PERF_CON1	0x0a204	W	0x00000000	a72 performance monitor control register
GRF_A72_PERF_CON2	0x0a208	W	0x00000000	a72 performance monitor control register
GRF_A72_PERF_CON3	0x0a20c	W	0x00000000	a72 performance monitor control register
GRF_A72_PERF_RD_MON_ST	0x0a210	W	0x00000000	performance monitor read start address
GRF_A72_PERF_RD_MON_END	0x0a214	W	0x00000000	performance monitor end address
GRF_A72_PERF_WR_MON_ST	0x0a218	W	0x00000000	performance write monitor start address
GRF_A72_PERF_WR_MON_END	0x0a21c	W	0x00000000	performance monitor write end address
GRF_A72_PERF_RD_MAX_LATENCY_NUM	0x0a220	W	0x00000000	a72 performance monitor status register
GRF_A72_PERF_RD_LATENCY_SAMP_NUM	0x0a224	W	0x00000000	a72 performance monitor status register
GRF_A72_PERF_RD_LATENCY_ACC_NUM	0x0a228	W	0x00000000	a72 performance monitor status register
GRF_A72_PERF_RD_AXI_TOTAL_BYTE	0x0a22c	W	0x00000000	a72 performance monitor status register
GRF_A72_PERF_WR_AXI_TOTAL_BYTE	0x0a230	W	0x00000000	a72 performance monitor status register
GRF_A72_PERF_WORKING_CNT	0x0a234	W	0x00000000	a72 performance monitor status register
GRF_A72_PERF_INT_STATUS	0x0a238	W	0x00000000	a72 performance monitor status register
GRF_GMAC_PERF_CON0	0x0c000	W	0x00000000	gmac performance monitor control register
GRF_GMAC_PERF_CON1	0x0c004	W	0x00000000	gmac performance monitor control register
GRF_GMAC_PERF_CON2	0x0c008	W	0x00000000	gmac performance monitor control register
GRF_GMAC_PERF_RD_MAX_LATENCY_NUM	0x0c00c	W	0x00000000	gmac performance monitor status register
GRF_GMAC_PERF_RD_LATENCY_SAMP_NUM	0x0c010	W	0x00000000	gmac performance monitor status register
GRF_GMAC_PERF_RD_LATENCY_ACC_NUM	0x0c014	W	0x00000000	gmac performance monitor status register
GRF_GMAC_PERF_RD_AXI_TOTAL_BYTE	0x0c018	W	0x00000000	gmac performance monitor status register

Name	Offset	Size	Reset Value	Description
GRF_GMAC_PERF_WR_AXI_TOTAL_BYTE	0x0c01c	W	0x00000000	gmac performance monitor status register
GRF_GMAC_PERF_WORKING_CNT	0x0c020	W	0x00000000	gmac performance monitor status register
GRF_SOC_CON5	0x0c214	W	0x00000008	SoC control register 5
GRF_SOC_CON6	0x0c218	W	0x00000000	SoC control register 6
GRF_GPIO2A_IOMUX	0x0e000	W	0x00000000	GPIO2A iomux control
GRF_GPIO2B_IOMUX	0x0e004	W	0x00000000	GPIO2B iomux control
GRF_GPIO2C_IOMUX	0x0e008	W	0x00000000	GPIO2C iomux control
GRF_GPIO2D_IOMUX	0x0e00c	W	0x00000000	GPIO2D iomux control
GRF_GPIO3A_IOMUX	0x0e010	W	0x00000000	GPIO3A iomux control
GRF_GPIO3B_IOMUX	0x0e014	W	0x00000000	GPIO3B iomux control
GRF_GPIO3C_IOMUX	0x0e018	W	0x00000000	GPIO3C iomux control
GRF_GPIO3D_IOMUX	0x0e01c	W	0x00000000	GPIO3D iomux control
GRF_GPIO4A_IOMUX	0x0e020	W	0x00000000	GPIO4A iomux control
GRF_GPIO4B_IOMUX	0x0e024	W	0x00000000	GPIO4B iomux control
GRF_GPIO4C_IOMUX	0x0e028	W	0x00000000	GPIO4C iomux control
GRF_GPIO4D_IOMUX	0x0e02c	W	0x00000000	GPIO4D iomux control
GRF_GPIO2A_P	0x0e040	W	0x00006aa5	GPIO2A PU/PD control
GRF_GPIO2B_P	0x0e044	W	0x00000155	GPIO2B PU/PD control
GRF_GPIO2C_P	0x0e048	W	0x0000ffff	GPIO2C PU/PD control
GRF_GPIO2D_P	0x0e04c	W	0x0000007f	GPIO2D PU/PD control
GRF_GPIO3A_P	0x0e050	W	0x00005a5a	GPIO3A PU/PD control
GRF_GPIO3B_P	0x0e054	W	0x00005559	GPIO3B PU/PD control
GRF_GPIO3C_P	0x0e058	W	0x00000005	GPIO3C PU/PD control
GRF_GPIO3D_P	0x0e05c	W	0x0000aaaa	GPIO3D PU/PD control
GRF_GPIO4A_P	0x0e060	W	0x0000aa96	GPIO4A PU/PD control
GRF_GPIO4B_P	0x0e064	W	0x00000655	GPIO4B PU/PD control
GRF_GPIO4C_P	0x0e068	W	0x00006965	GPIO4C PU/PD control
GRF_GPIO4D_P	0x0e06c	W	0x00002aa9	GPIO4D PU/PD control
GRF_GPIO2A_SR	0x0e080	W	0x00000000	GPIO2A slew rate control
GRF_GPIO2B_SR	0x0e084	W	0x00000000	GPIO2B slew rate control
GRF_GPIO2C_SR	0x0e088	W	0x00000000	GPIO2C slew rate control
GRF_GPIO2D_SR	0x0e08c	W	0x00000000	GPIO2D slew rate control
GRF_GPIO3D_SR	0x0e09c	W	0x00000000	GPIO3D slew rate control
GRF_GPIO4A_SR	0x0e0a0	W	0x00000000	GPIO4A slew rate control
GRF_GPIO4B_SR	0x0e0a4	W	0x0000003f	GPIO4B slew rate control
GRF_GPIO4C_SR	0x0e0a8	W	0x00000000	GPIO4C slew rate control
GRF_GPIO4D_SR	0x0e0ac	W	0x00000000	GPIO4D slew rate control
GRF_GPIO2A_SMT	0x0e0c0	W	0x00000000	GPIO2A smitter control register
GRF_GPIO2B_SMT	0x0e0c4	W	0x00000000	GPIO2B smitter control register

Name	Offset	Size	Reset Value	Description
GRF_GPIO2C_SMT	0x0e0c8	W	0x00000000	GPIO2C smitter control register
GRF_GPIO2D_SMT	0x0e0cc	W	0x00000000	GPIO2D smitter control register
GRF_GPIO3A_SMT	0x0e0d0	W	0x000000f0	GPIO3A smitter control register
GRF_GPIO3B_SMT	0x0e0d4	W	0x00000000	GPIO3B smitter control register
GRF_GPIO3C_SMT	0x0e0d8	W	0x00000000	GPIO3C smitter control register
GRF_GPIO3D_SMT	0x0e0dc	W	0x00000000	GPIO3D smitter control register
GRF_GPIO4A_SMT	0x0e0e0	W	0x00000000	GPIO4A smitter control register
GRF_GPIO4B_SMT	0x0e0e4	W	0x0000003f	GPIO4B smitter control register
GRF_GPIO4C_SMT	0x0e0e8	W	0x00000000	GPIO4C smitter control register
GRF_GPIO4D_SMT	0x0e0ec	W	0x00000000	GPIO4D smitter control register
GRF_GPIO2A_E	0x0e100	W	0x00000000	GPIO2A drive strength control
GRF_GPIO2B_E	0x0e104	W	0x00000000	GPIO2B drive strength control
GRF_GPIO2C_E	0x0e108	W	0x00000000	GPIO2C drive strength control
GRF_GPIO2D_E	0x0e10c	W	0x00000000	GPIO2D drive strength control
GRF_GPIO3A_E01	0x0e110	W	0x00000000	GPIO3A drive strength control
GRF_GPIO3A_E2	0x0e114	W	0x00000000	GPIO3B drive strength control
GRF_GPIO3B_E01	0x0e118	W	0x00000000	GPIO3B drive strength control
GRF_GPIO3B_E2	0x0e11c	W	0x00000000	GPIO3B drive strength control
GRF_GPIO3C_E01	0x0e120	W	0x00000000	GPIO3C drive strength control
GRF_GPIO3C_E2	0x0e124	W	0x00000000	GPIO3C drive strength control
GRF_GPIO3D_E	0x0e128	W	0x00000000	GPIO3D drive strength control
GRF_GPIO4A_E	0x0e12c	W	0x00000000	GPIO4A drive strength control

Name	Offset	Size	Reset Value	Description
GRF_GPIO4B_E01	0x0e130	W	0x00009249	GPIO4B drive strength control
GRF_GPIO4B_E2	0x0e134	W	0x00000000	GPIO4B drive strength control
GRF_GPIO4C_E	0x0e138	W	0x00000000	GPIO4C drive strength control
GRF_GPIO4D_E	0x0e13c	W	0x00000000	GPIO4D drive strength control
GRF_GPIO2C_HE	0x0e188	W	0x00000000	GPIO2C HE control
GRF_GPIO2D_HE	0x0e18c	W	0x00000000	GPIO2D HE control
GRF_SOC_CON0	0x0e200	W	0x00000000	SoC control register 0
GRF_SOC_CON1	0x0e204	W	0x00000000	SoC control register 2
GRF_SOC_CON2	0x0e208	W	0x00000000	SoC control register 1
GRF_SOC_CON3	0x0e20c	W	0x00000000	SoC control register 3
GRF_SOC_CON4	0x0e210	W	0x0000010f	SoC control register 4
GRF_SOC_CON_5_PCIE	0x0e214	W	0x00000002	SoC control register 5
GRF_SOC_CON7	0x0e21c	W	0x00001000	SoC control register 7
GRF_SOC_CON8	0x0e220	W	0x00000000	SoC control register 8
GRF_SOC_CON_9_PCIE	0x0e224	W	0x00000000	SoC control register 9 for PCIE
GRF_SOC_STATUS0	0x0e2a0	W	0x00000003	SOC status register 0
GRF_SOC_STATUS1	0x0e2a4	W	0x00000000	SOC status register 1
GRF_SOC_STATUS2	0x0e2a8	W	0x00000000	SOC status register 2
GRF_SOC_STATUS3	0x0e2ac	W	0x00000000	SOC status register 3
GRF_SOC_STATUS4	0x0e2b0	W	0x00000000	SOC status register 4
GRF_SOC_STATUS5	0x0e2b4	W	0x00000000	SOC status register 5
GRF_DDRC0_CON0	0x0e380	W	0x00001f81	ddrc0 control register 0
GRF_DDRC0_CON1	0x0e384	W	0x00000000	ddrc0 control register 1
GRF_DDRC1_CON0	0x0e388	W	0x00001f81	ddrc1 control register 0
GRF_DDRC1_CON1	0x0e38c	W	0x00000000	ddrc1 control register 1
GRF_SIG_DETECT_CON0	0x0e3c0	W	0x00000000	Singal detect control register0
GRF_SIG_DETECT_CON1	0x0e3c8	W	0x00000000	Singal detect control register1
GRF_SIG_DETECT_CLR	0x0e3d0	W	0x00000000	Signal detect status clear register
GRF_SIG_DETECT_STATUS	0x0e3e0	W	0x00000000	Signal detect status register
GRF_USB20_PHY0_CON0	0x0e450	W	0x00000000	USB20 PHY0 GRF Register 0
GRF_USB20_PHY0_CON1	0x0e454	W	0x00001452	USB20 PHY0 GRF Register 1
GRF_USB20_PHY0_CON2	0x0e458	W	0x000003d2	USB20 PHY0 GRF Register 2
GRF_USB20_PHY0_CON3	0x0e45c	W	0x00000001	USB20 PHY0 GRF Register 3
GRF_USB20_PHY1_CON0	0x0e460	W	0x00000000	USB20 PHY1 GRF Register 0
GRF_USB20_PHY1_CON1	0x0e464	W	0x00001452	USB20 PHY1GRF Register 1
GRF_USB20_PHY1_CON2	0x0e468	W	0x000003d2	USB20 PHY1 GRF Register 2

Name	Offset	Size	Reset Value	Description
GRF_USB20_PHY1_CON3	0x0e46c	W	0x00000001	USB20 PHY1 GRF Register 3
GRF_USB3PHY0_CON0	0x0e580	W	0x000099c8	TypeC PHY/TCPD PHY/TCPC Control register0
GRF_USB3PHY0_CON1	0x0e584	W	0x00001000	TypeC PHY/TCPD PHY/TCPC Control register1
GRF_USB3PHY0_CON2	0x0e588	W	0x00003cc8	TypeC PHY/TCPD PHY/TCPC Control register2
GRF_USB3PHY1_CON0	0x0e58c	W	0x000019c8	TypeC PHY/TCPD PHY/TCPC Control register0
GRF_USB3PHY1_CON1	0x0e590	W	0x00001000	TypeC PHY/TCPD PHY/TCPC Control register1
GRF_USB3PHY1_CON2	0x0e594	W	0x00003cc8	TypeC PHY/TCPD PHY/TCPC Control register2
GRF_USB3PHY_STATUS0	0x0e5c0	W	0x00000000	USB3PHY_STATUS0
GRF_USB3PHY_STATUS1	0x0e5c4	W	0x00000000	USB3PHY_STATUS1
GRF_DLL_CON0	0x0e600	W	0x00000000	pvtm control register
GRF_DLL_CON1	0x0e604	W	0x016e3600	pvtm control register
GRF_DLL_CON2	0x0e608	W	0x016e3600	pvtm control register
GRF_DLL_CON3	0x0e60c	W	0x016e3600	pvtm control register
GRF_DLL_CON4	0x0e610	W	0x016e3600	pvtm control register
GRF_DLL_CON5	0x0e614	W	0x00000000	pvtm control register
GRF_DLL_STATUS0	0x0e620	W	0x00000000	pvtm status register
GRF_DLL_STATUS1	0x0e624	W	0x00000000	pvtm status register
GRF_DLL_STATUS2	0x0e628	W	0x00000000	pvtm status register
GRF_DLL_STATUS3	0x0e62c	W	0x00000000	pvtm status register
GRF_DLL_STATUS4	0x0e630	W	0x00000000	pvtm status register
GRF_IO_VSEL	0x0e640	W	0x00000000	
GRF_SARADC_TESTBIT	0x0e644	W	0x00000000	saradc test bit control register
GRF_TSADC_TESTBIT_L	0x0e648	W	0x00000000	saradc test bit control register
GRF_TSADC_TESTBIT_H	0x0e64c	W	0x00000000	tsadc test bit control register
GRF_CHIP_ID_ADDR	0x0e800	W	0x00000000	chip id register
GRF_FAST_BOOT_ADDR	0x0e880	W	0x00000000	faster boot address register
GRF_EMMCCORE_CON0	0x0f000	W	0x00000000	emmc core control register
GRF_EMMCCORE_CON1	0x0f004	W	0x00000000	emmc core control register
GRF_EMMCCORE_CON2	0x0f008	W	0x00000000	emmc core control register
GRF_EMMCCORE_CON3	0x0f00c	W	0x00000000	emmc core control register
GRF_EMMCCORE_CON4	0x0f010	W	0x00000000	emmc core control register
GRF_EMMCCORE_CON5	0x0f014	W	0x00000000	emmc core control register
GRF_EMMCCORE_CON6	0x0f018	W	0x00000000	emmc core control register
GRF_EMMCCORE_CON7	0x0f01c	W	0x00000000	emmc core control register
GRF_EMMCCORE_CON8	0x0f020	W	0x00000000	emmc core control register
GRF_EMMCCORE_CON9	0x0f024	W	0x00000000	emmc core control register

Name	Offset	Size	Reset Value	Description
GRF_EMMCCORE_CON10	0x0f028	W	0x00000000	emmc core control register
GRF_EMMCCORE_CON11	0x0f02c	W	0x00000000	emmc core control register
GRF_EMMCCORE_STATUS0	0x0f040	W	0x00000000	emmc core status register
GRF_EMMCCORE_STATUS1	0x0f044	W	0x00000000	emmc core status register
GRF_EMMCCORE_STATUS2	0x0f048	W	0x00000000	emmc core status register
GRF_EMMCCORE_STATUS3	0x0f04c	W	0x00000000	emmc core status register
GRF_EMMCPHY_CON0	0x0f780	W	0x00000000	emmc phy control register
GRF_EMMCPHY_CON1	0x0f784	W	0x00000000	emmc phy control register
GRF_EMMCPHY_CON2	0x0f788	W	0x00000000	emmc phy control register
GRF_EMMCPHY_CON3	0x0f78c	W	0x00000000	emmc phy control register
GRF_EMMCPHY_CON4	0x0f790	W	0x00000000	emmc phy control register
GRF_EMMCPHY_CON5	0x0f794	W	0x00000000	emmc phy control register
GRF_EMMCPHY_CON6	0x0f798	W	0x00000000	emmc phy control register
GRF_EMMCPHY_STATUS	0x0f7a0	W	0x00000000	emmc phy status register

*Notes: Size : **B** - Byte (8 bits) access, **HW** - Half WORD (16 bits) access, **W** -WORD (32 bits) access*

4.3.2 Detail Register Description

GRF_USB3_PERF_CON0

Address: Operational Base + offset (0x02000)

usb3 performance monitor control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	usb3_rksoc_axi_perf_sel 0: usb3otg0 1: usb3otg1
14:12	RO	0x0	reserved
11:8	RW	0x0	usb3_sw_rd_latency_id Axi read channel id for latency AXI_PERFormance test
7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6:5	RW	0x0	usb3_sw_ddr_align_type 0: 16-Byte align 1: 32-Byte align 2: 64-Byte align 3: 128-Byte align
4	RW	0x0	usb3_sw_aw_cnt_id_type axi_perf counter id control 0: count all read channel id 1: count sw_ar_count_id read channel only
3	RW	0x0	usb3_sw_ar_cnt_id_type axi_perf counter id control 0: count all read channel id 1: count sw_ar_count_id read channel only
2	RW	0x0	usb3_sw_axi_cnt_type axi_perf counter type 0: axi transfer test 1: ddr align transfer test
1	RW	0x0	usb3_sw_axi_perf_clr Fi axi_perf clear bit 0: disable 1: enable
0	RW	0x0	usb3_sw_axi_perf_work axi_perf enable bit 0: disable 1: enable

GRF_USB3_PERF_CON1
Address: Operational Base + offset (0x02004)
usb3 performance monitor control register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:12	RO	0x0	reserved
11:0	RW	0x000	usb3_sw_rd_latency_thr Axi read channel id for latency AXI_PERFormance test

GRF_USB3_PERF_CON2
Address: Operational Base + offset (0x02008)
usb3 performance monitor control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:12	RO	0x0	reserved
11:8	RW	0x0	usb3_sw_aw_count_id When sw_aw_cnt_id_type=1, only count the id designated by sw_aw_count_id
7:4	RO	0x0	reserved

Bit	Attr	Reset Value	Description
3:0	RW	0x0	usb3_sw_ar_count_id When sw_ar_cnt_id_type=1, only count the id designated by sw_ar_count_id

GRF_USB3_PERF_RD_MAX_LATENCY_NUM
Address: Operational Base + offset (0x0200c)
usb3 performance monitor status register

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	rd_max_latency_r axi read max latency oaxi read max latency outpututput

GRF_USB3_PERF_RD_LATENCY_SAMP_NUM
Address: Operational Base + offset (0x02010)
usb3 performance monitor status register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rd_latency_samp_r AXI read latency total sample number

GRF_USB3_PERF_RD_LATENCY_ACC_NUM
Address: Operational Base + offset (0x02014)
usb3 performance monitor status register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rd_latency_acc_cnt_r AXI read latency (>sw_rd_latency_thr) total number

GRF_USB3_PERF_RD_AXI_TOTAL_BYTE
Address: Operational Base + offset (0x02018)
usb3 performance monitor status register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rd_axi_total_byte AXI active total read bytes/ddr align read bytes

GRF_USB3_PERF_WR_AXI_TOTAL_BYTE
Address: Operational Base + offset (0x0201c)
usb3 performance monitor status register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	wr_axi_total_byte AXI active total write bytes/ddr align write bytes

GRF_USB3_PERF_WORKING_CNT
Address: Operational Base + offset (0x02020)
usb3 performance monitor status register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	working_cnt_r working counter

GRF_USB3OTG0_CON0
Address: Operational Base + offset (0x02430)
USB3 OTG0 GRF Register0

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	host_u2_port_disable host_u2_port_disable USB2.0 Port Disable control. 0: Port Enabled 1: Port Disabled When 1, this signal stops reporting connect/disconnect events the port and keeps the port in disabled state.
14	RW	0x0	host_port_power_control_present host_port_power_control_present This indicates whether the host controller implementation includes port power control. 0: Indicates that the port does not have port power switches. 1: Indicates that the port has port power switches

Bit	Attr	Reset Value	Description
13:8	RW	0x20	fladj_30mhz_reg fladj_30mhz_reg HS Jitter Adjustment. Indicates the correction required to accommodate mac3 clock and utmi clock jitter to measure 125 's duration. With fladj_30mhz_reg tied to zero, the high speed 125us micro-frame is counted for 123933ns. You must program the value in terms of high speed bit times in a 30 MHz cycle. The default value that must be driven is 32 (assuming 30 MHz perfect clock).
7:6	RW	0x0	hub_port_perm_attach hub_port_perm_attach Indicates if the device attached to a downstream port is permanently attached or not. 0: Not permanently attached 1: Permanently attached Bit0 is for USB2.0 port and bit1 are for USB 3.0 SS port.
5:4	RW	0x0	hub_port_overcurrent hub_port_overcurrent This is the per port Overcurrent indication of the root-hub ports: 0: No Overcurrent 1: Overcurrent Bit0 is for USB 2.0 port and bit1 are for USB 3.0 SS port.

Bit	Attr	Reset Value	Description
3:0	RW	0x0	bus_filter_bypass bus_filter_bypass It is expected that this signal is set or reset at power-on reset and is not changed during the normal operation of the core. The function of each bit is: bus_filter_bypass[3]: Bypass the filter for utmiotg_iddig bus_filter_bypass[2]: Bypass the filters for utmisrp_bvalid and utmisrp_sessend bus_filter_bypass[1]: Bypass the filter for pipe3_PowerPresent all U3 ports bus_filter_bypass[0]: Bypass the filter for utmiotg_vbusvalid all U2 ports In non-OTG Host-only mode, internal bus filters are not needed. Values: 1'b0: Bus filter(s) enabled 1'b1: Bus filter(s) disabled (bypassed)

GRF_USB3OTG0_CON1
Address: Operational Base + offset (0x02434)
USB3 OTG0 GRF Register1

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:12	RW	0x1	host_u3_port host_u3_port xHCI usb3 port number, default as 1.

Bit	Attr	Reset Value	Description
11:8	RW	0x1	host_u2_port host_u2_port xHCI host USB2 Port number, default as 1.
7:6	RO	0x0	reserved
5	RW	0x0	host_legacy_smi_bar host_legacy_smi_bar Use this register to support SMI on BAR defined in xHCI spec. SW must set this register, then clear this register to indicate Base Address Register written
4	RW	0x0	host_legacy_smi_pci_cmd host_legacy_smi_pci_cmd Use this register to support SMI on PCI Command defined in xHCI spec. SW must set this register, then clear this register to indicate PCI command register written.
3:2	RO	0x0	reserved
1	RW	0x0	pme_en pme_en Enable signal for the pme_generation. Enable the core to assert pme_generation.
0	RW	0x0	host_u3_port_disable host_u3_port_disable USB 3.0 SS Port Disable control. 0: Port Enabled 1: Port Disabled

GRF_USB3OTG1_CON0
Address: Operational Base + offset (0x02440)
USB3 OTG1 GRF Register0

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	host_u2_port_disable host_u2_port_disable USB2.0 Port Disable control. 0: Port Enabled 1: Port Disabled When 1, this signal stops reporting connect/disconnect events the port and keeps the port in disabled state.
14	RW	0x0	host_port_power_control_present host_port_power_control_present This indicates whether the host controller implementation includes port power control. 0: Indicates that the port does not have port power switches. 1: Indicates that the port has port power switches
13:8	RW	0x20	fladj_30mhz_reg fladj_30mhz_reg HS Jitter Adjustment. Indicates the correction required to accommodate mac3 clock and utmi clock jitter to measure 125 's duration. With fladj_30mhz_reg tied to zero, the high speed 125us micro-frame is counted for 123933ns. You must program the value in terms of high speed bit times in a 30 MHz cycle. The default value that must be driven is 32 (assuming 30 MHz perfect clock).

Bit	Attr	Reset Value	Description
7:6	RW	0x0	hub_port_perm_attach hub_port_perm_attach Indicates if the device attached to a downstream port is permanently attached or not. 0: Not permanently attached 1: Permanently attached Bit0 is for USB2.0 port and bit1 are for USB 3.0 SS port.
5:4	RW	0x0	hub_port_overcurrent hub_port_overcurrent This is the per port Overcurrent indication of the root-hub ports: 0: No Overcurrent 1: Overcurrent Bit0 is for USB 2.0 port and bit1 are for USB 3.0 SS port.
3:0	RW	0x0	bus_filter_bypass bus_filter_bypass It is expected that this signal is set or reset at power-on reset and is not changed during the normal operation of the core. The function of each bit is: bus_filter_bypass[3]: Bypass the filter for utmiotg_iddig bus_filter_bypass[2]: Bypass the filters for utmisrp_bvalid and utmisrp_sessend bus_filter_bypass[1]: Bypass the filter for pipe3_PowerPresent all U3 ports bus_filter_bypass[0]: Bypass the filter for utmiotg_vbusvalid all U2 ports In non-OTG Host-only mode, internal bus filters are not needed. Values: 1'b0: Bus filter(s) enabled 1'b1: Bus filter(s) disabled (bypassed)

GRF_USB3OTG1_CON1
Address: Operational Base + offset (0x02444)
USB3 OTG1 GRF Register1

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:12	RW	0x1	host_u3_port host_u3_port xHCI usb3 port number, default as 1.
11:8	RW	0x1	host_u2_port host_u2_port xHCI host USB2 port number, default as 1.
7:6	RO	0x0	reserved
5	RW	0x0	host_legacy_smi_bar host_legacy_smi_bar Use this register to support SMI on BAR defined in xHCI spec. SW must set this register, then clear this register to indicate Base Address Register written
4	RW	0x0	host_legacy_smi_pci_cmd host_legacy_smi_pci_cmd Use this register to support SMI on PCI Command defined in xHCI spec. SW must set this register, then clear this register to indicate PCI command register written.
3:2	RO	0x0	reserved
1	RW	0x0	pme_en pme_en Enable signal for the pme_generation. Enable the core to assert pme_generation.

Bit	Attr	Reset Value	Description
0	RW	0x0	host_u3_port_disable host_u3_port_disable USB 3.0 SS Port Disable control. 0: Port Enabled 1: Port Disabled

GRF_USB3OTG0_STATUS_LAT0
Address: Operational Base + offset (0x02450)
USB3 OTG0 status register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	usbcphy0_otg_utmi_iddig status of usbcphy0_otg_utmi_iddig[31:0]

GRF_USB3OTG0_STATUS_LAT1
Address: Operational Base + offset (0x02454)
USB3 OTG1 status register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	usbcphy0_otg_utmi_iddig status of usbcphy0_otg_utmi_iddig[63:32]

GRF_USB3OTG0_STATUS_CB
Address: Operational Base + offset (0x02458)
USB3 OTG0 status register

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x000	usb3otg0_host_current_belt status of usb3otg0_host_current_belt

GRF_USB3OTG1_STATUS_LAT0
Address: Operational Base + offset (0x02460)
USB3 OTG1 status register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	usbcphy1_otg_utmi_iddig status of usbcphy1_otg_utmi_iddig[31:0]

GRF_USB3OTG1_STATUS_LAT1
Address: Operational Base + offset (0x02464)
USB3 OTG1 status register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	usbcphy1_otg_utmi_iddig status of usbcphy1_otg_utmi_iddig[63:32]

GRF_USB3OTG1_STATUS_CB
Address: Operational Base + offset (0x02468)

USB3 OTG1 status register

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x000	usb3otg1_host_current_belt status of usb3otg1_host_current_belt

GRF_PCIE_PERF_CON0

Address: Operational Base + offset (0x04000)

pcie performance monitor control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:13	RO	0x0	reserved
12:8	RW	0x00	pcie_sw_rd_latency_id Axi read channel id for latency AXI_PERFormance test
7	RO	0x0	reserved
6:5	RW	0x0	pcie_sw_ddr_align_type 0: 16-Byte align 1: 32-Byte align 2: 64-Byte align 3: 128-Byte align
4	RW	0x0	pcie_sw_aw_cnt_id_type 0: count all write channels 1: count sw_aw_count_id write channel only
3	RW	0x0	pcie_sw_ar_cnt_id_type axi_perf counter id control 0: count all read channel id 1: count sw_ar_count_id read channel only
2	RW	0x0	pcie_sw_axi_cnt_type axi_perf counter type 0: axi transfer test 1: ddr align transfer test

Bit	Attr	Reset Value	Description
1	RW	0x0	pcie_sw_axi_perf_clr axi_perf clear bit 0: disable 1: enable
0	RW	0x0	pcie_sw_axi_perf_work axi_perf enable bit 0: disable 1: enable

GRF_PCIE_PERF_CON1
Address: Operational Base + offset (0x04004)
pcie performance monitor control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:12	RO	0x0	reserved
11:0	RW	0x000	pcie_sw_rd_latency_thr Axi read channel id for latency AXI_PERFormance test

GRF_PCIE_PERF_CON2
Address: Operational Base + offset (0x04008)
pcie performance monitor control register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:13	RO	0x0	reserved
12:8	RW	0x00	pcie_sw_aw_count_id When sw_aw_cnt_id_type=1, only count the id designated by sw_aw_count_id
7:5	RO	0x0	reserved
4:0	RW	0x00	pcie_sw_ar_count_id When sw_ar_cnt_id_type=1, only count the id designated by sw_ar_count_id

GRF_PCIE_PERF_RD_MAX_LATENCY_NUM
Address: Operational Base + offset (0x0400c)
pcieperformance monitor status register

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	rd_max_latency_r axi read max latency output

GRF_PCIE_PERF_RD_LATENCY_SAMP_NUM
Address: Operational Base + offset (0x04010)
pcie performance monitor status register

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:0	RW	0x0000000	rd_latency_samp_r AXI read latency total sample number

GRF_PCIE_PERF_RD_LATENCY_ACC_NUM
Address: Operational Base + offset (0x04014)
pcie performance monitor status register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rd_latency_acc_cnt_r AXI read latency (>sw_rd_latency_thr) total number

GRF_PCIE_PERF_RD_AXI_TOTAL_BYTE
Address: Operational Base + offset (0x04018)
pcie performance monitor status register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rd_axi_total_byte AXI active total read bytes/ddr align read bytes

GRF_PCIE_PERF_WR_AXI_TOTAL_BYTE
Address: Operational Base + offset (0x0401c)
pcie performance monitor status register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	wr_axi_total_byte AXI active total write bytes/ddr align write bytes

GRF_PCIE_PERF_WORKING_CNT
Address: Operational Base + offset (0x04020)
pcie performance monitor status register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	working_cnt_r working counter

GRF_USB20_HOST0_CON0
Address: Operational Base + offset (0x04100)
USB20 Host0 GRF register0

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RO	0x0	reserved
13	RW	0x1	word_if word_if 1: select 16bit utmi interface 0: select 8bit utmi interface Note: usb2phy only support 16bit interface.
12	RW	0x0	sim_mode sim_mode Simulation only.
11	RW	0x0	ohci_susp_lgcy ohci_susp_lgcy
10	RW	0x0	ohci_cntsel ohci_cntsel
9	RW	0x1	ohci_clkcktrst ohci_clkcktrst

Bit	Attr	Reset Value	Description
8	RW	0x1	incrx_en incrx_en Forces AHB master to start INCR4/8/16 busts only on burst boundaries. AHB requires that double word width burst be addressed-aligned only to the double-word boundary. 1'b1: Start INCRX burst only on burst x-aligned addresses 1'b0: Normal AHB operation; start bursts on any double word boundary Note: When this function is enabled, the burst are started only when the lowest bits of haddr are: INCR4: haddr[3:0] == 4'b0000 INCR8: haddr[4:0] == 5'b00000 INCR16: haddr[5:0] == 6'b000000
7	RW	0x1	incr8_en incr8_en 1: enable AHB INCR8 burst 0: disable AHB INCR8 burst
6	RW	0x1	incr4_en incr4_en 1: enable AHB INCR4 burst 0: disable AHB INCR4 burst
5	RW	0x1	incr16_en incr16_en 1: enable AHB INCR16 burst 0: disable AHB INCR16 burst
4	RW	0x0	hubsetup_min hubsetup_min
3	RW	0x0	autoppd_on_overcur_en autoppd_on_overcur_en
2	RW	0x0	arb_pause arb_pause
1	RW	0x0	app_start_clk app_start_clk
0	RW	0x0	app_prt_ovrcur app_prt_ovrcur

GRF_USB20_HOST0_CON1

Address: Operational Base + offset (0x04104)
USB20 Host0 GRF register1

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:12	RO	0x0	reserved
11:6	RW	0x20	fladj_val_common fladj_val_common Must set this register to 0x20.
5:0	RW	0x20	fladj_val fladj_val Must set this register to 0x20.

GRF_USB20_HOST1_CON0
Address: Operational Base + offset (0x04110)
USB20 Host1 GRF register0

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13	RW	0x1	word_if word_if 1: select 16bit utmi interface 0: select 8bit utmi interface Note: usb2phy only support 16bit interface.
12	RW	0x0	sim_mode sim_mode Simulation only.
11	RW	0x0	ohci_susp_lgcy ohci_susp_lgcy
10	RW	0x0	ohci_cntsel ohci_cntsel
9	RW	0x1	ohci_clkcktrst ohci_clkcktrst
8	RW	0x1	incrx_en incrx_en Forces AHB master to start INCR4/8/16 busts only on burst boundaries. AHB requires that double word width burst be addressed-aligned only to the double-word boundary. 1'b1: Start INCRX burst only on burst x-aligned addresses 1'b0: Normal AHB operation; start bursts on any double word boundary Note: When this function is enabled, the burst are started only when the lowest bits of haddr are: INCR4: haddr[3:0] == 4'b0000 INCR8: haddr[4:0] == 5'b00000 INCR16: haddr[5:0] == 6'b000000
7	RW	0x1	incr8_en incr8_en 1: enable AHB INCR8 burst 0: disable AHB INCR8 burst
6	RW	0x1	incr4_en incr4_en 1: enable AHB INCR4 burst 0: disable AHB INCR4 burst
5	RW	0x1	incr16_en incr16_en 1: enable AHB INCR16 burst 0: disable AHB INCR16 burst

Bit	Attr	Reset Value	Description
4	RW	0x0	hubsetup_min hubsetup_min
3	RW	0x0	autoppd_on_overcur_en autoppd_on_overcur_en
2	RW	0x0	arb_pause arb_pause
1	RW	0x0	app_start_clk app_start_clk
0	RW	0x0	app_prt_ovrcur app_prt_ovrcur

GRF_USB20_HOST1_CON1
Address: Operational Base + offset (0x04114)
USB20 Host1 GRF register1

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:12	RO	0x0	reserved
11:6	RW	0x20	fladj_val_common fladj_val_common Must set this register to 0x20.
5:0	RW	0x20	fladj_val fladj_val Must set this register to 0x20.

GRF_HSIC_CON0
Address: Operational Base + offset (0x04120)

HSIC controller GRF register 0

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:10	RO	0x0	reserved
9	RW	0x1	hsic_word_if word_if 1: select 16bit utmi interface 0: select 8bit utmi interface Note: HSICPHY only support 16bit utmi interface.
8	RW	0x0	hsic_sim_mode sim_mode Simulation only.
7	RW	0x1	hsic_incrx_en Burst Alignment Enable Forces AHB master to start INCR4/8/16 busts only on burst boundaries. AHB requires that double word width burst be addressed-aligned only to the double-word boundary. 1'b1: Start INCRX burst only on burst x-aligned addresses 1'b0: Normal AHB operation; start bursts on any double word boundary Note: When this function is enabled, the burst are started only when the lowest bits of haddr are: INCR4: haddr[3:0] == 4'b0000 INCR8: haddr[4:0] == 5'b00000 INCR16: haddr[5:0] == 6'b000000
6	RW	0x1	hsic_incr8_en incr8_en 1: enable AHB INCR8 burst 0: disable AHB INCR8 burst

Bit	Attr	Reset Value	Description
5	RW	0x1	hsic_incr4_en incr4_en 1: enable AHB INCR4 burst 0: disable AHB INCR4 burst
4	RW	0x1	hsic_incr16_en incr16_en 1: enable AHB INCR16 burst 0: disable AHB INCR16 burst
3	RW	0x0	hsic_hubsetup_min hubsetup_min
2	RW	0x0	hsic_autoppd_on_overcur autoppd_on_overcur
1	RW	0x0	hsic_app_start_clk app_start_clk
0	RW	0x0	hsic_app_prt_ovrcur app_prt_ovrcur

GRF_HSIC_CON1
Address: Operational Base + offset (0x04124)
HSIC controller GRF register1

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12	RW	0x0	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
11:6	RW	0x20	hsic_fladj_val_common fladj_val_common Must set this register to 0x20

Bit	Attr	Reset Value	Description
5:0	RW	0x20	hsic_fladj fladj Must set this register to 0x20.

GRF_GRF_USBHOST0_STATUS
Address: Operational Base + offset (0x04140)
usb host0 controller status register

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	host0_ehci_bufacc
27	RW	0x0	host0_ehci_xfer_prdc
26	RW	0x0	host0_ohci_bufacc
25	RW	0x0	host0_ohci_ccs
24	RW	0x0	host0_ohci_drwe
23	RW	0x0	host0_ohci_globalsuspend
22	RW	0x0	host0_ohci_rmtwkp
21	RW	0x0	host0_ohci_rwe
20:17	RW	0x0	host0_ehci_lpsmc_state
16:11	RW	0x00	host0_ehci_usbsts
10:0	RW	0x000	host0_ehci_xfer_cnt

GRF_GRF_USBHOST1_STATUS
Address: Operational Base + offset (0x04144)
usb host1 controller status register

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28	RW	0x0	host1_ehci_bufacc
27	RW	0x0	host1_ehci_xfer_prdc
26	RW	0x0	host1_ohci_bufacc
25	RW	0x0	host1_ohci_ccs

Bit	Attr	Reset Value	Description
24	RW	0x0	host1_ohci_drwe
23	RW	0x0	host1_ohci_globalsuspend
22	RW	0x0	host1_ohci_rmtwkp
21	RW	0x0	host1_ohci_rwe
20:17	RW	0x0	host1_ehci_lpsmc_state
16:11	RW	0x00	host1_ehci_usbsts
10:0	RW	0x000	host1_ehci_xfer_cnt

GRF_GRF_HSIC_STATUS
Address: Operational Base + offset (0x04148)
hsic controller status register

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21	RW	0x0	hsic_ehci_xfer_prdc
20:17	RW	0x0	hsic_ehci_lpsms_state
16:11	RW	0x00	hsic_ehci_usbsts
10:0	RW	0x000	hsic_ehci_xfer_cnt

GRF_HSICPHY_CON0
Address: Operational Base + offset (0x04470)
HSICPHY GRF control register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:9	RO	0x0	reserved
8	RW	0x0	hsicphy_soft_con_sel soft_con_sel 1: soft control select utmi signals from GRF to HSIC PHY 0: soft control select utmi signals from HSIC controller to HSIC PHY
7:6	RW	0x1	i_hsic_utmi_xcvrselect utmi_xcvrselect select the value of this register to xcvrselect port of HSIC PHY when soft_con_sel=1.
5:4	RW	0x0	i_hsic_utmi_opmode utmi_opmode select the value of this register to opmode port of HSIC PHY when soft_con_sel=1
3	RW	0x1	i_hsic_utmi_termselect utmi_termselect select the value of this register to termselect port of HSIC PHY when soft_con_sel=1
2	RW	0x1	i_hsic_utmi_suspend_n utmi_suspend_n select the value of this register to ususpend_n port of HSIC PHY when soft_con_sel=1
1	RW	0x1	hsicphy_utmi_dmpulldown utmi_dmpulldown 1:DM pull down resistor enable 0:DM pull down resistor disable

Bit	Attr	Reset Value	Description
0	RW	0x1	hsicphy_utmi_dppulldown utmi_dppulldown 1:DP pull down resistor enable 0:DP pull down resistor disable

GRF_usbphy0_ctrl0
Address: Operational Base + offset (0x04480)
usbphy0_ctrl0

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x850f	usbphy_ctrl0 usbphy_ctrl0 Bit0~15 of usbphy_ctrl register

GRF_usbphy0_ctrl1
Address: Operational Base + offset (0x04484)
usbphy0_ctrl1

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0xe007	usbphy_ctrl1 usbphy_ctrl1 Bit16~31 of usbphy_ctrl register

GRF_usbphy0_ctrl2
Address: Operational Base + offset (0x04488)
usbphy0_ctrl2

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x82e7	usbphy_ctrl2 usbphy_ctrl2 Bit32~47 of usbphy_ctrl register

GRF_usbphy0_ctrl3
Address: Operational Base + offset (0x0448c)
usbphy0_ctrl3

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x02a2	usbphy_ctrl3 usbphy_ctrl3 Bit48~63 of usbphy_ctrl register

GRF_usbphy0_ctrl4
Address: Operational Base + offset (0x04490)
usbphy0_ctrl4

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x5554	usbphy_ctrl4 usbphy_ctrl4 Bit64~79 of usbphy_ctrl register

GRF_usbphy0_ctrl5
Address: Operational Base + offset (0x04494)
usbphy0_ctrl5

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x4555	usbphy_ctrl5 usbphy_ctrl5 Bit80~95 of usbphy_ctrl register

GRF_usbphy0_ctrl6
Address: Operational Base + offset (0x04498)
usbphy0_ctrl6

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0005	usbphy_ctrl6 usbphy_ctrl6 Bit96~111 of usbphy_ctrl register

GRF_usbphy0_ctrl7
Address: Operational Base + offset (0x0449c)
usbphy0_ctrl7

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x68c8	usbphy_ctrl7 usbphy_ctrl7 Bit112~127 of usbphy_ctrl register

GRF_usbphy0_ctrl8
Address: Operational Base + offset (0x044a0)
usbphy0_ctrl8

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0000	usbphy_ctrl8 usbphy_ctrl8 Bit128~143 of usbphy_ctrl register

GRF_usbphy0_ctrl9
Address: Operational Base + offset (0x044a4)
usbphy0_ctrl9

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0000	usbphy_ctrl9 usbphy_ctrl9 Bit144~159 of usbphy_ctrl register

GRF_usbphy0_ctrl10
Address: Operational Base + offset (0x044a8)
usbphy0_ctrl10

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0000	usbphy_ctrl10 usbphy_ctrl10 Bit160~175 of usbphy_ctrl register

GRF_usbphy0_ctrl11
Address: Operational Base + offset (0x044ac)
usbphy0_ctrl11

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0000	usbphy_ctrl11 usbphy_ctrl11 Bit176~191 of usbphy_ctrl register

GRF_usbphy0_ctrl12
Address: Operational Base + offset (0x044b0)
usbphy0_ctrl12

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x00a1	usbphy_ctrl12 usbphy_ctrl12 Bit192~207 of usbphy_ctrl register

GRF_usbphy0_ctrl13
Address: Operational Base + offset (0x044b4)
usbphy0_ctrl13

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x850f	usbphy_ctrl13 usbphy_ctrl13 Bit208~223 of usbphy_ctrl register

GRF_usbphy0_ctrl14
Address: Operational Base + offset (0x044b8)
usbphy0_ctrl14

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0xe007	usbphy_ctrl14 usbphy_ctrl14 Bit224~239 of usbphy_ctrl register

GRF_usbphy0_ctrl15
Address: Operational Base + offset (0x044bc)
usbphy0_ctrl15

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x02e7	usbphy_ctrl15 usbphy_ctrl15 Bit240~255 of usbphy_ctrl register

GRF_usbphy0_ctrl16
Address: Operational Base + offset (0x044c0)
usbphy0_ctrl16

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0200	usbphy_ctrl16 usbphy_ctrl16 Bit256~271 of usbphy_ctrl register

GRF_usbphy0_ctrl17
Address: Operational Base + offset (0x044c4)
usbphy0_ctrl17

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x5554	usbphy_ctrl17 usbphy_ctrl17 Bit272~287 of usbphy_ctrl register

GRF_usbphy0_ctrl18
Address: Operational Base + offset (0x044c8)
usbphy0_ctrl18

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x4555	usbphy_ctrl18 usbphy_ctrl18 Bit288~303 of usbphy_ctrl register

GRF_usbphy0_ctrl19
Address: Operational Base + offset (0x044cc)
usbphy0_ctrl19

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0005	usbphy_ctrl19 usbphy_ctrl19 Bit304~319 of usbphy_ctrl register

GRF_usbphy0_ctrl20
Address: Operational Base + offset (0x044d0)
usbphy0_ctrl20

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x68c8	usbphy_ctrl20 usbphy_ctrl20 Bit320~335 of usbphy_ctrl register

GRF_usbphy0_ctrl21
Address: Operational Base + offset (0x044d4)
usbphy0_ctrl21

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0000	usbphy_ctrl21 usbphy_ctrl21 Bit336~351 of usbphy_ctrl register

GRF_usbphy0_ctrl22
Address: Operational Base + offset (0x044d8)
usbphy0_ctrl22

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0000	usbphy_ctrl22 usbphy_ctrl22 Bit352~367 of usbphy_ctrl register

GRF_usbphy0_ctrl23
Address: Operational Base + offset (0x044dc)
usbphy0_ctrl23

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0000	usbphy_ctrl23 usbphy_ctrl23 Bit368~383 of usbphy_ctrl register

GRF_usbphy0_ctrl24
Address: Operational Base + offset (0x044e0)
usbphy0_ctrl24

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0000	usbphy_ctrl24 usbphy_ctrl24 Bit384~399 of usbphy_ctrl register

GRF_usbphy0_ctrl25
Address: Operational Base + offset (0x044e4)
usbphy0_ctrl25

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0021	usbphy_ctrl25 usbphy_ctrl25 Bit400~415 of usbphy_ctrl register

GRF_usbphy1_ctrl0
Address: Operational Base + offset (0x04500)
usbphy1_ctrl0

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x850f	usbphy_ctrl0 usbphy_ctrl0 Bit0~15 of usbphy_ctrl register

GRF_usbphy1_ctrl1
Address: Operational Base + offset (0x04504)
usbphy1_ctrl1

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0xe007	usbphy_ctrl1 usbphy_ctrl1 Bit16~31 of usbphy_ctrl register

GRF_usbphy1_ctrl2
Address: Operational Base + offset (0x04508)
usbphy1_ctrl2

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x82e7	usbphy_ctrl2 usbphy_ctrl2 Bit32~47 of usbphy_ctrl register

GRF_usbphy1_ctrl3
Address: Operational Base + offset (0x0450c)
usbphy1_ctrl3

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x02a2	usbphy_ctrl3 usbphy_ctrl3 Bit48~63 of usbphy_ctrl register

GRF_usbphy1_ctrl4
Address: Operational Base + offset (0x04510)
usbphy1_ctrl4

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x5554	usbphy_ctrl4 usbphy_ctrl4 Bit64~79 of usbphy_ctrl register

GRF_usbphy1_ctrl5
Address: Operational Base + offset (0x04514)
usbphy1_ctrl5

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x4555	usbphy_ctrl5 usbphy_ctrl5 Bit80~95 of usbphy_ctrl register

GRF_usbphy1_ctrl6
Address: Operational Base + offset (0x04518)
usbphy1_ctrl6

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0005	usbphy_ctrl6 usbphy_ctrl6 Bit96~111 of usbphy_ctrl register

GRF_usbphy1_ctrl7
Address: Operational Base + offset (0x0451c)
usbphy1_ctrl7

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x68c8	usbphy_ctrl7 usbphy_ctrl7 Bit112~127 of usbphy_ctrl register

GRF_usbphy1_ctrl8
Address: Operational Base + offset (0x04520)
usbphy1_ctrl8

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0000	usbphy_ctrl8 usbphy_ctrl8 Bit128~143 of usbphy_ctrl register

GRF_usbphy1_ctrl9
Address: Operational Base + offset (0x04524)
usbphy1_ctrl9

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0000	usbphy_ctrl9 usbphy_ctrl9 Bit144~159 of usbphy_ctrl register

GRF_usbphy1_ctrl10
Address: Operational Base + offset (0x04528)
usbphy1_ctrl10

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0000	usbphy_ctrl10 usbphy_ctrl10 Bit160~175 of usbphy_ctrl register

GRF_usbphy1_ctrl11
Address: Operational Base + offset (0x0452c)
usbphy1_ctrl11

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0000	usbphy_ctrl11 usbphy_ctrl11 Bit176~191 of usbphy_ctrl register

GRF_usbphy1_ctrl12
Address: Operational Base + offset (0x04530)
usbphy1_ctrl12

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x00a1	usbphy_ctrl12 usbphy_ctrl12 Bit192~207 of usbphy_ctrl register

GRF_usbphy1_ctrl13
Address: Operational Base + offset (0x04534)
usbphy1_ctrl13

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x850f	usbphy_ctrl13 usbphy_ctrl13 Bit208~223 of usbphy_ctrl register

GRF_usbphy1_ctrl14
Address: Operational Base + offset (0x04538)
usbphy1_ctrl14

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0xe007	usbphy_ctrl14 usbphy_ctrl14 Bit224~239 of usbphy_ctrl register

GRF_usbphy1_ctrl15
Address: Operational Base + offset (0x0453c)
usbphy1_ctrl15

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x02e7	usbphy_ctrl15 usbphy_ctrl15 Bit240~255 of usbphy_ctrl register

GRF_usbphy1_ctrl16
Address: Operational Base + offset (0x04540)
usbphy1_ctrl16

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0200	usbphy_ctrl16 usbphy_ctrl16 Bit256~271 of usbphy_ctrl register

GRF_usbphy1_ctrl17
Address: Operational Base + offset (0x04544)
usbphy1_ctrl17

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x5554	usbphy_ctrl17 usbphy_ctrl17 Bit272~287 of usbphy_ctrl register

GRF_usbphy1_ctrl18
Address: Operational Base + offset (0x04548)
usbphy1_ctrl18

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x4555	usbphy_ctrl18 usbphy_ctrl18 Bit288~303 of usbphy_ctrl register

GRF_usbphy1_ctrl19
Address: Operational Base + offset (0x0454c)
usbphy1_ctrl19

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0005	usbphy_ctrl19 usbphy_ctrl19 Bit304~319 of usbphy_ctrl register

GRF_usbphy1_ctrl20
Address: Operational Base + offset (0x04550)
usbphy1_ctrl20

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x68c8	usbphy_ctrl20 usbphy_ctrl20 Bit320~335 of usbphy_ctrl register

GRF_usbphy1_ctrl21
Address: Operational Base + offset (0x04554)
usbphy1_ctrl21

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0000	usbphy_ctrl21 usbphy_ctrl21 Bit336~351 of usbphy_ctrl register

GRF_usbphy1_ctrl22
Address: Operational Base + offset (0x04558)
usbphy1_ctrl22

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0000	usbphy_ctrl22 usbphy_ctrl22 Bit352~367 of usbphy_ctrl register

GRF_usbphy1_ctrl23
Address: Operational Base + offset (0x0455c)
usbphy1_ctrl23

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0000	usbphy_ctrl23 usbphy_ctrl23 Bit368~383 of usbphy_ctrl register

GRF_usbphy1_ctrl24
Address: Operational Base + offset (0x04560)
usbphy1_ctrl24

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0000	usbphy_ctrl24 usbphy_ctrl24 Bit384~399 of usbphy_ctrl register

GRF_usbphy1_ctrl25
Address: Operational Base + offset (0x04564)
usbphy1_ctrl25

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0021	usbphy_ctrl25 usbphy_ctrl25 Bit400~415 of usbphy_ctrl register

GRF_HDCP22_PERF_CON0
Address: Operational Base + offset (0x06000)
hdcp performance monitor control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:12	RO	0x0	reserved
11:8	RW	0x0	hdcp22_sw_rd_latency_id Axi read channel id for latency AXI_PERFormance test
7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6:5	RW	0x0	hdcp22_sw_ddr_align_type 0: 16-Byte align 1: 32-Byte align 2: 64-Byte align 3: 128-Byte align
4	RW	0x0	hdcp22_sw_aw_cnt_id_type 0: count all write channels 1: count sw_aw_count_id write channel only
3	RW	0x0	hdcp22_sw_ar_cnt_id_type axi_perf counter id control 0: count all read channel id 1: count sw_ar_count_id read channel only
2	RW	0x0	hdcp22_sw_axi_cnt_type axi_perf counter type 0: axi transfer test 1: ddr align transfer test
1	RW	0x0	hdcp22_sw_axi_perf_clr axi_perf clear bit 0: disable 1: enable
0	RW	0x0	hdcp22_sw_axi_perf_work axi_perf enable bit 0: disable 1: enable

GRF_HDCP22_PERF_CON1
Address: Operational Base + offset (0x06004)
hdcp performance monitor control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:12	RO	0x0	reserved

Bit	Attr	Reset Value	Description
11:0	RW	0x000	hdcp22_sw_rd_latency_thr Axi Read latency threshold

GRF_HDCP22_PERF_CON2
Address: Operational Base + offset (0x06008)
hdcp performance monitor control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RO	0x0	reserved
7:4	RW	0x0	hdcp22_sw_aw_count_id When sw_aw_cnt_id_type=1, only count the id designated by sw_aw_count_id
3:0	RW	0x0	hdcp22_sw_ar_count_id When sw_ar_cnt_id_type=1, only count the id designated by sw_ar_count_id

GRF_HDCP22_PERF_RD_MAX_LATENCY_NUM
Address: Operational Base + offset (0x0600c)
hdcp performance monitor status register

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	rd_max_latency_r axi read max latency output

GRF_HDCP22_PERF_RD_LATENCY_SAMP_NUM
Address: Operational Base + offset (0x06010)
hdcp performance monitor status register

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:0	RW	0x0000000	rd_latency_samp_r AXI read latency total sample number

GRF_HDCP22_PERF_RD_LATENCY_ACC_NUM
Address: Operational Base + offset (0x06014)
hdcp performance monitor status register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rd_latency_acc_cnt_r AXI read latency (>sw_rd_latency_thr) total number

GRF_HDCP22_PERF_RD_AXI_TOTAL_BYTE
Address: Operational Base + offset (0x06018)
hdcp performance monitor status register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rd_axi_total_byte AXI active total read bytes/ddr align read bytes

GRF_HDCP22_PERF_WR_AXI_TOTAL_BYTE
Address: Operational Base + offset (0x0601c)
hdcp performance monitor status register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	wr_axi_total_byte AXI active total write bytes/ddr align write bytes

GRF_HDCP22_PERF_WORKING_CNT
Address: Operational Base + offset (0x06020)
hdcp performance monitor status register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	working_cnt_r working counter

GRF_SOC_CON9
Address: Operational Base + offset (0x06224)
SoC control register 9

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	dsi0_dpiupdatecfg DSI host0 dpiupdatecfg bit control
14	RW	0x0	dsi0_dpishutdn DSI0 dpishutdn bit control
13	RW	0x0	dsi0_dpicolorm DSI0 dpicolorm bit control
12	RW	0x0	dp_lcdc_sel dp lcdc select 1'b0: vop big 1'b1: vop little
11	RW	0x0	dphy_rx1_clk_inv_sel dphy rx1 clock inveter select bit
10	RW	0x0	dphy_rx0_clk_inv_sel dphy rx0 clock inveter select bit
9	RW	0x0	disable_isp1 isp1 disable control
8	RW	0x0	disable_isp0 isp0 disable control
7:4	RO	0x0	reserved
3:0	RW	0x0	dphy_rx0_turnrequest dphy rx0 runrequest port control

GRF_SOC_CON20

Address: Operational Base + offset (0x06250)

SoC control register 20

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RO	0x0	reserved
14	RW	0x0	hdcp_i2c_force_sda hdcp_i2c_force_sda bit control
13	RW	0x0	hdcp_i2c_force_scl hdcp_i2c_force_scl control
12	RW	0x0	grf_vop_rgb_dclk_rev_sel dclk phase selct 0: 0 degree 1: 180 degree
11	RW	0x0	grf_con_rgb_lcdc_sel vop select 1'b0: vop big 1'b1: vop little
10	RO	0x0	reserved
9	RW	0x1	pclkin_dvp_rev_sel pclkin dvp clock select 0: not invet phase 1: invert phase
8	RW	0x0	edp_video_bist_en edp video bist enable 1: enable 0: disable
7	RW	0x0	vop_finish_sel vop finish select 1'b0: vop big 1'b1: vop little

Bit	Attr	Reset Value	Description
6	RW	0x1	hdmi_lcdc_sel hdmi lcdc select 1'b0: vop big 1'b1: vop little
5	RW	0x0	edp_lcdc_sel edp lcdc select 1'b0: vop big 1'b1: vop little
4	RW	0x0	dsi1_lcdc_sel dsi1 lcdc select 1'b0: vop big 1'b1: vop little
3	RW	0x1	dsi1_dpiupdatecfg dsi1 dpiupdatecfg bit control
2	RW	0x0	dsi1_dpishutdn dsi1 dpishutdn bit control
1	RW	0x0	dsi1_dpicolorm dsi1 dpicolorm bit control
0	RW	0x1	dsi0_lcdc_sel dsi0 vol select bit 1'b0: vop big 1'b1: vop little

GRF_SOC_CON21
Address: Operational Base + offset (0x06254)
SoC control register 21

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:12	RW	0x0	dphy_rx0_turndisable dphy_rx0_turndisable bit control

Bit	Attr	Reset Value	Description
11:8	RW	0x2	dphy_rx0_forcetxstopmode dphy_rx0_forcetxstopmode bit control
7:4	RW	0xc	dphy_rx0_forcerxmode dphy_rx0_forcerxmode bit control
3:0	RW	0xb	dphy_rx0_enable dphy_rx0_enable bit control

GRF_SOC_CON22
Address: Operational Base + offset (0x06258)
SoC control register 22

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:12	RW	0x1	dphy_tx0_turnrequest dphy_tx0_turnrequest bit control
11:8	RW	0x0	dphy_tx0_turndisable dphy_tx0_turndisable bit control
7:4	RW	0xc	dphy_tx0_forcetxstopmode dphy_tx0_forcetxstopmode bit control
3:0	RW	0xb	dphy_tx0_forcerxmode dphy_tx0_forcerxmode bit control

GRF_SOC_CON23
Address: Operational Base + offset (0x0625c)
SoC control register 23

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:12	RW	0x0	dphy_tx1rx1_turndisable dphy_tx1rx1_turndisable bit control
11:8	RW	0x0	dphy_tx1rx1_forcetxstopmode dphy_tx1rx1_forcetxstopmode bit control
7:4	RW	0x2	dphy_tx1rx1_forcerxmode dphy_tx1rx1_forcerxmode bit control
3:0	RW	0x1	dphy_tx1rx1_enable dphy_tx1rx1_enable bit control

GRF_SOC_CON24
Address: Operational Base + offset (0x06260)
SoC control register 24

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

Bit	Attr	Reset Value	Description
15:14	RW	0x0	vopl_dsi_ite_sel vopl_dsi_ite_sel bit control 0: mipi_dsi0_edpite 1: mipi_dsi1_edpite 2: 0 3: 1
13:12	RW	0x3	vopb_dsi_ite_sel vopb_dsi_ite_sel bit control 0: mipi_dsi0_edpite 1: mipi_dsi1_edpite 2: 0 3: 1
11:10	RW	0x2	vopl_dsi_halt_sel vopl_dsi_halt_sel bit control 0: mipi_dsi0_edpihalt 1: mipi_dsi0_edpihalt 2: low 3: high
9:8	RW	0x1	vopb_dsi_halt_sel vopb_dsi_halt_sel bit control 0: mipi_dsi0_edpihalt 1: mipi_dsi0_edpihalt 2: low 3: high
7	RW	0x1	dphy_tx1rx1_masterslavez dphy_tx1rx1_masterslavez bit control
6	RW	0x1	dphy_tx1rx1_enableclk dphy_tx1rx1_enableclk bit control
5	RW	0x1	dphy_tx1rx1_basedir dphy_tx1rx1_basedir bit control
4	RW	0x1	dphy_rx1_src_sel dphy_rx1_src_sel bit control
3:0	RW	0x0	dphy_tx1tx1_turnrequest dphy_tx1tx1_turnrequest bit control

GRF_SOC_CON25
Address: Operational Base + offset (0x06264)
SoC control register 25

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:12	RW	0xd	edp_tx_bscan_data edp_tx_bscan_data bit control
11	RW	0x0	edp_ref_clk_sel edp_ref_clk_sel bit control
10	RW	0x1	dphy_rx0_tsetclr dphy_rx0_tsetclr bit control
9	RW	0x0	dphy_rx0_tsetclk dphy_rx0_tsetclk bit control
8	RW	0x0	dphy_rx0_tseten dphy_rx0_tseten bit control
7:0	RW	0x5b	dphy_rx0_tsetdin dphy_rx0_tsetdin bit control

GRF_SOC_CON26

Address: Operational Base + offset (0x06268)

SoC control register 26

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RO	0x0	reserved
13:12	RW	0x0	dptx_hpd_sel dptx_hpd_sel bit control
11:9	RO	0x0	reserved
8	RW	0x1	force_dp_xt_ocdhaltonreset force_dp_xt_ocdhaltonreset bit control
7:4	RW	0x1	dptx_lane_sel dptx_lane_sel bit control
3	RW	0x0	uphy_dp_sel uphy_dp_sel bit control
2	RW	0x0	hdcp22_src_sel hdcp22_src_sel bit control
1	RO	0x0	reserved
0	RW	0x0	edp_tx_bscan_en edp_tx_bscan_en bit control

GRF_GPU_PERF_CON0

Address: Operational Base + offset (0x08000)

gpu performance monitor control register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RO	0x0	reserved
13:8	RW	0x00	gpu_sw_rd_latency_id Axi read channel id for latency AXI_PERFormance test
7	RO	0x0	reserved
6:5	RW	0x0	gpu_sw_ddr_align_type 0: 16-Byte align 1: 32-Byte align 2: 64-Byte align 3: 128-Byte align
4	RW	0x0	gpu_sw_aw_cnt_id_type axi_perf counter id control 0: count all write channel id 1: count sw_ar_count_id write channel only
3	RW	0x0	gpu_sw_ar_cnt_id_type axi_perf counter id control 0: count all read channel id 1: count sw_ar_count_id read channel only
2	RW	0x0	gpu_sw_axi_cnt_type axi_perf counter type 0: axi transfer test 1: ddr align transfer test
1	RW	0x0	gpu_sw_axi_perf_clr axi_perf clear bit 0: disable 1: enable
0	RW	0x0	gpu_sw_axi_perf_work axi_perf enable bit 0: disable 1: enable

GRF_GPU_PERF_CON1
Address: Operational Base + offset (0x08004)
gpu performance monitor control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:12	RO	0x0	reserved
11:0	RW	0x000	gpu_sw_rd_latency_thr Axi read channel id for latency AXI_PERFormance test

GRF_GPU_PERF_CON2
Address: Operational Base + offset (0x08008)
gpu performance monitor control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:13	RO	0x0	reserved

Bit	Attr	Reset Value	Description
12:8	RW	0x00	gpu_sw_aw_count_id When sw_aw_cnt_id_type=1, only count the id designated by sw_aw_count_id
7:5	RO	0x0	reserved
4:0	RW	0x00	gpu_sw_ar_count_id When sw_ar_cnt_id_type=1, only count the id designated by sw_ar_count_id

GRF_GPU_PERF_RD_MAX_LATENCY_NUM
Address: Operational Base + offset (0x0800c)
gpu performance monitor status register

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	rd_max_latency_r axi read max latency output

GRF_GPU_PERF_RD_LATENCY_SAMP_NUM
Address: Operational Base + offset (0x08010)
gpu performance monitor status register

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:0	RW	0x0000000	rd_latency_samp_r AXI read latency total sample number

GRF_GPU_PERF_RD_LATENCY_ACC_NUM
Address: Operational Base + offset (0x08014)
gpu performance monitor status register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rd_latency_acc_cnt_r AXI read latency (>sw_rd_latency_thr) total number

GRF_GPU_PERF_RD_AXI_TOTAL_BYTE
Address: Operational Base + offset (0x08018)
gpu performance monitor status register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rd_axi_total_byte AXI active total read bytes/ddr align read bytes

GRF_GPU_PERF_WR_AXI_TOTAL_BYTE
Address: Operational Base + offset (0x0801c)
gpu performance monitor status register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	wr_axi_total_byte AXI active total write bytes/ddr align write bytes

GRF_GPU_PERF_WORKING_CNT
Address: Operational Base + offset (0x08020)
gpu performance monitor status register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	working_cnt_r working counter

GRF_CPU_CON0
Address: Operational Base + offset (0x0a000)
cpu control register 0

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:12	RW	0x0	cfgte_pd_core_l pd_core_l cpu cfgte bit control 0: disable 1: enable
11:8	RW	0x0	cfgend_pd_core_l pd_core_l cpu cfgend bit control 0: disable 1: enable
7	RW	0x0	l2rstdisable_pd_core_l pd_core_l cpu l2rstdisable bit control 0: disable 1: enable

Bit	Attr	Reset Value	Description
6	RW	0x0	dbgl1rstdisable_pd_core_l pd_core_l cpu dbgl1rstdisable bit control 0: disable 1: enable
5	RO	0x0	reserved
4	RW	0x0	clrexmonreq_pd_core_l pd_core_l cpu clrexmonreq bit control 0: disable 1: enable
3	RW	0x1	sysbardisable_pd_core_l pd_core_l cpu sysbardisable bit control 0: disable 1: enable
2	RW	0x0	broadcastcachemaint_pd_core_l pd_core_l cpu broadcastcachemaint bit control 0: disable 1: enable
1	RW	0x1	broadcastouter_pd_core_l pd_core_l cpu broadcastouter bit control 0: disable 1: enable
0	RW	0x1	broadcastinner_pd_core_l pd_core_l cpu broadcastinner bit control 1: enable 0: disable

GRF_CPU_CON1

Address: Operational Base + offset (0x0a004)

cpu control register 1

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:12	RW	0xf	gic_active_core_l pd_core_l gic_active bit control
11:8	RW	0x0	clusteridaff1_pd_core_l pd_core_l clusteridaff1 bit control
7:4	RW	0x0	arqos_pd_core_l pd_core_l arqos bit control
3:0	RW	0x0	awqos_pd_core_l pd_core_l awqos bit control

GRF_CPU_CON2

Address: Operational Base + offset (0x0a008)

cpu control register 2

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RO	0x0	reserved

Bit	Attr	Reset Value	Description
14	RW	0x0	gic_axim_err_ack gic axi master error acknowledges 0: disable 1: enable
13:12	RW	0x0	cfgte_pd_core_b pd_core_b cpu cfgte bit control 0: disable 1: enable
11:10	RO	0x0	reserved
9:8	RW	0x0	cfgend_pd_core_b pd_core_b cpu cfgend bit control 0: disable 1: enable
7	RW	0x0	l2rstdisable_pd_core_b pd_core_b cpu l2rstdisable bit control 0: disable 1: enable
6	RW	0x0	dbgl1rstdisable_pd_core_b pd_core_b cpu dbgl1rstdisable bit control 0: disable 1: enable
5	RO	0x0	reserved
4	RW	0x0	clrexmonreq_pd_core_b pd_core_b cpu clrexmonreq bit control 0: disable 1: enable
3	RW	0x1	sysbardisable_pd_core_b pd_core_b cpu sysbardisable bit control 0: disable 1: enable
2	RW	0x0	broadcastcachemaint_pd_core_b pd_core_b cpu broadcastcachemaint bit control 0: disable 1: enable
1	RW	0x1	broadcastouter_pd_core_b pd_core_b cpu broadcastouter bit control 0: disable 1: enable
0	RW	0x1	broadcastinner_pd_core_b pd_core_b cpu broadcastinner bit control 1: enable 0: disable

GRF_CPU_CON3

Address: Operational Base + offset (0x0a00c)
cpu control register 3

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RO	0x0	reserved
13:12	RW	0x3	gic_active_core_b pd_core_b gic_active bit control
11:10	RO	0x0	reserved
9:8	RW	0x1	clusteridaff1_pd_core_b pd_core_b clusteridaff1 bit control
7:6	RO	0x0	reserved
5:4	RW	0x1	arqos_pd_core_b pd_core_b arqos bit control
3:2	RO	0x0	reserved
1:0	RW	0x0	awqos_pd_core_b pd_core_b awqos bit control

GRF_CPU_STATUS0
Address: Operational Base + offset (0x0a080)
cpu status register 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	wrmemattr_pd_core_b wrmemattr of pd_core_b status
23:16	RW	0x00	rdmemattr_pd_core_b rdmemattr of pd_core_b status
15:8	RW	0x00	rdmemattr_pd_core_l rdmemattr of pd_core_l status
7:0	RW	0x00	wrmemattr_pd_core_l wrmemattr of pd_core_l status

GRF_CPU_STATUS1
Address: Operational Base + offset (0x0a084)

cpu status register 1

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x0	clremonack_pd_core_b the status of clremonack_pd_core_b
26	RW	0x0	clremonack_pd_core_l the status of clremonack_pd_core_l
25	RW	0x0	standbywfil2_pd_core_b standbywfil2 of pd_core_b status bit
24	RW	0x0	standbywfil2_pd_core_l standbywfil2 of pd_core_l status bit
23:22	RO	0x0	reserved
21:20	RW	0x0	smpen_pd_core_b status of smpen_pd_core_b
19:16	RW	0x0	smpen_pd_core_l status of smpen_pd_core_l
15:14	RO	0x0	reserved
13:12	RW	0x0	standbywfe_pd_core_b standbywfe of pd_core_b status bit
11:10	RO	0x0	reserved
9:8	RW	0x0	standbywfi_pd_core_b standbywfi of pd_core_b status bit
7:4	RW	0x0	standbywfe_pd_core_l standbywfe of pd_core_l status bit
3:0	RW	0x0	standbywfi_pd_core_l standbywfi of pd_core_l status bit

GRF_CPU_STATUS2

Address: Operational Base + offset (0x0a088)

cpu status register 2

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cci_event_bus the status of cci_event_bus[31:0]

GRF_CPU_STATUS3

Address: Operational Base + offset (0x0a08c)

cpu status register 3

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cci_event_bus the status of cci_event_bus[63:32]

GRF_CPU_STATUS4

Address: Operational Base + offset (0x0a090)

cpu status register 4

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

Bit	Attr	Reset Value	Description
29:0	RW	0x00000000	cci_event_bus the status of cci_event_bus[93:64]

GRF_CPU_STATUS5
Address: Operational Base + offset (0x0a094)
cpu status register 5

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9	RW	0x0	gic_axim_err gic_axim_err status bit
8	RW	0x0	gic_ecc_fatal gic_ecc_fatal status bit
7:0	RW	0x00	cci_nevntcntoverflow cci_nevntcntoverflow status bit

GRF_A53_PERF_CON0
Address: Operational Base + offset (0x0a100)
a53 performance monitor control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RO	0x0	reserved
13:8	RW	0x00	a53_sw_rd_latency_id Axi read channel id for latency AXI_PERFormance test
7	RO	0x0	reserved
6:5	RW	0x0	a53_sw_ddr_align_type 0: 16-Byte align 1: 32-Byte align 2: 64-Byte align 3: 128-Byte align

Bit	Attr	Reset Value	Description
4	RW	0x0	a53_sw_aw_cnt_id_type axi_perf counter id control 0: count all write channel id 1: count sw_ar_count_id write channel only
3	RW	0x0	a53_sw_ar_cnt_id_type axi_perf counter id control 0: count all read channel id 1: count sw_ar_count_id read channel only
2	RW	0x0	a53_sw_axi_cnt_type axi_perf counter type 0: axi transfer test 1: ddr align transfer test
1	RW	0x0	a53_sw_axi_perf_clr axi_perf clear bit 0: disable 1: enable
0	RW	0x0	a53_sw_axi_perf_work a53 performance monitor control register axi_perf enable bit 0: disable 1: enable

GRF_A53_PERF_CON1
Address: Operational Base + offset (0x0a104)
a53 performance monitor control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:12	RO	0x0	reserved
11:0	RW	0x000	a53_sw_rd_latency_thr Axi read channel id for latency AXI_PERFormance test

GRF_A53_PERF_CON2
Address: Operational Base + offset (0x0a108)
a53 performance monitor control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:13	RO	0x0	reserved
12:8	RW	0x00	a53_sw_aw_count_id When sw_aw_cnt_id_type=1, only count the id designated by sw_aw_count_id
7:6	RO	0x0	reserved
5:0	RW	0x00	a53_sw_ar_count_id When sw_ar_cnt_id_type=1, only count the id designated by sw_ar_count_id

GRF_A53_PERF_CON3
Address: Operational Base + offset (0x0a10c)
a53 performance monitor control register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:9	RW	0x00	mon_id mon_id bit control
8:2	RW	0x00	mon_id_bmsk mon_id_bmsk bit control
1	RW	0x0	mon_id_type mon_id_type bit control
0	RW	0x0	mon_id_msk mon_id_msk bit control

GRF_A53_PERF_RD_MON_ST
Address: Operational Base + offset (0x0a110)
performance monitor read start address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rd_start_addr monitor read start address

GRF_A53_PERF_RD_MON_END
Address: Operational Base + offset (0x0a114)
performance monitor end address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rd_end_addr monitor read end address

GRF_A53_PERF_WR_MON_ST
Address: Operational Base + offset (0x0a118)
performance write monitor start address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	wr_start_addr monitor write start address

GRF_A53_PERF_WR_MON_END
Address: Operational Base + offset (0x0a11c)
performance monitor write end address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	wr_end_addr monitor write end address

GRF_A53_PERF_RD_MAX_LATENCY_NUM
Address: Operational Base + offset (0x0a120)
a53 performance monitor status register

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	rd_max_latency_r axi read max latency output

GRF_A53_PERF_RD_LATENCY_SAMP_NUM
Address: Operational Base + offset (0x0a124)
a53 performance monitor status register

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:0	RW	0x0000000	rd_latency_samp_r AXI read latency total sample number

GRF_A53_PERF_RD_LATENCY_ACC_NUM
Address: Operational Base + offset (0x0a128)
a53 performance monitor status register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rd_latency_acc_cnt_r AXI read latency (>sw_rd_latency_thr) total number

GRF_A53_PERF_RD_AXI_TOTAL_BYTE
Address: Operational Base + offset (0x0a12c)
a53 performance monitor status register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rd_axi_total_byte AXI active total read bytes/ddr align read bytes

GRF_A53_PERF_WR_AXI_TOTAL_BYTE
Address: Operational Base + offset (0x0a130)
a53 performance monitor status register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	wr_axi_total_byte AXI active total write bytes/ddr align write bytes

GRF_A53_PERF_WORKING_CNT
Address: Operational Base + offset (0x0a134)
a53 performance monitor status register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	working_cnt_r working counter

GRF_A53_PERF_INT_STATUS
Address: Operational Base + offset (0x0a138)
a53 performance monitor status register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	int_status interrupt status bit

GRF_A72_PERF_CON0
Address: Operational Base + offset (0x0a200)
a72 performance monitor control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RO	0x0	reserved
14:8	RW	0x00	a72_sw_rd_latency_id Axi read channel id for latency AXI_PERFormance test
7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6:5	RW	0x0	a72_sw_ddr_align_type 0: 16-Byte align 1: 32-Byte align 2: 64-Byte align 3: 128-Byte align
4	RW	0x0	a72_sw_aw_cnt_id_type axi_perf counter id control 0: count all write channel id 1: count sw_ar_count_id write channel only
3	RW	0x0	a72_sw_ar_cnt_id_type axi_perf counter id control 0: count all read channel id 1: count sw_ar_count_id read channel only
2	RW	0x0	a72_sw_axi_cnt_type axi_perf counter type 0: axi transfer test 1: ddr align transfer test
1	RW	0x0	a72_sw_axi_perf_clr axi_perf clear bit 0: disable 1: enable
0	RW	0x0	a72_sw_axi_perf_work axi_perf enable bit 0: disable 1: enable

GRF_A72_PERF_CON1
Address: Operational Base + offset (0x0a204)
a72 performance monitor control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

Bit	Attr	Reset Value	Description
15:12	RO	0x0	reserved
11:0	RW	0x000	a72_sw_rd_latency_thr Axi read channel id for latency AXI_PERFormance test

GRF_A72_PERF_CON2
Address: Operational Base + offset (0x0a208)
a72 performance monitor control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RO	0x0	reserved
14:8	RW	0x00	a72_sw_aw_count_id When sw_aw_cnt_id_type=1, only count the id designated by sw_aw_count_id
7:6	RO	0x0	reserved
5:0	RW	0x00	a72_sw_ar_count_id When sw_ar_cnt_id_type=1, only count the id designated by sw_ar_count_id

GRF_A72_PERF_CON3
Address: Operational Base + offset (0x0a20c)
a72 performance monitor control register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:9	RW	0x00	mon_id mon_id bit control
8:2	RW	0x00	mon_id_bmsk mon_id_bmsk bit control
1	RW	0x0	mon_id_type mon_id_type bit control
0	RW	0x0	mon_id_msk mon_id_msk bit control

GRF_A72_PERF_RD_MON_ST
Address: Operational Base + offset (0x0a210)
performance monitor read start address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rd_start_addr monitor read start address

GRF_A72_PERF_RD_MON_END
Address: Operational Base + offset (0x0a214)
performance monitor end address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rd_end_addr monitor read end address

GRF_A72_PERF_WR_MON_ST
Address: Operational Base + offset (0x0a218)
performance write monitor start address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	wr_start_addr monitor write start address

GRF_A72_PERF_WR_MON_END
Address: Operational Base + offset (0x0a21c)
performance monitor write end address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	wr_end_addr monitor write end address

GRF_A72_PERF_RD_MAX_LATENCY_NUM
Address: Operational Base + offset (0x0a220)
a72 performance monitor status register

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	rd_max_latency_r axi read max latency output

GRF_A72_PERF_RD_LATENCY_SAMP_NUM
Address: Operational Base + offset (0x0a224)
a72 performance monitor status register

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:0	RW	0x0000000	rd_latency_samp_r AXI read latency total sample number

GRF_A72_PERF_RD_LATENCY_ACC_NUM
Address: Operational Base + offset (0x0a228)
a72 performance monitor status register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rd_latency_acc_cnt_r AXI read latency (>sw_rd_latency_thr) total number

GRF_A72_PERF_RD_AXI_TOTAL_BYTE
Address: Operational Base + offset (0x0a22c)
a72 performance monitor status register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rd_axi_total_byte AXI active total read bytes/ddr align read bytes

GRF_A72_PERF_WR_AXI_TOTAL_BYTE
Address: Operational Base + offset (0x0a230)
a72 performance monitor status register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	wr_axi_total_byte AXI active total write bytes/ddr align write bytes

GRF_A72_PERF_WORKING_CNT
Address: Operational Base + offset (0x0a234)
a72 performance monitor status register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	working_cnt_r working counter

GRF_A72_PERF_INT_STATUS
Address: Operational Base + offset (0x0a238)
a72 performance monitor status register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	int_status interrupt status bit

GRF_GMAC_PERF_CON0
Address: Operational Base + offset (0x0c000)
gmac performance monitor control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:13	RO	0x0	reserved
12:8	RW	0x00	gmac_sw_rd_latency_id Axi read channel id for latency AXI_PERFormance test
7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6:5	RW	0x0	gmac_sw_ddr_align_type 0: 16-Byte align 1: 32-Byte align 2: 64-Byte align 3: 128-Byte align
4	RW	0x0	gmac_sw_aw_cnt_id_type 0: count all write channels 1: count sw_aw_count_id write channel only
3	RW	0x0	gmac_sw_ar_cnt_id_type axi_perf counter id control 0: count all read channel id 1: count sw_ar_count_id read channel only
2	RW	0x0	gmac_sw_axi_cnt_type axi_perf counter type 0: axi transfer test 1: ddr align transfer test
1	RW	0x0	gmac_sw_axi_perf_clr axi_perf clear bit 0: disable 1: enable
0	RW	0x0	gmac_sw_axi_perf_work axi_perf enable bit 0: disable 1: enable

GRF_GMAC_PERF_CON1
Address: Operational Base + offset (0x0c004)
gmac performance monitor control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:12	RO	0x0	reserved

Bit	Attr	Reset Value	Description
11:0	RW	0x000	gmac_sw_rd_latency_thr Axi read channel id for latency AXI_PERFormance test

GRF_GMAC_PERF_CON2
Address: Operational Base + offset (0x0c008)
gmac performance monitor control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:12	RO	0x0	reserved
11:8	RW	0x0	gmac_sw_aw_count_id When sw_aw_cnt_id_type=1, only count the id designated by sw_aw_count_id
7:4	RO	0x0	reserved
3:0	RW	0x0	gmac_sw_ar_count_id When sw_ar_cnt_id_type=1, only count the id designated by sw_ar_count_id

GRF_GMAC_PERF_RD_MAX_LATENCY_NUM
Address: Operational Base + offset (0x0c00c)
gmac performance monitor status register

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:0	RW	0x0000	rd_max_latency_r axi read max latency oaxi read max latency outpututput

GRF_GMAC_PERF_RD_LATENCY_SAMP_NUM
Address: Operational Base + offset (0x0c010)
gmac performance monitor status register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:0	RW	0x0000000	rd_latency_samp_r AXI read latency total sample number

GRF_GMAC_PERF_RD_LATENCY_ACC_NUM
Address: Operational Base + offset (0x0c014)
gmac performance monitor status register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rd_latency_acc_cnt_r AXI read latency (>sw_rd_latency_thr) total number

GRF_GMAC_PERF_RD_AXI_TOTAL_BYTE
Address: Operational Base + offset (0x0c018)
gmac performance monitor status register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	rd_axi_total_byte AXI active total read bytes/ddr align read bytes

GRF_GMAC_PERF_WR_AXI_TOTAL_BYTE
Address: Operational Base + offset (0x0c01c)
gmac performance monitor status register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	wr_axi_total_byte AXI active total write bytes/ddr align write bytes

GRF_GMAC_PERF_WORKING_CNT
Address: Operational Base + offset (0x0c020)
gmac performance monitor status register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	working_cnt_r working counter

GRF_SOC_CON5
Address: Operational Base + offset (0x0c214)
SoC control register 5

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:12	RO	0x0	reserved
11:9	RW	0x0	gmac_phy_intf_sel PHY interface select 3'b001: RGMII 3'b100: RMII All others: Reserved
8	RW	0x0	gmac_flowctrl GMAC transmit flow control When set high, instructs the GMAC to transmit PAUSE Control frames in Full-duplex mode. In Half-duplex mode, the GMAC enables the Back-pressure function until this signal is made low again
7	RW	0x0	gmac_speed MAC speed 1'b1: 100-Mbps 1'b0: 10-Mbps
6	RW	0x0	rmii_mode RMII mode selection 1'b1: RMII mode 1'b0: MII mode
5:4	RW	0x0	gmac_clk_sel RGMII clock selection 2'b00: 125MHz 2'b11: 25MHz 2'b10: 2.5MHz
3	RW	0x1	rmii_clk_sel RMII clock selection 1'b1: 25MHz 1'b0: 2.5MHz

Bit	Attr	Reset Value	Description
2:0	RO	0x0	reserved

GRF_SOC_CON6
Address: Operational Base + offset (0x0c218)
SoC control register 6

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	gmac_rxclk_dly_ena RGMII TX clock delayline enable 1'b1: enable 1'b0: disable
14:8	RW	0x00	gmac_clk_rx_dl_cfg RGMII RX clock delayline value
7	RW	0x0	gmac_txclk_dly_ena RGMII TX clock delayline enable 1'b1: enable 1'b0: disable
6:0	RW	0x00	gmac_clk_tx_dl_cfg RGMII TX clock delayline value

GRF_GPIO2A_IOMUX
Address: Operational Base + offset (0x0e000)
GPIO2A iomux control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x0	gpio2a7_sel GPIO2A[7] iomux select 2'b00: gpio 2'b01: vop_data7 2'b10: i2c7nfc_sda 2'b11: cif_data7
13:12	RW	0x0	gpio2a6_sel GPIO2A[6] iomux select 2'b00: gpio 2'b01: vop_data6 2'b10: uphyjtag_tms 2'b11:cif_data6
11:10	RW	0x0	gpio2a5_sel GPIO2A[5] iomux select 2'b00: gpio 2'b01: vop_data5 2'b10: uphyjtag_tck 2'b11: cif_data5
9:8	RW	0x0	gpio2a4_sel GPIO2A[4] iomux select 2'b00: gpio 2'b01: vop_data4 2'b10: uphyjtag_tdo 2'b11: cif_data4
7:6	RW	0x0	gpio2a3_sel GPIO2A[3] iomux select 2'b00: gpio 2'b01: vop_data3 2'b10: uphyjtag_tdi 2'b11: cif_data3

Bit	Attr	Reset Value	Description
5:4	RW	0x0	gpio2a2_sel GPIO2A[2] iomux select 2'b00: gpio 2'b01: vop_data2 2'b10: uphyjtag_trstn 2'b11: cif_data2
3:2	RW	0x0	gpio2a1_sel GPIO2A[1] iomux select 2'b00: gpio 2'b01: vop_data1 2'b10: i2c2tp_scl 2'b11: cif_data1
1:0	RW	0x0	gpio2a0_sel GPIO2A[0] iomux select 2'b00: gpio 2'b01: vop_data0 2'b10: i2c2tp_sda 2'b11: cif_data0

GRF_GPIO2B_IOMUX
Address: Operational Base + offset (0x0e004)
GPIO2B iomux control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:10	RO	0x0	reserved
9:8	RW	0x0	gpio2b4_sel GPIO2B[4] iomux select 2'b00: gpio 2'b01: spi2tpm_csn0 2'b10: reserved 2'b11: reserved

Bit	Attr	Reset Value	Description
7:6	RW	0x0	gpio2b3_sel GPIO2B[3] iomux select 2'b00: gpio 2'b01: spi2tpm_clk 2'b10: vop_den 2'b11: cif_clkouta
5:4	RW	0x0	gpio2b2_sel GPIO2B[2] iomux select 2'b00: gpio 2'b01: spi2tpm_txd 2'b10: i2c6tpm_scl 2'b11: cif_clkin
3:2	RW	0x0	gpio2b1_sel GPIO2B[1] iomux select 2'b00: gpio 2'b01: spi2tpm_rxd 2'b10: i2c6tpm_sda 2'b11: cif_href
1:0	RW	0x0	gpio2b0_sel GPIO2B[0] iomux select 2'b00: gpio 2'b01: vop_dclk 2'b10: i2c7nfc_scl 2'b11: cif_vsync

GRF_GPIO2C_IOMUX
Address: Operational Base + offset (0x0e008)
GPIO2C iomux control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

Bit	Attr	Reset Value	Description
15:14	RW	0x0	gpio2c7_sel GPIO2C[7] iomux select 2'b00: gpio 2'b01: sdio_data3 2'b10: spi5expplus_csn0 2'b11: reserved
13:12	RW	0x0	gpio2c6_sel GPIO2C[6] iomux select 2'b00: gpio 2'b01: sdio_data2 2'b10: spi5expplus_clk 2'b11: reserved
11:10	RW	0x0	gpio2c5_sel GPIO2C[5] iomux select 2'b00: gpio 2'b01: sdio_data1 2'b10: spi5expplus_txd 2'b11: reserved
9:8	RW	0x0	gpio2c4_sel GPIO2C[4] iomux select 2'b00: gpio 2'b01: sdio_data0 2'b10: spi5expplus_rxd 2'b11: reserved
7:6	RW	0x0	gpio2c3_sel GPIO2C[3] iomux select 2'b00: gpio 2'b01: uart0bt_rtsn 2'b10: reserved 2'b11: reserved
5:4	RW	0x0	gpio2c2_sel GPIO2C[2] iomux select 2'b00: gpio 2'b01: uart0bt_ctsn 2'b10: reserved 2'b11: reserved
3:2	RW	0x0	gpio2c1_sel GPIO2C[1] iomux select 2'b00: gpio 2'b01: uart0bt_sout 2'b10: reserved 2'b11: reserved

Bit	Attr	Reset Value	Description
1:0	RW	0x0	gpio2c0_sel GPIO2C[0] iomux select 2'b00: gpio 2'b01: uart0bt_sin 2'b10: reserved 2'b11: reserved

GRF_GPIO2D_IOMUX
Address: Operational Base + offset (0x0e00c)
GPIO2D iomux control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:10	RO	0x0	reserved
9:8	RW	0x0	gpio2d4_sel GPIO2D[4] iomux select 2'b00: gpio 2'b01: sdio_bkpwr 2'b10: reserved 2'b11: reserved
7:6	RW	0x0	gpio2d3_sel GPIO2D[3] iomux select 2'b00: gpio 2'b01: sdio_pwren 2'b10: reserved 2'b11: reserved
5:4	RW	0x0	gpio2d2_sel GPIO2D[2] iomux select 2'b00: gpio 2'b01: sdio_detectn 2'b10: pcie_clkreqn 2'b11: reserved

Bit	Attr	Reset Value	Description
3:2	RW	0x0	gpio2d1_sel GPIO2D[1] iomux select 2'b00: gpio 2'b01: sdio_clkout 2'b10: test_clkout1 2'b11: reserved
1:0	RW	0x0	gpio2d0_sel GPIO2D[0] iomux select 2'b00: gpio 2'b01: sdio_cmd 2'b10: reserved 2'b11: reserved

GRF_GPIO3A_IOMUX
Address: Operational Base + offset (0x0e010)
GPIO3A iomux control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x0	gpio3a7_sel GPIO3A[7] iomux select 2'b00: gpio 2'b01: mac_rxd1 2'b10: spi0norcodec_csn0 2'b11: reserved
13:12	RW	0x0	gpio3a6_sel GPIO3A[6] iomux select 2'b00: gpio 2'b01: mac_rxd0 2'b10: spi0norcodec_clk 2'b11: reserved

Bit	Attr	Reset Value	Description
11:10	RW	0x0	gpio3a5_sel GPIO3A[5] iomux select 2'b00: gpio 2'b01: mac_txd1 2'b10: spi0norcodec_txd 2'b11: reserved
9:8	RW	0x0	gpio3a4_sel GPIO3A[4] iomux select 2'b00: gpio 2'b01: mac_txd0 2'b10: spi0norcodec_rxd 2'b11: reserved
7:6	RW	0x0	gpio3a3_sel GPIO3A[3] iomux select 2'b00: gpio 2'b01: mac_rxd3 2'b10: spi4exp_csn0 2'b11: trace_data15
5:4	RW	0x0	gpio3a2_sel GPIO3A[2] iomux select 2'b00: gpio 2'b01: mac_rxd2 2'b10: spi4exp_clk 2'b11: trace_data14
3:2	RW	0x0	gpio3a1_sel GPIO3A[1] iomux select 2'b00: gpio 2'b01: mac_txd3 2'b10: spi4exp_txd 2'b11: trace_data13
1:0	RW	0x0	gpio3a0_sel GPIO3A[0] iomux select 2'b00: gpio 2'b01: mac_txd2 2'b10: spi4exp_rxd 2'b11: trace_data12

GRF_GPIO3B_IOMUX
Address: Operational Base + offset (0x0e014)
GPIO3B iomux control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x0	gpio3b7_sel GPIO3B[7] iomux select 2'b00: gpio 2'b01: mac_crs 2'b10: uart3gps_sout 2'b11: cif_clkoutb
13:12	RW	0x0	gpio3b6_sel GPIO3B[6] iomux select 2'b00: gpio 2'b01: mac_rxclk 2'b10: uart3gps_sin 2'b11: reserved
11:10	RW	0x0	gpio3b5_sel GPIO3B[5] iomux select 2'b00: gpio 2'b01: mac_mdio 2'b10: uart1bb_sout 2'b11: reserved
9:8	RW	0x0	gpio3b4_sel GPIO3B[4] iomux select 2'b00: gpio 2'b01: mac_txen 2'b10: uart1bb_sin 2'b11: reserved
7:6	RW	0x0	gpio3b3_sel GPIO3B[3] iomux select 2'b00: gpio 2'b01: mac_clk 2'b10: i2c5trackpad_scl 2'b11: reserved

Bit	Attr	Reset Value	Description
5:4	RW	0x0	gpio3b2_sel GPIO3B[2] iomux select 2'b00: gpio 2'b01: mac_rxer 2'b10: i2c5trackpad_sda 2'b11: reserved
3:2	RW	0x0	gpio3b1_sel GPIO3B[1] iomux select 2'b00: gpio 2'b01: mac_rxdv 2'b10: reserved 2'b11: reserved
1:0	RW	0x0	gpio3b0_sel GPIO3B[0] iomux select 2'b00: gpio 2'b01: mac_mdc 2'b10: spi0norcodec_csn1 2'b11: reserved

GRF_GPIO3C_IOMUX
Address: Operational Base + offset (0x0e018)
GPIO3C iomux control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:4	RO	0x0	reserved
3:2	RW	0x0	gpio3c1_sel GPIO3C[1] iomux select 2'b00: gpio 2'b01: mac_txclk 2'b10: uart3gps_rtsn 2'b11: reserved

Bit	Attr	Reset Value	Description
1:0	RW	0x0	gpio3c0_sel GPIO3C[0] iomux select 2'b00: gpio 2'b01: mac_col 2'b10: uart3gps_ctsn 2'b11: spdif_txb

GRF_GPIO3D_IOMUX
Address: Operational Base + offset (0x0e01c)
GPIO3D iomux control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x0	gpio3d7_sel GPIO3D[7] iomux select 2'b00: gpio 2'b01: i2s0_sdo0 2'b10: trace_data7 2'b11: a53l2_wfi
13:12	RW	0x0	gpio3d6_sel GPIO3D[6] iomux select 2'b00: gpio 2'b01: i2s0_sdi3sdo1 2'b10: trace_data6 2'b11: a72l2_wfi
11:10	RW	0x0	gpio3d5_sel GPIO3D[5] iomux select 2'b00: gpio 2'b01: i2s0_sdi2sdo2 2'b10: trace_data5 2'b11: a53core3_wfi

Bit	Attr	Reset Value	Description
9:8	RW	0x0	gpio3d4_sel GPIO3D[4] iomux select 2'b00: gpio 2'b01: i2s0_sdi1sdo3 2'b10: trace_data4 2'b11: a53core2_wfi
7:6	RW	0x0	gpio3d3_sel GPIO3D[3] iomux select 2'b00: gpio 2'b01: i2s0_sdi0 2'b10: trace_data3 2'b11: a53core1_wfi
5:4	RW	0x0	gpio3d2_sel GPIO3D[2] iomux select 2'b00: gpio 2'b01: i2s0_lrcktx 2'b10: trace_data2 2'b11: a53core0_wfi
3:2	RW	0x0	gpio3d1_sel GPIO3D[1] iomux select 2'b00: gpio 2'b01: i2s0_lrckrx 2'b10: trace_data1 2'b11: a72core1_wfi
1:0	RW	0x0	gpio3d0_sel GPIO3D[0] iomux select 2'b00: gpio 2'b01: i2s0_sclk 2'b10: trace_data0 2'b11: a72core0_wfi

GRF_GPIO4A_IOMUX
Address: Operational Base + offset (0x0e020)
GPIO4A iomux control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x0	gpio4a7_sel GPIO4A[7] iomux select 2'b00: gpio 2'b01: i2s1_sdo0 2'b10: reserved 2'b11: reserved
13:12	RW	0x0	gpio4a6_sel GPIO4A[6] iomux select 2'b00: gpio 2'b01: i2s1_sdi0 2'b10: reserved 2'b11: reserved
11:10	RW	0x0	gpio4a5_sel GPIO4A[5] iomux select 2'b00: gpio 2'b01: i2s1_lrcktx 2'b10: trace_data11 2'b11: reserved
9:8	RW	0x0	gpio4a4_sel GPIO4A[4] iomux select 2'b00: gpio 2'b01: i2s1_lrckrx 2'b10: trace_data10 2'b11: reserved
7:6	RW	0x0	gpio4a3_sel GPIO4A[3] iomux select 2'b00: gpio 2'b01: i2s1_sclk 2'b10: trace_data9 2'b11: reserved

Bit	Attr	Reset Value	Description
5:4	RW	0x0	gpio4a2_sel GPIO4A[2] iomux select 2'b00: gpio 2'b01: i2c1audiocam_scl 2'b10: trace_data8 2'b11: reserved
3:2	RW	0x0	gpio4a1_sel GPIO4A[1] iomux select 2'b00: gpio 2'b01: i2c1audiocam_sda 2'b10: trace_clk 2'b11: reserved
1:0	RW	0x0	gpio4a0_sel GPIO4A[0] iomux select 2'b00: gpio 2'b01: i2s_clk 2'b10: trace_ctl 2'b11: lpm0_wfi

GRF_GPIO4B_IOMUX
Address: Operational Base + offset (0x0e024)
GPIO4B iomux control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:12	RO	0x0	reserved
11:10	RW	0x0	gpio4b5_sel GPIO4B[5] iomux select 2'b00: gpio 2'b01: sdmmc_cmd 2'b10: mcujtag_tms 2'b11: hdcpjtag_tms

Bit	Attr	Reset Value	Description
9:8	RW	0x0	gpio4b4_sel GPIO4B[4] iomux select 2'b00: gpio 2'b01: sdmmc_clkout 2'b10: mcujtag_tck 2'b11: hdcpjtag_tck
7:6	RW	0x0	gpio4b3_sel GPIO4B[3] iomux select 2'b00: gpio 2'b01: sdmmc_data3 2'b10: cxcsjtag_tms 2'b11: hdcpjtag_tdo
5:4	RW	0x0	gpio4b2_sel GPIO4B[2] iomux select 2'b00: gpio 2'b01: sdmmc_data2 2'b10: cxcsjtag_tck 2'b11: hdcpjtag_tdi
3:2	RW	0x0	gpio4b1_sel GPIO4B[1] iomux select 2'b00: gpio 2'b01: sdmmc_data1 2'b10: uart2dbga_sout 2'b11: hdcpjtag_trstn
1:0	RW	0x0	gpio4b0_sel GPIO4B[0] iomux select 2'b00: gpio 2'b01: sdmmc_data0 2'b10: uart2dbga_sin 2'b11: reserved

GRF_GPIO4C_IOMUX
Address: Operational Base + offset (0x0e028)
GPIO4C iomux control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x0	gpio4c7_sel GPIO4C[7] iomux select 2'b00: gpio 2'b01: hdmi_cecinout 2'b10: edp_hotplug 2'b11: reserved
13:12	RW	0x0	gpio4c6_sel GPIO4C[6] iomux select 2'b00: gpio 2'b01: pwm_1 2'b10: reserved 2'b11: reserved
11:10	RW	0x0	gpio4c5_sel GPIO4C[5] iomux select 2'b00: gpio 2'b01: spdif_tx 2'b10: reserved 2'b11: reserved
9:8	RW	0x0	gpio4c4_sel GPIO4C[4] iomux select 2'b00: gpio 2'b01: uart2dbgc_sout 2'b10: uarthdcp_sout 2'b11: reserved
7:6	RW	0x0	gpio4c3_sel GPIO4C[3] iomux select 2'b00: gpio 2'b01: uart2dbgc_sin 2'b10: uarthdcp_sin 2'b11: reserved

Bit	Attr	Reset Value	Description
5:4	RW	0x0	gpio4c2_sel GPIO4C[2] iomux select 2'b00: gpio 2'b01: pwm_0 2'b10: vop0_pwm 2'b11: vop1_pwm
3:2	RW	0x0	gpio4c1_sel GPIO4C[1] iomux select 2'b00: gpio 2'b01: i2c3hdmi_scl 2'b10: uart2dbgb_sout 2'b11: hdmii2c_scl
1:0	RW	0x0	gpio4c0_sel GPIO4C[0] iomux select 2'b00: gpio 2'b01: i2c3hdmi_sda 2'b10: uart2dbgb_sin 2'b11: hdmii2c_sda

GRF_GPIO4D_IOMUX
Address: Operational Base + offset (0x0e02c)
GPIO4D iomux control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:4	RO	0x0	reserved
3:2	RW	0x0	gpio4d1_sel GPIO4D[1] iomux select 2'b00: gpio 2'b01: dp_hotplug 2'b10: reserved 2'b11: reserved

Bit	Attr	Reset Value	Description
1:0	RW	0x0	gpio4d0_sel GPIO4D[0] iomux select 2'b00: gpio 2'b01: pcie_clkreqnb 2'b10: reserved 2'b11: reserved

GRF_GPIO2A_P
Address: Operational Base + offset (0x0e040)
GPIO2A PU/PD control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x1	gpio2a7_p GPIO2A PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)
13:12	RW	0x2	gpio2a6_p GPIO2A PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

Bit	Attr	Reset Value	Description
11:10	RW	0x2	gpio2a5_p GPIO2A PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)
9:8	RW	0x2	gpio2a4_p GPIO2A PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)
7:6	RW	0x2	gpio2a3_p GPIO2A PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)
5:4	RW	0x2	gpio2a2_p GPIO2A PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)
3:2	RW	0x1	gpio2a1_p GPIO2A PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)
1:0	RW	0x1	gpio2a0_p GPIO2A PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO2B_P
Address: Operational Base + offset (0x0e044)

GPIO2B PU/PD control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:10	RO	0x0	reserved
9:8	RW	0x1	gpio2b4_p GPIO2B PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)
7:6	RW	0x1	gpio2b3_p GPIO2B PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)
5:4	RW	0x1	gpio2b2_p GPIO2B PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)
3:2	RW	0x1	gpio2b1_p GPIO2B PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

Bit	Attr	Reset Value	Description
1:0	RW	0x1	gpio2b0_p GPIO2B PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO2C_P
Address: Operational Base + offset (0x0e048)
GPIO2C PU/PD control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x3	gpio2c7_p GPIO2C PE/PS programmation section, every GPIO bit corresponding to 2bits 2'b00: pervious-state 2'b01: weak 0(pull-down); 2'b10: pervious-state 2'b11: weak 1(pull-up);
13:12	RW	0x3	gpio2c6_p GPIO2C PE/PS programmation section, every GPIO bit corresponding to 2bits 2'b00: pervious-state 2'b01: weak 0(pull-down); 2'b10: pervious-state 2'b11: weak 1(pull-up);

Bit	Attr	Reset Value	Description
11:10	RW	0x3	gpio2c5_p GPIO2C PE/PS programmation section, every GPIO bit corresponding to 2bits 2'b00: pervious-state 2'b01: weak 0(pull-down); 2'b10: pervious-state 2'b11: weak 1(pull-up);
9:8	RW	0x3	gpio2c4_p GPIO2C PE/PS programmation section, every GPIO bit corresponding to 2bits 2'b00: pervious-state 2'b01: weak 0(pull-down); 2'b10: pervious-state 2'b11: weak 1(pull-up);
7:6	RW	0x3	gpio2c3_p GPIO2C PE/PS programmation section, every GPIO bit corresponding to 2bits 2'b00: pervious-state 2'b01: weak 0(pull-down); 2'b10: pervious-state 2'b11: weak 1(pull-up);
5:4	RW	0x3	gpio2c2_p GPIO2C PE/PS programmation section, every GPIO bit corresponding to 2bits 2'b00: pervious-state 2'b01: weak 0(pull-down); 2'b10: pervious-state 2'b11: weak 1(pull-up);
3:2	RW	0x3	gpio2c1_p GPIO2C PE/PS programmation section, every GPIO bit corresponding to 2bits 2'b00: pervious-state 2'b01: weak 0(pull-down); 2'b10: pervious-state 2'b11: weak 1(pull-up);
1:0	RW	0x3	gpio2c0_p GPIO2C PE/PS programmation section, every GPIO bit corresponding to 2bits 2'b00: pervious-state 2'b01: weak 0(pull-down); 2'b10: pervious-state 2'b11: weak 1(pull-up);

GRF_GPIO2D_P

Address: Operational Base + offset (0x0e04c)
GPIO2D PU/PD control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:10	RO	0x0	reserved
9:8	RW	0x0	gpio2d4_p GPIO2D PE/PS programmation section, every GPIO bit corresponding to 2bits 2'b00: pervious-state 2'b01: weak 0(pull-down); 2'b10: pervious-state 2'b11: weak 1(pull-up);
7:6	RW	0x1	gpio2d3_p GPIO2D PE/PS programmation section, every GPIO bit corresponding to 2bits 2'b00: pervious-state 2'b01: weak 0(pull-down); 2'b10: pervious-state 2'b11: weak 1(pull-up);
5:4	RW	0x3	gpio2d2_p GPIO2D PE/PS programmation section, every GPIO bit corresponding to 2bits 2'b00: pervious-state 2'b01: weak 0(pull-down); 2'b10: pervious-state 2'b11: weak 1(pull-up);
3:2	RW	0x3	gpio2d1_p GPIO2D PE/PS programmation section, every GPIO bit corresponding to 2bits 2'b00: pervious-state 2'b01: weak 0(pull-down); 2'b10: pervious-state 2'b11: weak 1(pull-up);

Bit	Attr	Reset Value	Description
1:0	RW	0x3	gpio2d0_p GPIO2D PE/PS programmation section, every GPIO bit corresponding to 2bits 2'b00: pervious-state 2'b01: weak 0(pull-down); 2'b10: pervious-state 2'b11: weak 1(pull-up);

GRF_GPIO3A_P
Address: Operational Base + offset (0x0e050)
GPIO3A PU/PD control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x1	gpio3a7_p GPIO3A PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)
13:12	RW	0x1	gpio3a6_p GPIO3A PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

Bit	Attr	Reset Value	Description
11:10	RW	0x2	gpio3a5_p GPIO3A PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)
9:8	RW	0x2	gpio3a4_p GPIO3A PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)
7:6	RW	0x1	gpio3a3_p GPIO3A PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)
5:4	RW	0x1	gpio3a2_p GPIO3A PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)
3:2	RW	0x2	gpio3a1_p GPIO3A PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)
1:0	RW	0x2	gpio3a0_p GPIO3A PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO3B_P
Address: Operational Base + offset (0x0e054)

GPIO3B PU/PD control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x1	gpio3b7_p GPIO3B PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)
13:12	RW	0x1	gpio3b6_p GPIO3B PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)
11:10	RW	0x1	gpio3b5_p GPIO3B PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)
9:8	RW	0x1	gpio3b4_p GPIO3B PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

Bit	Attr	Reset Value	Description
7:6	RW	0x1	gpio3b3_p GPIO3B PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)
5:4	RW	0x1	gpio3b2_p GPIO3B PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)
3:2	RW	0x2	gpio3b1_p GPIO3B PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)
1:0	RW	0x1	gpio3b0_p GPIO3B PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO3C_P
Address: Operational Base + offset (0x0e058)
GPIO3C PU/PD control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:4	RO	0x0	reserved
3:2	RW	0x1	gpio3c1_p GPIO3A PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)
1:0	RW	0x1	gpio3c0_p GPIO3C PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO3D_P
Address: Operational Base + offset (0x0e05c)
GPIO3D PU/PD control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x2	gpio3d7_p GPIO3D PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)
13:12	RW	0x2	gpio3d6_p GPIO3D PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)
11:10	RW	0x2	gpio3d5_p GPIO3D PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)
9:8	RW	0x2	gpio3d4_p GPIO3D PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

Bit	Attr	Reset Value	Description
7:6	RW	0x2	gpio3d3_p GPIO3D PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)
5:4	RW	0x2	gpio3d2_p GPIO3D PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)
3:2	RW	0x2	gpio3d1_p GPIO3D PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)
1:0	RW	0x2	gpio3d0_p GPIO3D PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO4A_P
Address: Operational Base + offset (0x0e060)
GPIO4A PU/PD control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x2	gpio4a7_p GPIO4A PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)
13:12	RW	0x2	gpio4a6_p GPIO4A PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)
11:10	RW	0x2	gpio4a5_p GPIO4A PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)
9:8	RW	0x2	gpio4a4_p GPIO4A PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

Bit	Attr	Reset Value	Description
7:6	RW	0x2	gpio4a3_p GPIO4A PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)
5:4	RW	0x1	gpio4a2_p GPIO4A PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)
3:2	RW	0x1	gpio4a1_p GPIO4A PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)
1:0	RW	0x2	gpio4a0_p GPIO4A PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO4B_P
Address: Operational Base + offset (0x0e064)
GPIO4B PU/PD control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:12	RO	0x0	reserved
11:10	RW	0x1	gpio4b5_p GPIO4B PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)
9:8	RW	0x2	gpio4b4_p GPIO4B PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)
7:6	RW	0x1	gpio4b3_p GPIO4B PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)
5:4	RW	0x1	gpio4b2_p GPIO4B PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

Bit	Attr	Reset Value	Description
3:2	RW	0x1	gpio4b1_p GPIO4B PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)
1:0	RW	0x1	gpio4b0_p GPIO4B PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO4C_P
Address: Operational Base + offset (0x0e068)
GPIO4C PU/PD control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x1	gpio4c7_p GPIO4C PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

Bit	Attr	Reset Value	Description
13:12	RW	0x2	gpio4c6_p GPIO4C PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)
11:10	RW	0x2	gpio4c5_p GPIO4C PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)
9:8	RW	0x1	gpio4c4_p GPIO4C PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)
7:6	RW	0x1	gpio4c3_p GPIO4C PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)
5:4	RW	0x2	gpio4c2_p GPIO4C PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)
3:2	RW	0x1	gpio4c1_p GPIO4C PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

Bit	Attr	Reset Value	Description
1:0	RW	0x1	gpio4c0_p GPIO4C PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO4D_P
Address: Operational Base + offset (0x0e06c)
GPIO4D PU/PD control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RO	0x0	reserved
13:12	RW	0x2	gpio4d6_p GPIO4D PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)
11:10	RW	0x2	gpio4d5_p GPIO4D PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

Bit	Attr	Reset Value	Description
9:8	RW	0x2	gpio4d4_p GPIO4D PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)
7:6	RW	0x2	gpio4d3_p GPIO4D PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)
5:4	RW	0x2	gpio4d2_p GPIO4D PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)
3:2	RW	0x2	gpio4d1_p GPIO4D PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)
1:0	RW	0x1	gpio4d0_p GPIO4D PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

GRF_GPIO2A_SR

Address: Operational Base + offset (0x0e080)

GPIO2A slew rate control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RO	0x0	reserved
7:0	RW	0x00	gpio2a_sr GPIO slew rate programmation section, every GPIO bit corresponding to 1bits 1'b0: slow 1'b1: fast

GRF_GPIO2B_SR
Address: Operational Base + offset (0x0e084)
GPIO2B slew rate control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:5	RO	0x0	reserved

Bit	Attr	Reset Value	Description
4:0	RW	0x00	gpio2b_sr GPIO slew rate programmation section, every GPIO bit corresponding to 1bits 1'b0: slow 1'b1: fast

GRF_GPIO2C_SR
Address: Operational Base + offset (0x0e088)
GPIO2C slew rate control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RO	0x0	reserved
7:0	RW	0x00	gpio2c_sr GPIO slew rate programmation section, every GPIO bit corresponding to 1bits 1'b0: slow 1'b1: fast

GRF_GPIO2D_SR
Address: Operational Base + offset (0x0e08c)
GPIO2D slew rate control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:5	RO	0x0	reserved
4:0	RW	0x00	gpio2d_sr GPIO slew rate programmation section, every GPIO bit corresponding to 1bits 1'b0: slow 1'b1: fast

GRF_GPIO3D_SR
Address: Operational Base + offset (0x0e09c)
GPIO3D slew rate control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RO	0x0	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0x00	gpio3d_sr GPIO slew rate programmation section, every GPIO bit corresponding to 1bits 1'b0: slow 1'b1: fast

GRF_GPIO4A_SR
Address: Operational Base + offset (0x0e0a0)
GPIO4A slew rate control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RO	0x0	reserved
7:0	RW	0x00	gpio4a_sr GPIO slew rate programmation section, every GPIO bit corresponding to 1bits 1'b0: slow 1'b1: fast

GRF_GPIO4B_SR
Address: Operational Base + offset (0x0e0a4)
GPIO4B slew rate control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:6	RO	0x0	reserved
5:0	RW	0x3f	gpio4b_sr GPIO slew rate programmation section, every GPIO bit corresponding to 1bits 1'b0: slow 1'b1: fast

GRF_GPIO4C_SR
Address: Operational Base + offset (0x0e0a8)
GPIO4C slew rate control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RO	0x0	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0x00	gpio4c_sr GPIO slew rate programmation section, every GPIO bit corresponding to 1bits 1'b0: slow 1'b1: fast

GRF_GPIO4D_SR
Address: Operational Base + offset (0x0e0ac)
GPIO4D slew rate control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:7	RO	0x0	reserved
6:0	RW	0x00	gpio4d_sr GPIO slew rate programmation section, every GPIO bit corresponding to 1bits 1'b0: slow 1'b1: fast

GRF_GPIO2A_SMT
Address: Operational Base + offset (0x0e0c0)
GPIO2A smitter control register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RO	0x0	reserved
7:0	RW	0x00	gpio2a_smt GPIO schmitt trigger control, every GPIO bit corresponding to 1bits . 0: No hysteresis 1: Schmitt trigger enabled.

GRF_GPIO2B_SMT
Address: Operational Base + offset (0x0e0c4)
GPIO2B smitter control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RO	0x0	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0x00	gpio2b_smt GPIO schmitt trigger control, every GPIO bit corresponding to 1bits . 0: No hysteresis 1: Schmitt trigger enabled.

GRF_GPIO2C_SMT
Address: Operational Base + offset (0x0e0c8)
GPIO2C smitter control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0000	gpio2c_smt GPIO schmitt trigger control, every GPIO bit corresponding to 2 bits . 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3

GRF_GPIO2D_SMT
Address: Operational Base + offset (0x0e0cc)
GPIO2D smitter control register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0000	gpio2d_smt GPIO schmitt trigger control, every GPIO bit corresponding to 2 bits . 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3

GRF_GPIO3A_SMT
Address: Operational Base + offset (0x0e0d0)
GPIO3A smitter control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RO	0x0	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0xf0	gpio3a_smt GPIO schmitt trigger control, every GPIO bit corresponding to 1bits . 0: No hysteresis 1: Schmitt trigger enabled.

GRF_GPIO3B_SMT
Address: Operational Base + offset (0x0e0d4)
GPIO3B smitter control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RO	0x0	reserved
7:0	RW	0x00	gpio3b_smt GPIO schmitt trigger control, every GPIO bit corresponding to 1bits . 0: No hysteresis 1: Schmitt trigger enabled.

GRF_GPIO3C_SMT
Address: Operational Base + offset (0x0e0d8)
GPIO3C smitter control register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:2	RO	0x0	reserved
1:0	RW	0x0	gpio3c_smt GPIO schmitt trigger control, every GPIO bit corresponding to 1bits . 0: No hysteresis 1: Schmitt trigger enabled.

GRF_GPIO3D_SMT
Address: Operational Base + offset (0x0e0dc)
GPIO3D smitter control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RO	0x0	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0x00	gpio3d_smt GPIO schmitt trigger control, every GPIO bit corresponding to 1bits . 0: No hysteresis 1: Schmitt trigger enabled.

GRF_GPIO4A_SMT
Address: Operational Base + offset (0x0e0e0)
GPIO4A smitter control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RO	0x0	reserved
7:0	RW	0x00	gpio4a_smt GPIO schmitt trigger control, every GPIO bit corresponding to 1bits . 0: No hysteresis 1: Schmitt trigger enabled.

GRF_GPIO4B_SMT
Address: Operational Base + offset (0x0e0e4)
GPIO4B smitter control register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:6	RO	0x0	reserved
5:0	RW	0x3f	gpio4b_smt GPIO schmitt trigger control, every GPIO bit corresponding to 1bits . 0: No hysteresis 1: Schmitt trigger enabled.

GRF_GPIO4C_SMT
Address: Operational Base + offset (0x0e0e8)
GPIO4C smitter control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RO	0x0	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0x00	gpio4c_smt GPIO schmitt trigger control, every GPIO bit corresponding to 1bits . 0: No hysteresis 1: Schmitt trigger enabled.

GRF_GPIO4D_SMT
Address: Operational Base + offset (0x0e0ec)
GPIO4D smitter control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:7	RO	0x0	reserved
6:0	RW	0x00	gpio4d_smt GPIO schmitt trigger control, every GPIO bit corresponding to 1bits . 0: No hysteresis 1: Schmitt trigger enabled.

GRF_GPIO2A_E
Address: Operational Base + offset (0x0e100)
GPIO2A drive strength control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x0	gpio2a7_e GPIO2A7 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3
13:12	RW	0x0	gpio2a6_e GPIO2A6 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3
11:10	RW	0x0	gpio2a5_e GPIO2A5 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3
9:8	RW	0x0	gpio2a4_e GPIO2A4 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3

Bit	Attr	Reset Value	Description
7:6	RW	0x0	gpio2a3_e GPIO2A3 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3
5:4	RW	0x0	gpio2a2_e GPIO2A2 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3
3:2	RW	0x0	gpio2a1_e GPIO2A1 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3
1:0	RW	0x0	gpio2a0_e GPIO2A0 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3

GRF_GPIO2B_E
Address: Operational Base + offset (0x0e104)
GPIO2B drive strength control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x0	gpio2b7_e GPIO2B7 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3
13:12	RW	0x0	gpio2b6_e GPIO2B6 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3
11:10	RW	0x0	gpio2b5_e GPIO2B5 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3
9:8	RW	0x0	gpio2b4_e GPIO2B4 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3

Bit	Attr	Reset Value	Description
7:6	RW	0x0	gpio2b3_e GPIO2B3 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3
5:4	RW	0x0	gpio2b2_e GPIO2B2 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3
3:2	RW	0x0	gpio2b1_e GPIO2B1 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3
1:0	RW	0x0	gpio2b0_e GPIO2B0 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3

GRF_GPIO2C_E
Address: Operational Base + offset (0x0e108)
GPIO2C drive strength control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x0	gpio2c7_e GPIO2C7 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3
13:12	RW	0x0	gpio2c6_e GPIO2C6 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3
11:10	RW	0x0	gpio2c5_e GPIO2C5 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3
9:8	RW	0x0	gpio2c4_e GPIO2C4 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3

Bit	Attr	Reset Value	Description
7:6	RW	0x0	gpio2c3_e GPIO2C3 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3
5:4	RW	0x0	gpio2c2_e GPIO2C2 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3
3:2	RW	0x0	gpio2c1_e GPIO2C1 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3
1:0	RW	0x0	gpio2c0_e GPIO2C0 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3

GRF_GPIO2D_E
Address: Operational Base + offset (0x0e10c)
GPIO2D drive strength control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x0	gpio2d7_e GPIO2D7 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3
13:12	RW	0x0	gpio2d6_e GPIO2D6 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3
11:10	RW	0x0	gpio2d5_e GPIO2D5 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3
9:8	RW	0x0	gpio2d4_e GPIO2D4 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3

Bit	Attr	Reset Value	Description
7:6	RW	0x0	gpio2d3_e GPIO2D3 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3
5:4	RW	0x0	gpio2d2_e GPIO2D2 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3
3:2	RW	0x0	gpio2d1_e GPIO2D1 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3
1:0	RW	0x0	gpio2d0_e GPIO2D0 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3

GRF_GPIO3A_E01
Address: Operational Base + offset (0x0e110)
GPIO3A drive strength control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	gpio3a5_e0 GPIO3A5 drive strength control bit0
14:12	RW	0x0	gpio3a4_e GPIO3A4 drive strength control bit0 to bit2
11:9	RW	0x0	gpio3a3_e GPIO3A3 drive strength control bit0 to bit2
8:6	RW	0x0	gpio3a2_e GPIO3A2 drive strength control bit0 to bit2
5:3	RW	0x0	gpio3a1_e GPIO3A1 drive strength control bit0 to bit2
2:0	RW	0x0	gpio3a0_e GPIO3A0 drive strength control bit0 to bit2

GRF_GPIO3A_E2
Address: Operational Base + offset (0x0e114)
GPIO3B drive strength control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RO	0x0	reserved
7:5	RW	0x0	gpio3a7_e GPIO3A7 drive strength control bit0 to bit2
4:2	RW	0x0	gpio3a6_e GPIO3A6 drive strength control bit0 to bit2
1:0	RW	0x0	gpio3a5_e12 GPIO3A5 drive strength control bit1 and bit2

GRF_GPIO3B_E01
Address: Operational Base + offset (0x0e118)
GPIO3B drive strength control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	gpio3b5_e0 GPIO3B5 drive strength control bit0

Bit	Attr	Reset Value	Description
14:12	RW	0x0	gpio3b4_e GPIO3B4 drive strength control bit0 to bit2
11:9	RW	0x0	gpio3b3_e GPIO3B3 drive strength control bit0 to bit2
8:6	RW	0x0	gpio3b2_e GPIO3B2 drive strength control bit0 to bit2
5:3	RW	0x0	gpio3b1_e GPIO3B1 drive strength control bit0 to bit2
2:0	RW	0x0	gpio3b0_e GPIO3B0 drive strength control bit0 to bit2

GRF_GPIO3B_E2
Address: Operational Base + offset (0x0e11c)
GPIO3B drive strength control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RO	0x0	reserved
7:5	RW	0x0	gpio3b7_e GPIO3B7 drive strength control bit0 to bit2
4:2	RW	0x0	gpio3b6_e GPIO3B6 drive strength control bit0 to bit2
1:0	RW	0x0	gpio3b5_e12 GPIO3B5 drive strength control bit1 to bit2

GRF_GPIO3C_E01
Address: Operational Base + offset (0x0e120)
GPIO3C drive strength control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	gpio3c5_e0 GPIO3C5 drive strength control bit0
14:12	RW	0x0	gpio3c4_e GPIO3C4 drive strength control bit0 to bit2
11:9	RW	0x0	gpio3c3_e GPIO3C3 drive strength control bit0 to bit2
8:6	RW	0x0	gpio3c2_e GPIO3C2 drive strength control bit0 to bit2
5:3	RW	0x0	gpio3c1_e GPIO3C1 drive strength control bit0 to bit2
2:0	RW	0x0	gpio3c0_e GPIO3C0 drive strength control bit0 to bit2

GRF_GPIO3C_E2
Address: Operational Base + offset (0x0e124)
GPIO3C drive strength control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RO	0x0	reserved
7:5	RW	0x0	gpio3c7_e GPIO3C7 drive strength control bit0 to bit2
4:2	RW	0x0	gpio3c6_e GPIO3C6 drive strength control bit0 to bit2
1:0	RW	0x0	gpio3c5_e12 GPIO3C5 drive strength control bit1 and bit2

GRF_GPIO3D_E
Address: Operational Base + offset (0x0e128)
GPIO3D drive strength control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

Bit	Attr	Reset Value	Description
15:14	RW	0x0	gpio3d7_e GPIO3D7 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3
13:12	RW	0x0	gpio3d6_e GPIO3D6 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3
11:10	RW	0x0	gpio3d5_e GPIO3D5 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3
9:8	RW	0x0	gpio3d4_e GPIO3D4 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3
7:6	RW	0x0	gpio3d3_e GPIO3D3 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3
5:4	RW	0x0	gpio3d2_e GPIO3D2 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3

Bit	Attr	Reset Value	Description
3:2	RW	0x0	gpio3d1_e GPIO3D1 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3
1:0	RW	0x0	gpio3d0_e GPIO3D0 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3

GRF_GPIO4A_E
Address: Operational Base + offset (0x0e12c)
GPIO4A drive strength control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x0	gpio4a7_e GPIO4A7 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3

Bit	Attr	Reset Value	Description
13:12	RW	0x0	gpio4a6_e GPIO4A6 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3
11:10	RW	0x0	gpio4a5_e GPIO4A5 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3
9:8	RW	0x0	gpio4a4_e GPIO4A4 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3
7:6	RW	0x0	gpio4a3_e GPIO4A3 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3
5:4	RW	0x0	gpio4a2_e GPIO4A2 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3
3:2	RW	0x0	gpio4a1_e GPIO4A1 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3

Bit	Attr	Reset Value	Description
1:0	RW	0x0	gpio4a0_e GPIO4A0 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3

GRF_GPIO4B_E01
Address: Operational Base + offset (0x0e130)
GPIO4B drive strength control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x1	gpio4b5_e0 GPIO4B5 drive strength control bit0
14:12	RW	0x1	gpio4b4_e GPIO4B4 drive strength control bit0 to bit2
11:9	RW	0x1	gpio4b3_e GPIO4B3 drive strength control bit0 to bit2
8:6	RW	0x1	gpio4b2_e GPIO4B2 drive strength control bit0 to bit2
5:3	RW	0x1	gpio4b1_e GPIO4B1 drive strength control bit0 to bit2
2:0	RW	0x1	gpio4b0_e GPIO4B0 drive strength control bit0 to bit2

GRF_GPIO4B_E2
Address: Operational Base + offset (0x0e134)
GPIO4B drive strength control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RO	0x0	reserved
7:5	RW	0x0	gpio4b7_e GPIO4B7 drive strength control bit0 to bit2
4:2	RW	0x0	gpio4b6_e GPIO4B6 drive strength control bit0 to bit2
1:0	RW	0x0	gpio4b5_e12 GPIO4B5 drive strength control bit2

GRF_GPIO4C_E
Address: Operational Base + offset (0x0e138)
GPIO4C drive strength control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

Bit	Attr	Reset Value	Description
15:14	RW	0x0	gpio4c7_e GPIO4C7 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3
13:12	RW	0x0	gpio4c6_e GPIO4C6 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3
11:10	RW	0x0	gpio4c5_e GPIO4C5 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3
9:8	RW	0x0	gpio4c4_e GPIO4C4 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3
7:6	RW	0x0	gpio4c3_e GPIO4C3 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3
5:4	RW	0x0	gpio4c2_e GPIO4C2 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3

Bit	Attr	Reset Value	Description
3:2	RW	0x0	gpio4c1_e GPIO4C1 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3
1:0	RW	0x0	gpio4c0_e GPIO4C0 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3

GRF_GPIO4D_E
Address: Operational Base + offset (0x0e13c)
GPIO4D drive strength control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x0	gpio4d7_e GPIO4D7 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3

Bit	Attr	Reset Value	Description
13:12	RW	0x0	gpio4d6_e GPIO4D6 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3
11:10	RW	0x0	gpio4d5_e GPIO4D5 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3
9:8	RW	0x0	gpio4d4_e GPIO4D4 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3
7:6	RW	0x0	gpio4d3_e GPIO4D3 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3
5:4	RW	0x0	gpio4d2_e GPIO4D2 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3
3:2	RW	0x0	gpio4d1_e GPIO4D1 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3

Bit	Attr	Reset Value	Description
1:0	RW	0x0	gpio4d0_e GPIO4D0 drive strength control, every GPIO bit corresponding to 2bits 2'b00: level 0 2'b01: level 1 2'b10: level 2 2'b11: level 3

GRF_GPIO2C_HE
Address: Operational Base + offset (0x0e188)
GPIO2C HE control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RO	0x0	reserved
7:0	RW	0x00	gpio2c_he GPIO2C gpio keep privous state control, every GPIO bit corresponding to 1bit 1'b0: disable 1'b1: enable

GRF_GPIO2D_HE
Address: Operational Base + offset (0x0e18c)
GPIO2D HE control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:5	RO	0x0	reserved
4:0	RW	0x00	gpio2d_he GPIO2D gpio keep privous state control, every GPIO bit corresponding to 1bit 1'b0: disable 1'b1: enable

GRF_SOC_CON0
Address: Operational Base + offset (0x0e200)
SoC control register 0

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

Bit	Attr	Reset Value	Description
15	RW	0x0	emmc_fwd_perihp_pwrDiscTargPwrStall noc_emmc_fwd_perihp_rsp_err_stall bit control 0: error response 1: stall response
14	RW	0x0	centersrv_fwd_ccim1_pwrDiscTargPwrStall noc_centersrv_fwd_ccim1_rsp_err_stall bit control 0: error response 1: stall response
13	RW	0x0	center_fwd_vio_pwrDiscTargPwrStall noc_center_fwd_vio_rsp_err_stall bit control 0: error response 1: stall response
12	RW	0x0	center_fwd_vdu_pwrDiscTargPwrStall noc_center_fwd_vdu_rsp_err_stall bit control 0: error response 1: stall response
11	RW	0x0	center_fwd_vcodec_pwrDiscTargPwrStall noc_center_fwd_vcodec_rsp_err_stall bit control 0: error response 1: stall response
10	RW	0x0	center_fwd_usb3_pwrDiscTargPwrStall noc_center_fwd_usb3_rsp_err_stall bit control 0: error response 1: stall response
9	RW	0x0	center_fwd_rga_pwrDiscTargPwrStall noc_center_fwd_rga_rsp_err_stall bit control 0: error response 1: stall response
8	RW	0x0	center_fwd_perihp_pwrDiscTargPwrStall noc_center_fwd_perihp_rsp_err_stall bit control 0: error response 1: stall response
7	RW	0x0	center_fwd_iep_pwrDiscTargPwrStall noc_center_fwd_iep_rsp_err_stall bit control 0: error response 1: stall response
6	RW	0x0	center_fwd_gpu_pwrDiscTargPwrStall noc_center_fwd_gpu_rsp_err_stall bit control 0: error response 1: stall response

Bit	Attr	Reset Value	Description
5	RW	0x0	perilp_fwd_gmac_pwrDiscTargPwrStall perilp_fwd_gmac_rsp_err_stall bit control 0: error response 1: stall response
4	RW	0x0	perilp_fwd_emmc_pwrDiscTargPwrStall perilp_fwd_emmc_rsp_err_stall bit control 0: error response 1: stall response
3	RW	0x0	center_fwd_edp_pwrDiscTargPwrStall noc_center_fwd_edp_rsp_err_stall bit control 0: error response 1: stall response
2	RW	0x0	cci_req_msch1_pwrDiscTargPwrStall noc_cci_req_msch1_rsp_err_stall bit control 0: error response 1: stall response
1	RW	0x0	cci_req_msch0_pwrDiscTargPwrStall noc__rsp_err_stall bit control 0: error response 1: stall response
0	RW	0x0	cci_fwd_perilp_pwrDiscTargPwrStall noc_cci_fwd_perilp_rsp_err_stall bit control 0: error response 1: stall response

GRF_SOC_CON1
Address: Operational Base + offset (0x0e204)
SoC control register 2

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

Bit	Attr	Reset Value	Description
15	RW	0x0	perihp_fwd_cci_pwrDiscTargPwrStall noc_perihp_fwd_cci_rsp_err_stall bit control 0: error response 1: stall response
14	RW	0x0	perihp_fwd_alive_pwrDiscTargPwrStall noc_perihp_fwd_alive_rsp_err_stall bit control 0: error response 1: stall response
13	RW	0x0	perihp_cm0_fwd_perihp_pwrDiscTargPwrStall noc_perihp_cm0_fwd_perihp_rsp_err_stall bit control 0: error response 1: stall response
12	RW	0x0	perihp_req_msch1_pwrDiscTargPwrStall noc_perihp_req_msch1_rsp_err_stall bit control 0: error response 1: stall response
11	RW	0x0	perihp_req_msch0_pwrDiscTargPwrStall noc_perihp_req_msch0_rsp_err_stall bit control 0: error response 1: stall response
10	RW	0x0	perihp_fwd_center_pwrDiscTargPwrStall noc_perihp_fwd_center_rsp_err_stall bit control 0: error response 1: stall response
9	RW	0x0	pcie_fwd_perihp_pwrDiscTargPwrStall noc_pcie_fwd_perihp_rsp_err_stall bit control 0: error response 1: stall response
8	RW	0x0	msch1regsrv_fwd_msch1_pwrDiscTargPwrStall noc_msch1regsrv_fwd_msch1_rsp_err_stall bit control 0: error response 1: stall response

Bit	Attr	Reset Value	Description
7	RW	0x0	msch0regsrv_fwd_msch0_pwrDiscTargPwrStall noc_msch0regsrv_fwd_msch0_rsp_err_stall bit control 0: error response 1: stall response
6	RW	0x0	isp1_req_msch01_pwrDiscTargPwrStall noc_isp1_req_msch01_rsp_err_stall bit control 0: error response 1: stall response
5	RW	0x0	isp0_req_msch01_pwrDiscTargPwrStall noc_isp0_req_msch01_rsp_err_stall bit control 0: error response 1: stall response
4	RW	0x0	iep_req_msch1_pwrDiscTargPwrStall noc_iep_req_msch1_rsp_err_stall bit control 0: error response 1: stall response
3	RW	0x0	iep_req_msch0_pwrDiscTargPwrStall noc_iep_req_msch0_rsp_err_stall bit control 0: error response 1: stall response
2	RW	0x0	hdcp_req_msch01_pwrDiscTargPwrStall noc_hdcp_req_msch01_rsp_err_stall bit control 0: error response 1: stall response
1	RW	0x0	gpu_req_msch1_pwrDiscTargPwrStall noc_gpu_req_msch1_rsp_err_stall bit control 0: error response 1: stall response
0	RW	0x0	gpu_req_msch0_pwrDiscTargPwrStall noc_gpu_req_msch0_rsp_err_stall bit control 0: error response 1: stall response

GRF_SOC_CON2

Address: Operational Base + offset (0x0e208)

SoC control register 1

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable Fbit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	vio0_req_msch0_pwrDiscTargPwrStall noc_vio0_req_msch0_rsp_err_stall bit control 0: error response 1: stall response
14	RW	0x0	vdu_req_msch1_pwrDiscTargPwrStall noc_vdu_req_msch1_rsp_err_stall bit control 0: error response 1: stall response
13	RW	0x0	vdu_req_msch0_pwrDiscTargPwrStall noc_vdu_req_msch0_rsp_err_stall bit control 0: error response 1: stall response
12	RW	0x0	vcodec_req_msch1_pwrDiscTargPwrStall noc_vcodec_req_msch1_rsp_err_stall bit control 0: error response 1: stall response
11	RW	0x0	vcodec_req_msch0_pwrDiscTargPwrStall noc_vcodec_req_msch0_rsp_err_stall bit control 0: error response 1: stall response
10	RW	0x0	usb3_req_msch1_pwrDiscTargPwrStall noc_usb3_req_msch1_rsp_err_stall bit control 0: error response 1: stall response

Bit	Attr	Reset Value	Description
9	RW	0x0	usb3_req_msch0_pwrDiscTargPwrStall noc_usb3_req_msch0_rsp_err_stall bit control 0: error response 1: stall response
8	RW	0x0	rga_req_msch1_pwrDiscTargPwrStall noc_rga_req_msch1_rsp_err_stall bit control 0: error response 1: stall response
7	RW	0x0	rga_req_msch0_pwrDiscTargPwrStall noc_rga_req_msch0_rsp_err_stall bit control 0: error response 1: stall response
6	RW	0x0	sdioaudio_fwd_perilp_pwrDiscTargPwrStall noc_pmu_fwd_perilp_rsp_err_stall bit control 0: error response 1: stall response
5	RW	0x0	gmac_fwd_perihp_pwrDiscTargPwrStall noc_gmac_fwd_perihp_rsp_err_stall bit control 0: error response 1: stall response
4	RW	0x0	perilpsrv_fwd_cm0_pwrDiscTargPwrStall noc_perilpsrv_fwd_cm0_rsp_err_stall bit control 0: error response 1: stall response
3	RW	0x0	perilp_req_msch1_pwrDiscTargPwrStall noc_perilp_req_msch1_rsp_err_stall bit control 0: error response 1: stall response
2	RW	0x0	perilp_req_msch0_pwrDiscTargPwrStall noc_perilp_req_msch0_rsp_err_stall bit control 0: error response 1: stall response
1	RW	0x0	perilp_fwd_pmu_pwrDiscTargPwrStall noc_perilp_fwd_pmu_rsp_err_stall bit control 0: error response 1: stall response

Bit	Attr	Reset Value	Description
0	RW	0x0	perilp_fwd_center_pwrDiscTargPwrStall noc_perilp_fwd_center_rsp_err_stall bit control 0: error response 1: stall response

GRF_SOC_CON3
Address: Operational Base + offset (0x0e20c)
SoC control register 3

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	perihp_fwd_sd_pwrDiscTargPwrStall noc_perihp_fwd_sd_rsp_err_stall bit control 0: error response 1: stall response
14	RW	0x0	gic_fwd_perilp_pwrDiscTargPwrStall noc_gic_fwd_perilp_rsp_err_stall bit control 0: error response 1: stall response
13	RW	0x0	sd_fwd_perihp_pwrDiscTargPwrStall noc_sd_fwd_perihp_rsp_err_stall bit control 0: error response 1: stall response
12	RW	0x0	vopl_req_msch11_pwrDiscTargPwrStall noc_vopl_req_msch11_rsp_err_stall bit control 0: error response 1: stall response

Bit	Attr	Reset Value	Description
11	RW	0x0	vopb_req_msch11_pwrDiscTargPwrStall noc_vopb_req_msch11_rsp_err_stall bit control 0: error response 1: stall response
10	RW	0x0	vio_fwd_hdcp_pwrDiscTargPwrStall noc_vio_fwd_hdcp_rsp_err_stall bit control 0: error response 1: stall response
9	RW	0x0	vio_fwd_vopl_pwrDiscTargPwrStall noc_vio_fwd_vopl_rsp_err_stall bit control 0: error response 1: stall response
8	RW	0x0	vio_fwd_vopb_pwrDiscTargPwrStall noc_vio_fwd_vopb_rsp_err_stall bit control 0: error response 1: stall response
7	RW	0x0	vio_fwd_isp1_pwrDiscTargPwrStall noc_vio_fwd_isp1_rsp_err_stall bit control 0: error response 1: stall response
6	RW	0x0	vio_fwd_isp0_pwrDiscTargPwrStall noc_vio_fwd_isp0_rsp_err_stall bit control 0: error response 1: stall response
5	RW	0x0	usb3_fwd_perilp_pwrDiscTargPwrStall noc_usb3_fwd_perilp_rsp_err_stall bit control 0: error response 1: stall response
4	RW	0x0	viol_req_msch01_pwrDiscTargPwrStall noc_viol_req_msch01_rsp_err_stall bit control 0: error response 1: stall response
3	RW	0x0	viob_req_msch01_pwrDiscTargPwrStall noc_viob_req_msch01_rsp_err_stall bit control 0: error response 1: stall response
2	RW	0x0	vio1_req_msch1_pwrDiscTargPwrStall noc_vio1_req_msch1_rsp_err_stall bit control 0: error response 1: stall response

Bit	Attr	Reset Value	Description
1	RW	0x0	vio1_req_msch0_pwrDiscTargPwrStall noc_vio1_req_msch0_rsp_err_stall bit control 0: error response 1: stall response
0	RW	0x0	vio0_req_msch1_pwrDiscTargPwrStall noc_vio0_req_msch1_rsp_err_stall bit control 0: error response 1: stall response

GRF_SOC_CON4
Address: Operational Base + offset (0x0e210)
SoC control register 4

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RO	0x0	reserved
14	RW	0x0	perilp_fwd_centerslv_pwrDiscTargPwrStall noc_perilp_fwd_centerslv_rsp_err_stall bit control 0: error response 1: stall response
13	RW	0x0	perilp_fwd_sdioaudio_pwrDiscTargPwrStall noc_perilp_fwd_sdioaudio_rsp_err_stall bit control 0: error response 1: stall response
12	RW	0x0	perilp_fwd_gic_pwrDiscTargPwrStall noc_perilp_fwd_gic_rsp_err_stall bit control 0: error response 1: stall response

Bit	Attr	Reset Value	Description
11:9	RW	0x0	ddr_debug_sel select ddr debug port 0: ddr_dbug_port[7:0] 1: ddr_dbug_port[15:8] 2: ddr_dbug_port[23:16] 3: ddr_dbug_port[31:24] 4: ddr_dbug_port[39:32] 5: ddr_dbug_port[47:40] 6: ddr_dbug_port[55:48] 7: ddr_dbug_port[63:56]
8	RW	0x1	cci_force_wakeup cci force wakeup control 1'b0: disable 1'b1: enable
7:6	RW	0x0	cci_qosoverride cci port QOSOVERRIDE bit control
5:4	RW	0x0	cci_ordered_wr_obsv cci port ORDERED_WRITE_OBSERVATION control
3:2	RW	0x3	acchannelens1_cci500 CCI ACCHANNELEN input control. Slave interface supports DVM messages. This is overridden to 0x0 if you set the Control Override Register[1].
1:0	RW	0x3	acchannelens0_cci500 CCI ACCHANNELEN input control. Slave interface supports DVM messages. This is overridden to 0x0 if you set the Control Override Register[1].

GRF_SOC_CON_5_PCIE

Address: Operational Base + offset (0x0e214)

SoC control register 5

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:7	RO	0x0	reserved
6:3	RW	0x0	pcie_tx_elec_idle_off pcie_tx_elec_idle_off[3:0] port control
2	RW	0x0	pcie_rx_elec_idle_irq_en pcie_rx_elec_idle_irq_en port control
1	RW	0x1	pcie_tx_elec_idle_set pcie_tx_elec_idle_set port control
0	RW	0x0	pcie_tx_elec_idle_sel pcie_tx_elec_idle_sel port control

GRF_SOC_CON7
Address: Operational Base + offset (0x0e21c)
SoC control register 7

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

Bit	Attr	Reset Value	Description
15	RW	0x0	gic_awuser_mode gic_awuser mode select 1: address mode 0: user mode
14	RW	0x0	pcie_clkreq_sel pcie_clkreq_sel port control
13	RO	0x0	reserved
12	RW	0x1	grf_con_force_jtag
11:10	RW	0x0	grf_uart_dbg_sel
9:5	RW	0x00	grf_uart_rts_sel uart_rts_sel bit control UART polarity selection for rts port Every bit for one UART. 1'b1: invert uart_rts_n 1'b0: keep the rts_n value from UART module output
4:0	RW	0x00	grf_uart_cts_sel UART polarity selection for cts port Every bit for one UART. 1'b1: invert uart_cts_n 1'b0: keep the cts_n value from IO

GRF_SOC_CON8

Address: Operational Base + offset (0x0e220)

SoC control register 8

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RO	0x0	reserved

Bit	Attr	Reset Value	Description
14:11	RW	0x0	i2s0_sclk_oe_n i2s0_sclk_oe_n bit control
10:7	RW	0x0	pcie_test_i pci test input
6:1	RW	0x00	pcie_test_addr pci test address control
0	RW	0x0	pcie_test_write pcie test write control 1'b0: disable 1'b1: enable

GRF_SOC_CON_9_PCIE
Address: Operational Base + offset (0x0e224)
SoC control register 9 for PCIE

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:1	RO	0x0	reserved
0	RW	0x0	pcie_rc_mode_idle_irq_clr irq clear bit for pcie_rc_mode_idle_irq

GRF_SOC_STATUS0
Address: Operational Base + offset (0x0e2a0)
SOC status register 0

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	ddr1_mem_rst_valid status bit of ddr1_mem_rst_valid
23	RW	0x0	ddr1_q_almost_full status bit of ddr1_q_almost_full

Bit	Attr	Reset Value	Description
22	RW	0x0	ddr1_refresh_in_process status bit of ddr1_refresh_in_process
21	RW	0x0	ddr1_controller_busy status bit of ddr1_controller_busy
20	RW	0x0	ddr1_port_busy status bit of ddr1_port_busy
19:18	RW	0x0	ddr1_zq_status_out status bit of ddr1_zq_status_out
17:16	RW	0x0	ddr1_cke_status status bit of ddr1_cke_status
15:9	RO	0x0	reserved
8	RW	0x0	ddr0_mem_rst_valid status bit of ddr0_mem_rst_valid
7	RW	0x0	ddr0_q_almost_full status bit of ddr0_q_almost_full
6	RW	0x0	ddr0_refresh_in_process status bit of ddr0_refresh_in_process
5	RW	0x0	ddr0_controller_busy status bit of ddr0_controller_busy
4	RW	0x0	ddr0_port_busy status bit of ddr0_port_busy
3:2	RW	0x0	ddr0_zq_status_out status bit of ddr0_zq_status_out
1:0	RW	0x3	ddr0_cke_status status bit of ddr0_cke_status

GRF_SOC_STATUS1
Address: Operational Base + offset (0x0e2a4)
SOC status register 1

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:8	RW	0x0	grf_pcie_test_o status bit of grf_pcie_test_o
7:0	RW	0x00	dphy_rx0_testdout status bit of dphy_rx0_testdout

GRF_SOC_STATUS2
Address: Operational Base + offset (0x0e2a8)
SOC status register 2

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10	RW	0x0	m0_perilp_cdbgpwrupreq m0_perilp_cdbgpwrupreq status bit
9	RW	0x0	m0_perilp_sysresetreq m0_perilp_sysresetreq

Bit	Attr	Reset Value	Description
8	RW	0x0	jtagnsw_st status bit of jtagnsw_st
7	RW	0x0	jtagtop_st status bit of jtagtop_st
6	RW	0x0	txev_m0_perilp status bit of xev_m0_perilp
5	RW	0x0	m0_perilp_dbgrestarted status bit of m0_perilp_dbgrestarted
4	RW	0x0	m0_perilp_halted status bit of m0_perilp_halted
3	RW	0x0	m0_perilp_core_lockup status bit of m0_perilp_core_lockup
2	RW	0x0	m0_perilp_sleepdeep status bit of m0_perilp_sleeping
1	RW	0x0	m0_perilp_sleeping status bit of m0_perilp_sleeping
0	RW	0x0	m0_perilp_wakeup status bit of m0_perilp_wakeup

GRF_SOC_STATUS3
Address: Operational Base + offset (0x0e2ac)
SOC status register 3

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RO	0x0	usbcphy1_host_utmi_hostdisconnect usbcphy1_host_utmi_hostdisconnect status
26:25	RO	0x0	usbcphy1_host_utmi_linestate usbcphy1_host_utmi_linestate status
24	RO	0x0	usbcphy1_host_utmi_fs_xver_own 1: ohci owns usb2phy 0: ehci owns usb2phy
23	RO	0x0	usbcphy0_host_utmi_hostdisconnect usbcphy0_host_utmi_hostdisconnect status
22:21	RO	0x0	usbcphy0_host_utmi_linestate usbcphy0_host_utmi_linestate status
20	RO	0x0	usbcphy0_host_utmi_fs_xver_own 1: ohci owns usb2phy 0: ehci owns usb2phy
19	RO	0x0	usbcphy1_otg_utmi_hostdisconnect usbcphy1_otg_utmi_hostdisconnect status
18:17	RO	0x0	usbcphy1_otg_utmi_linestate usbcphy1_otg_utmi_linestate status bit
16	RO	0x0	usbcphy1_otg_utmi_bvalid usbcphy1_otg_utmi_bvalid status bit

Bit	Attr	Reset Value	Description
15	RO	0x0	usbcphy0_otg_utmi_hostdisconnect usbcphy0_otg_utmi_hostdisconnect status
14:13	RO	0x0	usbcphy0_otg_utmi_linestate usbcphy0_otg_utmi_linestate status bit
12	RO	0x0	usbcphy0_otg_utmi_bvalid usbcphy0_otg_utmi_bvalid status bit
11	RW	0x0	usbcphy1_otg_utmi_iddig usbcphy1_otg_utmi_iddig status bit
10	RW	0x0	usbcphy1_otg_utmi_avalid usbcphy1_otg_utmi_avalid status bit
9	RW	0x0	usbcphy1_otg_utmi_sessend usbcphy1_otg_utmi_sessend status bit
8	RW	0x0	usbcphy0_otg_utmi_iddig usbcphy0_otg_utmi_iddig status bit
7	RW	0x0	usbcphy0_otg_utmi_avalid usbcphy0_otg_utmi_avalid status bit
6	RW	0x0	usbcphy0_otg_utmi_sessend usbcphy0_otg_utmi_sessend status bit
5	RW	0x0	usb20_phy1_stat_cp_detected usb20_phy1_stat_cp_detected status bit
4	RW	0x0	usb20_phy1_stat_dcp_detected usb20_phy1_stat_dcp_detected status bit
3	RW	0x0	usb20_phy1_stat_dp_attached usb20_phy1_stat_dp_attached status bit
2	RW	0x0	usb20_phy0_stat_cp_detected usb20_phy0_stat_cp_detected status bit
1	RW	0x0	usb20_phy0_stat_dcp_detected usb20_phy0_stat_dcp_detected status bit
0	RW	0x0	usb20_phy0_stat_dp_attached usb20_phy0_stat_dp_attached status bit

GRF_SOC_STATUS4
Address: Operational Base + offset (0x0e2b0)
SOC status register 4

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ddr_monitor ddr_monitor[31:0] status bit

GRF_SOC_STATUS5
Address: Operational Base + offset (0x0e2b4)
SOC status register 5

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:0	RW	0x00000000	ddr_monitor ddr_monitor[62:32] status bit

GRF_DDRC0_CON0
Address: Operational Base + offset (0x0e380)
ddrc0 control register 0

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:13	RO	0x0	reserved
12	RW	0x1	ddr0_oe_polarity bit control of ddr0_oe_polarity
11	RW	0x1	ddr0_dram_clk_enable_polarity bit control of ddr0_dram_clk_enable_polarity
10	RW	0x1	ddr0_io_ctrl_oe_polarity bit control of ddr0_io_ctrl_ie_polarity
9	RW	0x1	ddr0_io_ctrl_ie_polarity bit control of ddr0_io_ctrl_ie_polarity
8	RW	0x1	ddr0_ie_polarity bit control of ddr0_ie_polarity
7	RW	0x1	ddr0_tsel_en_polarity bit control of ddr0_tsel_en_polarity
6:3	RO	0x0	reserved
2	RW	0x0	ddr0_lp4_addr_dup bit conrol of ddr0_lp4_addr_dup
1:0	RW	0x1	ddr0_zq_status_in bit control of ddr0_zq_status_in

GRF_DDRC0_CON1
Address: Operational Base + offset (0x0e384)
ddrc0 control register 1

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:10	RO	0x0	reserved
9:8	RW	0x0	denali0_command_priority bit control of denali0_command_priority
7	RW	0x0	clk_ddr0_msch_en_stdby bit control of clk_ddr0_msch_en_stdby
6	RW	0x0	clk_ddrphy0_en_stdby bit control of clk_ddrphy0_en_stdby
5	RW	0x0	clk_ddrphy_ctrl0_en_stdby bit control of clk_ddrc0_en_stdby
4	RW	0x0	clk_ddrc0_en_stdby bit control of clk_ddrc0_en_stdby
3:0	RO	0x0	reserved

GRF_DDRC1_CON0
Address: Operational Base + offset (0x0e388)
ddrc1 control register 0

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:13	RO	0x0	reserved
12	RW	0x1	ddr1_oe_polarity bit control of ddr1_oe_polarity
11	RW	0x1	ddr1_dram_clk_enable_polarity bit control of ddr1_dram_clk_enable_polarity
10	RW	0x1	ddr1_io_ctrl_oe_polarity bit control of ddr1_io_ctrl_oe_polarity
9	RW	0x1	ddr1_io_ctrl_ie_polarity bit control of ddr1_io_ctrl_ie_polarity
8	RW	0x1	ddr1_ie_polarity bit control of ddr1_ie_polarity
7	RW	0x1	ddr1_tsel_en_polarity bit control of ddr1_tsel_en_polarity
6:3	RO	0x0	reserved
2	RW	0x0	ddr1_lp4_addr_dup bit control of ddr1_lp4_addr_dup
1:0	RW	0x1	ddr1_zq_status_in bit control of ddr1_zq_status_in

GRF_DDRC1_CON1

Address: Operational Base + offset (0x0e38c)

ddrc1 control register 1

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:10	RO	0x0	reserved
9:8	RW	0x0	denali1_command_priority bit control of denali1_command_priority
7	RW	0x0	clk_ddr1_msch_en_stdby bit control of clk_ddr1_msch_en_stdby
6	RW	0x0	clk_ddrphy1_en_stdby bit control of clk_ddrphy1_en_stdby
5	RW	0x0	clk_ddrphy_ctrl1_en_stdby bit control of clk_ddrphy_ctrl1_en_stdby
4	RW	0x0	clk_ddrc1_en_stdby bit control of clk_ddrc1_en_stdby
3:0	RO	0x0	reserved

GRF_SIG_DETECT_CON0
Address: Operational Base + offset (0x0e3c0)
Singal detect control register0

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	uphy1_rxdet_en uphy1_rxdet phy conrol bit
14	RW	0x0	uphy0_rxdet_en uphy0_rxdet phy conrol bit
13	RW	0x0	uphy1_rxdet_change uphy1_rxdet_change detect control 1'b0: disbale 1'b1: enable
12	RW	0x0	uphy0_rxdet_change uphy0_rxdet_change detect control 1'b0: disbale 1'b1: enable
11	RW	0x0	cphy1_host_linestate_change cphy1_host_linestate_change detect control 1'b0: disbale 1'b1: enable
10	RW	0x0	cphy1_otg_id_fall cphy1_otg_id_fall detect control 1'b0: disbale 1'b1: enable
9	RW	0x0	cphy1_otg_id_rise cphy1_otg_id_rise detect control 1'b0: disbale 1'b1: enable
8	RW	0x0	cphy1_otg_bvalid_rise cphy1_otg_bvalid_rise detect control 1'b0: disbale 1'b1: enable

Bit	Attr	Reset Value	Description
7	RW	0x0	cphy1_otg_linestate_change cphy1_otg_linestate_change detect control 1'b0: disbale 1'b1: enable
6	RW	0x0	cphy0_host_linestate_change cphy0_host_linestate_change detect control 1'b0: disbale 1'b1: enable
5	RW	0x0	cphy0_otg_id_fall cphy0_otg_id_fall detect control 1'b0: disbale 1'b1: enable
4	RW	0x0	cphy0_otg_id_rise cphy0_otg_id_rise detect control 1'b0: disbale 1'b1: enable
3	RW	0x0	cphy0_otg_bvalid_rise cphy0_otg_bvalid_rise detect control 1'b0: disbale 1'b1: enable
2	RW	0x0	cphy0_otg_linestate_change cphy0_otg_linestate_change detect control 1'b0: disbale 1'b1: enable
1	RW	0x0	sdmmc_card_fall_edge sdmmc card fall edge detect control 1'b0: disbale 1'b1: enable
0	RW	0x0	sdmmc_card_rise_edge sdmmc card rise edge detect control 1'b0: disbale 1'b1: enable

GRF_SIG_DETECT_CON1
Address: Operational Base + offset (0x0e3c8)
Singal detect control register1

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RO	0x0	reserved
13:12	RW	0x0	host0_llinestate_filter_time_sel filter time select 00: 100us 01: 500us 10: 1ms 11: 10ms
11:10	RW	0x0	otg0_llinestate_filter_time_sel filter time select 00: 100us 01: 500us 10: 1ms 11: 10ms
9:8	RW	0x0	otg0_id_filter_time_sel filter time select 00: 5ms 01: 15ms 10: 35ms 11: 50ms
7:0	RO	0x0	reserved

GRF_SIG_DETECT_CLR

Address: Operational Base + offset (0x0e3d0)

Signal detect status clear register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RO	0x0	reserved
13	RW	0x0	uphy1_rxdet_change uphy1_rxdet_change detect control 1'b0: disbale 1'b1: enable
12	RW	0x0	uphy0_rxdet_change uphy0_rxdet_change detect control 1'b0: disbale 1'b1: enable
11	RW	0x0	cphy1_host_linestate_change cphy1_host_linestate_change detect control 1'b0: disbale 1'b1: enable
10	RW	0x0	cphy1_otg_id_fall cphy1_otg_id_fall detect control 1'b0: disbale 1'b1: enable
9	RW	0x0	cphy1_otg_id_rise cphy1_otg_id_rise detect control 1'b0: disbale 1'b1: enable
8	RW	0x0	cphy1_otg_bvalid_rise cphy1_otg_bvalid_rise detect control 1'b0: disbale 1'b1: enable
7	RW	0x0	cphy1_otg_linestate_change cphy1_otg_linestate_change detect control 1'b0: disbale 1'b1: enable

Bit	Attr	Reset Value	Description
6	RW	0x0	cphy0_host_linestate_change cphy0_host_linestate_change detect control 1'b0: disbale 1'b1: enable
5	RW	0x0	cphy0_otg_id_fall cphy0_otg_id_fall detect control 1'b0: disbale 1'b1: enable
4	RW	0x0	cphy0_otg_id_rise cphy0_otg_id_rise detect control 1'b0: disbale 1'b1: enable
3	RW	0x0	cphy0_otg_bvalid_rise cphy0_otg_bvalid_rise detect control 1'b0: disbale 1'b1: enable
2	RW	0x0	cphy0_otg_linestate_change cphy0_otg_linestate_change detect control 1'b0: disbale 1'b1: enable
1	RW	0x0	sdmmc_card_fall_edge sdmmc card fall edge detect control 1'b0: disbale 1'b1: enable
0	RW	0x0	sdmmc_card_rise_edge sdmmc card rise edge detect control 1'b0: disbale 1'b1: enable

GRF_SIG_DETECT_STATUS
Address: Operational Base + offset (0x0e3e0)
Signal detect status register

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13	RW	0x0	uphy1_rxdet_change uphy1_rxdet_change detect status
12	RW	0x0	uphy0_rxdet_change uphy0_rxdet_change detect status
11	RW	0x0	cphy1_host_linestate_change cphy1_host_linestate_change detect status
10	RW	0x0	cphy1_otg_id_fall cphy1_otg_id_fall detect status
9	RW	0x0	cphy1_otg_id_rise cphy1_otg_id_rise detect status

Bit	Attr	Reset Value	Description
8	RW	0x0	cphy1_otg_bvalid_rise cphy1_otg_bvalid_rise detect status
7	RW	0x0	cphy1_otg_linestate_change cphy1_otg_linestate_change detect status
6	RW	0x0	cphy0_host_linestate_change cphy0_host_linestate_change detect status
5	RW	0x0	cphy0_otg_id_fall cphy0_otg_id_fall detect status
4	RW	0x0	cphy0_otg_id_rise cphy0_otg_id_rise detect status
3	RW	0x0	cphy0_otg_bvalid_rise cphy0_otg_bvalid_rise detect status
2	RW	0x0	cphy0_otg_linestate_change cphy0_otg_linestate_change detect status
1	RW	0x0	sdmmc_card_fall_edge sdmmc card fall edge detect status
0	RW	0x0	sdmmc_card_rise_edge sdmmc card rise edge detect status

GRF_USB20_PHY0_CON0
Address: Operational Base + offset (0x0e450)
USB20 PHY0 GRF Register 0

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:13	RO	0x0	reserved
12	RW	0x0	vdm_src_en vdm_src_en 1: enable vdm_src for battery charge for usb3otg0

Bit	Attr	Reset Value	Description
11	RW	0x0	vdp_src_en vdp_src_en 1:enable vdp_src for battery charge for usb3otg0
10	RW	0x0	rdm_pdwn_en rdm_pdwn_en 1: enable rdm_pdwn for battery charge for usb3otg0
9	RW	0x0	idp_src_en idp_src_en 1: enable idp_src for battery charge for usb3otg0
8	RW	0x0	idm_sink_en idm_sink_en 1: enable idm_sink for battery charge for usb3otg0
7	RW	0x0	idp_sink_en idp_sink_en 1: enable idp_sink for battery charge for usb3otg0
6:5	RO	0x0	reserved
4	RW	0x0	otg_commononn otg_commononn configure pll clock output in suspend mode
3	RW	0x0	bypasssel bypasssel 1: bypass DP/DM as uart sin/sout for usb3otg0 0: Normal USB function for usb3otg0
2	RW	0x0	bypassdmen bypassdmen 1: enable bypass uart_sout to DM for usb3otg0 0: disable bypass uart_sout to DM for usb3otg0
1	RW	0x0	otg_disable_1 otg_disable_1 1:disable otg function of usb20 host0 0:enable otg function of usb20 host0
0	RW	0x0	otg_disable_0 otg_disable_0 1:disable otg function of usb3otg0 0:enable otg function of usb3otg0

GRF_USB20_PHY0_CON1

Address: Operational Base + offset (0x0e454)
USB20 PHY0 GRF Register 1

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:13	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
12	RW	0x1	suspend_n_sel1 suspend_n_sel1 Pls see suspend_n.
11	RW	0x0	suspend_n_sel suspend_n_sel Pls see suspend_n.
10	RW	0x1	iddig iddig Select the value of this register to usb3otg0 register
9	RW	0x0	iddig_sel iddig_sel 1: select the value of bit10 of USB20_PHY0_CON1 to usb3otg0 controller 0: select the iddig from usb2phy to usb3otg0 controller
8	RW	0x0	dmpulldown dmpulldown Select the value of this register to usb2phy when utmi_sel=1
7	RW	0x0	dppulldown dppulldown Select the value of this register to usb2phy when utmi_sel=1
6	RW	0x1	termselect termselect Select the value of this register to usb2phy when utmi_sel=1

Bit	Attr	Reset Value	Description
5:4	RW	0x1	xcvrselect xcvrselect Select the value of this register to usb2phy when utmi_sel=1
3:2	RW	0x0	opmode opmode Select the value of this register to usb2phy when utmi_sel=1
1	RW	0x1	suspend_n suspend_n utmi_sel=1, select the value of this register to usb2phy utmi_sel=0 and bit11 of USB20_PHY0_CON1=0, and bit 12 of USB20_PHY0_CON1=0 select the value of the value of this bit to usb2phy utmi_sel=0 and bit11 of USB20_PHY0_CON1=0, and bit 12 of USB20_PHY0_CON1=1 select suspend_n signals from usb3otg0 controller to usb2phy for free running utmi clock utmi_sel=0 and bit11 of USB20_PHY0_CON1=1, select suspend_com_n signals from usb3otg0 controller to usb2phy for not free running utmi clock
0	RW	0x0	utmi_sel utmi_sel 1: select utmi interface signals from GRF reister to usb2phy 0: select utmi interface signals from utmi interface of usb3otg0 controller to usb2phy

GRF_USB20_PHY0_CON2

Address: Operational Base + offset (0x0e458)

USB20 PHY0 GRF Register 2

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:10	RO	0x0	reserved
9	RW	0x1	idpullup idpullup Use the value of this register input to idpullup of usb2phy
8	RW	0x1	dmpulldown dmpulldown Use the value of this register input to dmpulldown of usb2phy
7	RW	0x1	dppulldown dppulldown Use the value of this register input to dppulldown of usb2phy
6	RW	0x1	termselect termselect Select the value of this register to usb2phy when utmi_sel=1
5:4	RW	0x1	xcvrselect xcvrselect Select the value of this register to usb2phy when utmi_sel=1
3:2	RW	0x0	opmode opmode Select the value of this register to usb2phy when utmi_sel=1
1	RW	0x1	suspend_n suspend_n Select the value of this register to usb2phy when utmi_sel=1

Bit	Attr	Reset Value	Description
0	RW	0x0	utmi_sel utmi_sel 1: select utmi interface signals from GRF reister to usb2phy 0: select utmi interface signals from utmi interface of usb20 host0 controller to usb2phy

GRF_USB20_PHY0_CON3
Address: Operational Base + offset (0x0e45c)
USB20 PHY0 GRF Register 3

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:5	RO	0x0	reserved
4	RW	0x0	dischrgvbus dischrgvbus Use the value of this register input to chrgvbus of usb2phy
3	RW	0x0	chrgvbus chrgvbus Use the value of this register input to chrgvbus of usb2phy
2	RW	0x0	drvvbus drvvbus Pls see drvvbus_sel.

Bit	Attr	Reset Value	Description
1	RW	0x0	drvvbus_sel drvvbus_sel 1: select the value of bit2 of USB20_PHY0_CON3 to drvvbus of usb2phy and GPIO to external PMIC 0: select drvvbus from usb3otg0 controller to drvvbus of usb2phy and GPIO to external PMIC
0	RW	0x1	idpullup idpullup Use the value of this register input to idpullup of usb2phy

GRF_USB20_PHY1_CON0
Address: Operational Base + offset (0x0e460)
USB20 PHY1 GRF Register 0

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:13	RO	0x0	reserved
12	RW	0x0	vdm_src_en vdm_src_en 1: enable vdm_src for battery charge for usb3otg1
11	RW	0x0	vdp_src_en vdp_src_en 1:enable vdp_src for battery charge for usb3otg1
10	RW	0x0	rdm_pdwn_en rdm_pdwn_en 1: enable rdm_pdwn for battery charge for usb3otg1

Bit	Attr	Reset Value	Description
9	RW	0x0	idp_src_en idp_src_en 1: enable idp_src for battery charge for usb3otg1
8	RW	0x0	idm_sink_en idm_sink_en 1: enable idm_sink for battery charge for usb3otg1
7	RW	0x0	idp_sink_en idp_sink_en 1: enable idp_sink for battery charge for usb3otg1
6:5	RO	0x0	reserved
4	RW	0x0	otg_commononn otg_commononn configure pll clock output in suspend mode
3	RW	0x0	bypasssel bypasssel 1: bypass DP/DM as uart sin/sout for usb3otg1 0: Normal USB function for usb3otg1
2	RW	0x0	bypassdmen bypassdmen 1: enable bypass uart_sout to DM for usb3otg1 0: disable bypass uart_sout to DM for usb3otg1
1	RW	0x0	otg_disable_1 otg_disable_1 1:disable otg function of usb2 host1 0:enable otg function of usb2 host1
0	RW	0x0	otg_disable_0 otg_disable_0 1:disable otg function of usb3otg1 0:enable otg function of usb3otg1

GRF_USB20_PHY1_CON1
Address: Operational Base + offset (0x0e464)
USB20 PHY1GRF Register 1

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved

Bit	Attr	Reset Value	Description
28:13	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
12	RW	0x1	suspend_n_sel1 suspend_n-_sel1 Pls see suspend_n.
11	RW	0x0	suspend_n_sel suspend_n_sel Pls see suspend_n.
10	RW	0x1	iddig iddig Select the value of this register to usb3otg1 register
9	RW	0x0	iddig_sel iddig_sel 1: select the value of bit10 of USB20_PHY0_CON1 to usb3otg1 controller 0: select the iddig from usb2phy to usb3otg1 controller
8	RW	0x0	dmpulldown dmpulldown Select the value of this register to usb2phy when utmi_sel=1
7	RW	0x0	dppulldown dppulldown Select the value of this register to usb2phy when utmi_sel=1
6	RW	0x1	termselect termselect Select the value of this register to usb2phy when utmi_sel=1

Bit	Attr	Reset Value	Description
5:4	RW	0x1	xcvrselect xcvrselect Select the value of this register to usb2phy when utmi_sel=1
3:2	RW	0x0	opmode opmode Select the value of this register to usb2phy when utmi_sel=1
1	RW	0x1	suspend_n suspend_n utmi_sel=1, select the value of this register to usb2phy utmi_sel=0 and bit11 of USB20_PHY0_CON1=0, and bit 12 of USB20_PHY0_CON1=0 select the value of the value of this bit to usb2phy utmi_sel=0 and bit11 of USB20_PHY0_CON1=0, and bit 12 of USB20_PHY0_CON1=1 select suspend_n signals from usb3otg0 controller to usb2phy for free running utmi clock utmi_sel=0 and bit11 of USB20_PHY0_CON1=1, select suspend_com_n signals from usb3otg0 controller to usb2phy for not free running utmi clock
0	RW	0x0	utmi_sel utmi_sel 1: select utmi interface signals from GRF reister to usb2phy 0: select utmi interface signals from utmi interface of usb3otg1 controller to usb2phy

GRF_USB20_PHY1_CON2

Address: Operational Base + offset (0x0e468)

USB20 PHY1 GRF Register 2

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:10	RO	0x0	reserved
9	RW	0x1	idpullup idpullup Use the value of this register input to idpullup of usb2phy
8	RW	0x1	dmpulldown dmpulldown Use the value of this register input to dmpulldown of usb2phy
7	RW	0x1	dppulldown dppulldown Use the value of this register input to dppulldown of usb2phy
6	RW	0x1	termselect termselect Select the value of this register to usb2phy when utmi_sel=1
5:4	RW	0x1	xcvrselect xcvrselect Select the value of this register to usb2phy when utmi_sel=1
3:2	RW	0x0	opmode opmode Select the value of this register to usb2phy when utmi_sel=1
1	RW	0x1	suspend_n suspend_n Select the value of this register to usb2phy when utmi_sel=1

Bit	Attr	Reset Value	Description
0	RW	0x0	utmi_sel utmi_sel 1: select utmi interface signals from GRF reister to usb2phy 0: select utmi interface signals from utmi interface of usb20 host1 controller to usb2phy

GRF_USB20_PHY1_CON3
Address: Operational Base + offset (0x0e46c)
USB20 PHY1 GRF Register 3

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:5	RO	0x0	reserved
4	RW	0x0	dischrgvbus dischrgvbus Use the value of this register input to chrgvbus of usb2phy
3	RW	0x0	chrgvbus chrgvbus Use the value of this register input to chrgvbus of usb2phy
2	RW	0x0	drvvbus drvvbus Pls see drvvbus_sel.

Bit	Attr	Reset Value	Description
1	RW	0x0	drvvbus_sel drvvbus_sel 1: select the value of bit2 of USB20_PHY1_CON3 to drvvbus of usb2phy and GPIO to external PMIC 0: select drvvbus from usb3otg1 controller to drvvbus of usb2phy and GPIO to external PMIC
0	RW	0x1	idpullup idpullup Use the value of this register input to idpullup of usb2phy

GRF_USB3PHY0_CON0
Address: Operational Base + offset (0x0e580)
TypeC PHY/TCPD PHY/TCPC Control register0

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x2	vbus_src_sel vbus source select to IOMUX 0: select vbus_source_en of TCPC0 to IOMUX 1: select vbus_source_en of TCPC1 to IOMUX 2: select host0_drvvbus, host1_drvvbus, otg0_drvvbus, otg1_drvvbus to IOMUX
13	RO	0x0	reserved
12	RW	0x1	cc2_overcurrent_n cc2 overcurrent 0: cc2 overcurrent 1: cc2 not overcurrent

Bit	Attr	Reset Value	Description
11	RW	0x1	cc1_overcurrent_n cc1 overcurrent 0: cc1 overcurrent 1: cc1 not overcurrent
10	RW	0x0	vbus_valid_sel vbus valid select 0: use bvalid from usb2phy to usb3 controller 1: usb vbus_valid from TCPC to usb3 controller
9	RW	0x0	tcpc_vbus_on TCPC Vbus On 0: disable TCPC vbus supply 1: enable TCPC vbus supply
8	RW	0x1	typec_conn_dir_sel TypeC connect direction select 0: select typec_conn_dir (bit0 of this register) to TypeC PHY 1: select TCPC ouput typec_con_dir to TypeC PHY
7	RW	0x1	dead_battery_n dead_battery_n 1: no dead battery 0: dead battery
6	RW	0x1	dead_battery_sel dead_battery_sel 0: select external dead_battery_n from IOMUX 1: select internal bit7 of this register
5:4	RW	0x0	tcpc_role_strap TCPC role trap 01: TCPC default as DFP 10: TCPC default as UFP 11: TCPC default as DRP
3	RW	0x1	usb3tousb2_en force usb3 to usb2 enable control 1: force usb3 controller work as usb2. 0: not force usb3 controller work as usb2.
2:1	RW	0x0	pipe_data_bus_width Pipe interface data bus width 0: 32bit data bus width, only support 32bit data bus width.
0	RW	0x0	typec_conn_dir TypeC PHY connect direction 0: normal orientation 1: flip orientation

GRF_USB3PHY0_CON1
Address: Operational Base + offset (0x0e584)
TypeC PHY/TCPD PHY/TCPC Control register1

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	JTAG_select JTAG_select 0: select TDO of TCPC0 to IOMUX 1: select TDO of TCPC1 to IOMUX
14:13	RO	0x0	reserved
12	RW	0x1	vbus_overvoltage_n vbus overvoltage 0: vbus over voltage 1: vbus not over voltage
11	RW	0x0	JTRST JTRST TCPC extensa core JTAG JTRST reset control
10	RW	0x0	DReset DReset TCPC extensa core JTAG DReset
9	RW	0x0	BRreset BRreset TCPC extensa core JTAG BRreset
8	RW	0x0	OCDHaltOnReset OCDHaltOnReset TCPC extensa core JTAG OCDHaltOnReset
7:6	RO	0x0	reserved
5	RW	0x0	txdetectrxloopbk txdetectrxloopbk pipe_sel=1, select this bit to TypeC PHY

Bit	Attr	Reset Value	Description
4:3	RW	0x0	powerdown powerdown pipe_sel: select this two bit to TypeC PHY
2	RW	0x0	txelecidle txelecidle pipe_sel=1, select this bit to TypeC PHY
1	RW	0x0	rxtermination rx termination pipe_sel=1, select this bit to TypeC PHY
0	RW	0x0	pipe_sel pipe interface select 0: select pipe interface from usb3otg 1: select pipe interface from grf controller register

GRF_USB3PHY0_CON2
Address: Operational Base + offset (0x0e588)
TypeC PHY/TCPD PHY/TCPC Control register2

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RO	0x0	reserved
13:10	RW	0xf	vbus_overcurrent_n vbus source overcurrent 0: vbus source over current 1: vbus source not over current
9:0	RW	0x0c8	vbus_voltage TCPC vbus voltage TCPC vbus voltage

GRF_USB3PHY1_CON0
Address: Operational Base + offset (0x0e58c)

TypeC PHY/TCPD PHY/TCPC Control register0

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:13	RO	0x0	reserved
12	RW	0x1	cc2_overcurrent_n cc2 overcurrent 0: cc2 overcurrent 1: cc2 not overcurrent
11	RW	0x1	cc1_overcurrent_n cc1 overcurrent 0: cc1 overcurrent 1: cc1 not overcurrent
10	RW	0x0	vbus_valid_sel vbus valid select 0: use bvalid from usb2phy to usb3 controller 1: usb vbus_valid from TCPC to usb3 controller
9	RW	0x0	tcpc_vbus_on TCPC Vbus On 0: disable TCPC vbus supply 1: enable TCPC vbus supply
8	RW	0x1	typec_conn_dir_sel TypeC connect direction select 0: select typec_conn_dir (bit0 of this register) to TypeC PHY 1: select TCPC ouput typec_con_dir to TypeC PHY
7	RW	0x1	dead_battery_n dead_battery_n 1: no dead battery 0: dead battery

Bit	Attr	Reset Value	Description
6	RW	0x1	dead_battery_sel dead_battery_sel 0: select external dead_battery_n from IOMUX 1: select internal bit7 of this register
5:4	RW	0x0	tcpc_role_strap TCPC role trap 01: TCPC default as DFP 10: TCPC default as UFP 11: TCPC default as DRP
3	RW	0x1	usb3tousb2_en force usb3 to usb2 enable control 1: force usb3 controller work as usb2. 0: not force usb3 controller work as usb2.
2:1	RW	0x0	pipe_data_bus_width Pipe interface data bus width 0: 32bit data bus width, only support 32bit data bus width.
0	RW	0x0	typec_conn_dir TypeC PHY connect direction 0: normal orientation 1: flip orientation

GRF_USB3PHY1_CON1

Address: Operational Base + offset (0x0e590)

TypeC PHY/TCPD PHY/TCPC Control register1

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:13	RO	0x0	reserved

Bit	Attr	Reset Value	Description
12	RW	0x1	vbus_overvoltage_n vbus overvoltage 0: vbus over voltage 1: vbus not over voltage
11	RW	0x0	JTRST JTRST TCPC extensa core JTAG JTRST reset control
10	RW	0x0	DReset DReset TCPC extensa core JTAG DReset
9	RW	0x0	BRreset BRreset TCPC extensa core JTAG BRreset
8	RW	0x0	OCDHaltOnReset OCDHaltOnReset TCPC extensa core JTAG OCDHaltOnReset
7:6	RO	0x0	reserved
5	RW	0x0	txdetectrxloopbk txdetectrxloopbk pipe_sel=1, select this bit to TypeC PHY
4:3	RW	0x0	powerdown powerdown pipe_sel: select this two bit to TypeC PHY
2	RW	0x0	txelecidle txelecidle pipe_sel=1, select this bit to TypeC PHY
1	RW	0x0	rxtermination rx termination pipe_sel=1, select this bit to TypeC PHY
0	RW	0x0	pipe_sel pipe interface select 0: select pipe interface from usb3otg 1: select pipe interface from grf controller register

GRF_USB3PHY1_CON2

Address: Operational Base + offset (0x0e594)

TypeC PHY/TCPD PHY/TCPC Control register2

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RO	0x0	reserved
13:10	RW	0xf	vbus_overcurrent_n vbus source overcurrent 0: vbus source over current 1: vbus source not over current
9:0	RW	0x0c8	vbus_voltage TCPC vbus voltage TCPC vbus voltage

GRF_USB3PHY_STATUS0
Address: Operational Base + offset (0x0e5c0)
USB3PHY_STATUS0

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:25	RO	0x0	TCPC1_vbus_source_en TCPC1_vbus_source_en 1: select corresponding vbus source
24	RW	0x0	TCPC1_sink_en TCPC1_sink_en 1: TCPC1 enable to sink vbus
23	RW	0x0	TCPC1_bdis_en TCPC1_bdis_en 1: TCPC1 bleed discharge enable
22	RW	0x0	TCPC1_fdis_en TCPC1_fdis_en 1: TCPC1 force discharge enable
21	RO	0x0	TCPC1_vconn_to_cc2 TCPC1 supply VCONN to CC2 1: TCPC1 supply VCONN to CC2

Bit	Attr	Reset Value	Description
20	RO	0x0	TCPC1_vconn_to_cc1 TCPC1 vconn supply to CC1 1: support voconn to CC1
19	RO	0x0	TCPC1_vbus_overcurrent TCPC1 vbus overcurrent ouput 1: vbus over current
18	RO	0x0	TCPC1_JTAG_XOCDMode TCPC1 JTAG XOCDMode
17	RO	0x0	typec_pd_phy1_ready TypeC PD PHY 1 ready 1: TypeC PD PHY ready
16	RO	0x0	typec_phy1_pipe_status TypeC PHY 0 pipe status 0: indicate TypeC PHY pipe ready after release TypeC PHY pipe reset.
15:13	RO	0x0	reserved
12:9	RO	0x0	TCPC0_vbus_source_en TCPC0_vbus_source_en 1: select corresponding vbus source
8	RO	0x0	TCPC0_sink_en TCPC0_sink_en 1: TCPC0 enable to sink vbus
7	RO	0x0	TCPC0_bdis_en TCPC0_bdis_en 1: TCPC0 bleed discharge enable
6	RO	0x0	TCPC0_fdis_en TCPC0_fdis_en 1: TCPC0 force discharge enable
5	RO	0x0	TCPC0_vconn_to_cc2 TCPC0 supply VCONN to CC2 1: TCPC0 supply VCONN to CC2
4	RO	0x0	TCPC0_vconn_to_cc1 TCPC0 vconn supply to CC1 1: support voconn to CC1
3	RO	0x0	TCPC0_vbus_overcurrent TCPC0 vbus overcurrent ouput 1: vbus over current
2	RO	0x0	TCPC0_JTAG_XOCDMode TCPC0 JTAG XOCDMode
1	RO	0x0	typec_pd_phy0_ready TypeC PD PHY 0 ready 1: TypeC PD PHY ready

Bit	Attr	Reset Value	Description
0	RO	0x0	typec_phy0_pipe_status TypeC PHY 0 pipe status 0: indicate TypeC PHY pipe ready after release TypeC PHY pipe reset.

GRF_USB3PHY_STATUS1
Address: Operational Base + offset (0x0e5c4)
USB3PHY_STATUS1

Bit	Attr	Reset Value	Description
31	RO	0x0	cc_dead_battery_n CC dead battery indicator from IOMUX 0: dead battery happen 1: No dead battery happen
30:28	RO	0x0	reserved
27	RW	0x0	TCPC1_vbus_overcurrent_en TCPC vbus over current enable 1: enable
26	RO	0x0	TCPC1_vconn_overcurrent_en TCPC vconn overcurrent enable 1: enable
25	RO	0x0	TCPC1_vbus_voltage_en TCPC vbus voltage enable 1: enable
24	RO	0x0	TCPC1_vbus_overvoltage_en TCPC vbus overvoltage enable 1: enable
23	RO	0x0	TCPC1_outs_to_hiz TCPC outs to hiz
22	RO	0x0	TCPC1_dbg_acc_conn_n TCPC debug accessory connect 0: Debug accessory connected 1: No debug accessory connected
21	RO	0x0	TCPC1_audio_acc_conn_n TCPC audio accessory connect 0: audio accessory connected 1: No audio accessory connected
20	RO	0x0	TCPC1_act_cable_conn_n TCPC active cable connect 0: No connected 1: Active cable connected

Bit	Attr	Reset Value	Description
19:18	RO	0x0	TCPC1_mux_ctrl TCPC MUX CTRL 0: No connect 1: USB3.1 connect 2: DP 4 lanes 3: USB3.1 and DP 2 lanes
17	RO	0x0	TCPC1_conn_present TCPC connect present 0: No connect 1: Connected
16	RO	0x0	TCPC1_conn_orientation TCPC connect orientation 0: normal 1: flip
15:12	RO	0x0	reserved
11	RW	0x0	TCPC0_vbus_overcurrent_en TCPC vbus over current enable 1: enable
10	RO	0x0	TCPC0_vconn_overcurrent_en TCPC vconn overcurrent enable 1: enable
9	RO	0x0	TCPC0_vbus_voltage_en TCPC vbus voltage enable 1: enable
8	RO	0x0	TCPC0_vbus_overvoltage_en TCPC vbus overvoltage enable 1: enable
7	RO	0x0	TCPC0_outs_to_hiz TCPC outs to hiz
6	RO	0x0	TCPC0_dbg_acc_conn_n TCPC debug accessory connect 0: Debug accessory connected 1: No debug accessory connected
5	RO	0x0	TCPC0_audio_acc_conn_n TCPC audio accessory connect 0: audio accessory connected 1: No audio accessory connected
4	RO	0x0	TCPC0_act_cable_conn_n TCPC active cable connect 0: No connected 1: Active cable connected

Bit	Attr	Reset Value	Description
3:2	RO	0x0	TCPC0_mux_ctrl TCPC MUX CTRL 0: No connect 1: USB3.1 connect 2: DP 4 lanes 3: USB3.1 and DP 2 lanes
1	RO	0x0	TCPC0_conn_present TCPC connect present 0: No connect 1: Connected
0	RO	0x0	TCPC0_conn_orientation TCPC connect orientation 0: normal 1: flip

GRF_DLL_CON0
Address: Operational Base + offset (0x0e600)
pvtm control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x0	pvtm_gpu_osc_ring_sel gpu PVT monitor oscilator ring select
13	RW	0x0	pvtm_gpu_osc_en gpu PVT monitor oscilator enable 1'b1: enable 1'b0: disable
12	RW	0x0	pvtm_gpu_start gpu PVT monitor start control
11:10	RW	0x0	pvtm_ddr_osc_ring_sel ddr PVT monitor oscilator ring select

Bit	Attr	Reset Value	Description
9	RW	0x0	pvtm_ddr_osc_en ddr PVT monitor oscilator enable 1'b1: enable 1'b0: disable
8	RW	0x0	pvtm_ddr_start ddr PVT monitor start control
7:6	RW	0x0	pvtm_core_b_osc_sel pd_core_l PVT monitor oscilator select pvtm_core_b_osc_sel[1:0]
5	RW	0x0	pvtm_core_b_osc_en pd_core_b PVT monitor oscilator enable 1'b1: enable 1'b0: disable
4	RW	0x0	pvtm_core_b_start pd_core_b PVT monitor start control
3:2	RW	0x0	pvtm_core_l_osc_sel pd_core_l PVT monitor oscilator select
1	RW	0x0	pvtm_core_l_osc_en pd_core_l PVT monitor oscilator enable 1'b1: enable 1'b0: disable
0	RW	0x0	pvtm_core_l_start pd_core_l PVT monitor start control

GRF_DLL_CON1
Address: Operational Base + offset (0x0e604)
pvtm control register

Bit	Attr	Reset Value	Description
31:0	RW	0x016e3600	pvtm_core_l_cal_cnt pd_core_l pvtm calculator counter

GRF_DLL_CON2
Address: Operational Base + offset (0x0e608)
pvtm control register

Bit	Attr	Reset Value	Description
31:0	RW	0x016e3600	pvtm_core_b_cal_cnt pd_core_b pvtm calculator counter

GRF_DLL_CON3
Address: Operational Base + offset (0x0e60c)
pvtm control register

Bit	Attr	Reset Value	Description
31:0	RW	0x016e3600	pvtm_ddr_cal_cnt ddr pvtm calculator counter

GRF_DLL_CON4
Address: Operational Base + offset (0x0e610)
pvtm control register

Bit	Attr	Reset Value	Description
31:0	RW	0x016e3600	pvtm_gpu_cal_cnt gpu pvtm calculator counter

GRF_DLL_CON5
Address: Operational Base + offset (0x0e614)
pvtm control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:1	RO	0x0	reserved
0	RW	0x0	pvtm_core_b_osc_sel pvtm_core_b_osc_sel[2]

GRF_DLL_STATUS0
Address: Operational Base + offset (0x0e620)
pvtm status register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:4	RO	0x0	reserved
3	RW	0x0	pvtm_ddr_freq_done ddr pvtm frequency calculate done stutus
2	RW	0x0	pvtm_gpu_freq_done gpu pvtm frequency calculate done stutus
1	RW	0x0	pvtm_core_b_freq_done pd_core_b pvtm frequency calculate done stutus
0	RW	0x0	pvtm_core_l_freq_done pd_core_l pvtm frequency calculate done stutus

GRF_DLL_STATUS1
Address: Operational Base + offset (0x0e624)
pvtm status register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pvtm_core_l_freq_cnt pd_core_l pvtm frequency count

GRF_DLL_STATUS2
Address: Operational Base + offset (0x0e628)
pvtm status register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pvtm_core_b_freq_cnt pd_core_b pvtm frequency count

GRF_DLL_STATUS3
Address: Operational Base + offset (0x0e62c)
pvtm status register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pvtm_gpu_freq_cnt gpu pvtm frequency count

GRF_DLL_STATUS4
Address: Operational Base + offset (0x0e630)
pvtm status register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pvtm_ddr_freq_cnt ddr pvtm frequency count

GRF_IO_VSEL
Address: Operational Base + offset (0x0e640)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:4	RO	0x0	reserved
3	RW	0x0	gpio1833_gpio4cd_ms
2	RW	0x0	sdmmc_gpio4b_ms
1	RW	0x0	audio_gpio3d4a_ms
0	RW	0x0	bt656_gpio2ab_ms

GRF_SARADC_TESTBIT
Address: Operational Base + offset (0x0e644)
saradc test bit control register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:1	RO	0x0	reserved
0	RW	0x0	saradc_testbit saradc test bit control

GRF_TSADC_TESTBIT_L
Address: Operational Base + offset (0x0e648)
saradc test bit control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:4	RO	0x0	reserved
3	RW	0x0	grf_tsadc_dig_bypass
2	RW	0x0	grf_tsadc_clk_sel
1	RW	0x0	grf_tsadc_tsen_pd_1

Bit	Attr	Reset Value	Description
0	RW	0x0	grf_tsadc_tsen_pd_0

GRF_TSADC_TESTBIT_H
Address: Operational Base + offset (0x0e64c)
tsadc test bit control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:1	RO	0x0	reserved
0	RW	0x0	tsadc_testbit_h tsadc test bit control

GRF_CHIP_ID_ADDR
Address: Operational Base + offset (0x0e800)
chip id register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	chip_id 3399

GRF_FAST_BOOT_ADDR
Address: Operational Base + offset (0x0e880)
faster boot address register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	fast_boot_addr fast boot address

GRF_EMMCCORE_CON0
Address: Operational Base + offset (0x0f000)
emmc core control register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0000	emmccore_con0 emmc controller control register 0

GRF_EMMCCORE_CON1
Address: Operational Base + offset (0x0f004)
emmc core control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0000	emmccore_con1 emmc controller control register 1

GRF_EMMCCORE_CON2
Address: Operational Base + offset (0x0f008)
emmc core control register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0000	emmccore_con2 emmc controller control register 2

GRF_EMMCCORE_CON3
Address: Operational Base + offset (0x0f00c)
emmc core control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0000	emmccore_con3 emmc controller control register 3

GRF_EMMCCORE_CON4
Address: Operational Base + offset (0x0f010)
emmc core control register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0000	emmccore_con4 emmc controller control register 4

GRF_EMMCCORE_CON5
Address: Operational Base + offset (0x0f014)
emmc core control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0000	emmccore_con5 emmc controller control register 5

GRF_EMMCCORE_CON6
Address: Operational Base + offset (0x0f018)
emmc core control register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0000	emmccore_con6 emmc controller control register 6

GRF_EMMCCORE_CON7
Address: Operational Base + offset (0x0f01c)
emmc core control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0000	emmccore_con7 emmc controller control register 7

GRF_EMMCCORE_CON8
Address: Operational Base + offset (0x0f020)
emmc core control register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0000	emmccore_con8 emmc controller control register 8

GRF_EMMCCORE_CON9
Address: Operational Base + offset (0x0f024)
emmc core control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0000	emmccore_con9 emmc controller control register 9

GRF_EMMCCORE_CON10
Address: Operational Base + offset (0x0f028)
emmc core control register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0000	emmccore_con10 emmc controller control register 10

GRF_EMMCCORE_CON11
Address: Operational Base + offset (0x0f02c)
emmc core control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0000	emmccore_con11 emmc controller control register 11

GRF_EMMCCORE_STATUS0
Address: Operational Base + offset (0x0f040)
emmc core status register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	emmccore_status0 emmc controller status register 0

GRF_EMMCCORE_STATUS1
Address: Operational Base + offset (0x0f044)
emmc core status register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	emmccore_status1 emmc controller status register 1

GRF_EMMCCORE_STATUS2
Address: Operational Base + offset (0x0f048)
emmc core status register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	emmccore_status2 emmc controller status register 2

GRF_EMMCCORE_STATUS3
Address: Operational Base + offset (0x0f04c)
emmc core status register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	emmccore_status3 emmc controller status register 3

GRF_EMMCPHY_CON0
Address: Operational Base + offset (0x0f780)
emmc phy control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0000	emmcphy_con0 emmc phy control register 0

GRF_EMMCPHY_CON1
Address: Operational Base + offset (0x0f784)
emmc phy control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0000	emmcphy_con1 emmc phy control register 1

GRF_EMMCPHY_CON2
Address: Operational Base + offset (0x0f788)
emmc phy control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0000	emmcphy_con2 emmc phy control register 2

GRF_EMMCPHY_CON3

Address: Operational Base + offset (0x0f78c)
emmc phy control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0000	emmcphy_con3 emmc phy control register 3

GRF_EMMCPHY_CON4
Address: Operational Base + offset (0x0f790)
emmc phy control register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0000	emmcphy_con4 emmc phy control register 4

GRF_EMMCPHY_CON5
Address: Operational Base + offset (0x0f794)
emmc phy control register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0000	emmcphy_con5 emmc phy control register 5

GRF_EMMCPHY_CON6
Address: Operational Base + offset (0x0f798)
emmc phy control register

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	emmcphy_con6 emmc phy control register 5

GRF_EMMCPHY_STATUS
Address: Operational Base + offset (0x0f7a0)
emmc phy status register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	emmcphy_status emmc phy status register

4.4 PMU GRF Register description

4.4.1 Register Summary

Name	Offset	Size	Reset Value	Description
PMUGRF_GPIO0A_IOMUX	0x00000	W	0x00000000	GPIO0A iomux control
PMUGRF_GPIO0B_IOMUX	0x00004	W	0x00000014	GPIO0B iomux control
PMUGRF_GPIO1A_IOMUX	0x00010	W	0x00000000	GPIO1A iomux control
PMUGRF_GPIO1B_IOMUX	0x00014	W	0x00000000	GPIO1B iomux control
PMUGRF_GPIO1C_IOMUX	0x00018	W	0x00000000	GPIO1C iomux control
PMUGRF_GPIO1D_IOMUX	0x0001c	W	0x00000000	GPIO1D iomux control
PMUGRF_GPIO0A_P	0x00040	W	0x0000dd5f	GPIO0A PU/PD control

Name	Offset	Size	Reset Value	Description
PMUGRF_GPIO0B_P	0x00044	W	0x00000557	GPIO0B PU/PD control
PMUGRF_GPIO1A_P	0x00050	W	0x00006aaa	GPIO1A PU/PD control
PMUGRF_GPIO1B_P	0x00054	W	0x00006955	GPIO1B PU/PD control
PMUGRF_GPIO1C_P	0x00058	W	0x0000a599	GPIO1C PU/PD control
PMUGRF_GPIO1D_P	0x0005c	W	0x00000002	GPIO0D PU/PD control
PMUGRF_GPIO0A_E	0x00080	W	0x00000000	GPIO0A drive strength control
PMUGRF_GPIO0B_E	0x00088	W	0x00000000	GPIO0D drive strength control
PMUGRF_GPIO1A_E	0x000a0	W	0x00004000	GPIO1A drive strength control
PMUGRF_GPIO1B_E	0x000a8	W	0x00000015	GPIO1D drive strength control
PMUGRF_GPIO1C_E	0x000b0	W	0x00005000	GPIO1C drive strength control
PMUGRF_GPIO1D_E	0x000b8	W	0x00000001	GPIO1D drive strength control
PMUGRF_GPIO0L_SR	0x00100	W	0x00000000	GPIO0 A/B SR control
PMUGRF_GPIO1L_SR	0x00108	W	0x00000000	GPIO1 A/B SR control
PMUGRF_GPIO1H_SR	0x0010c	W	0x0000000f	GPIO1C/D SR control
PMUGRF_GPIO0A_SMT	0x00120	W	0x00000000	GPIO0A smit control
PMUGRF_GPIO0B_SMT	0x00124	W	0x00000000	GPIO0B smit control
PMUGRF_GPIO1A_SMT	0x00130	W	0x00000000	GPIO1A smit control
PMUGRF_GPIO1B_SMT	0x00134	W	0x00000000	GPIO1B smit control
PMUGRF_GPIO1C_SMT	0x00138	W	0x00000000	GPIO1C smit control
PMUGRF_GPIO1D_SMT	0x0013c	W	0x00000000	GPIO1D smit control
PMUGRF_GPIO0L_HE	0x00160	W	0x00000000	GPIO0 A/B HE control
PMUGRF_GPIO1L_HE	0x00168	W	0x00000000	GPIO1 A/B HE control
PMUGRF_GPIO1H_HE	0x0016c	W	0x0000000f	GPIO1C/D HE control
PMUGRF_SOC_CON0	0x00180	W	0x00000320	SoC control register 0
PMUGRF_SOC_CON10	0x001a8	W	0x000061a8	SoC control register 10
PMUGRF_SOC_CON11	0x001ac	W	0x00000000	SoC control register 11
PMUGRF_PMUPVTM_CON0	0x00240	W	0x00000000	pmu pvtm configuration register0
PMUGRF_PMUPVTM_CON1	0x00244	W	0x00000000	pmu pvtm configuration register1
PMUGRF_PMUPVTM_STATUS0	0x00248	W	0x00000000	pmu pvtm status register
PMUGRF_PMUPVTM_STATUS1	0x0024c	W	0x00000000	pmu pvtm status register
PMUGRF_OSC_E	0x00250	W	0x00000006	OSC control register
PMUGRF_OS_REG0	0x00300	W	0x00000000	os register
PMUGRF_OS_REG1	0x00304	W	0x00000000	os register
PMUGRF_OS_REG2	0x00308	W	0x00000000	os register
PMUGRF_OS_REG3	0x0030c	W	0x00000000	os register

*Notes: Size : **B** - Byte (8 bits) access, **HW** - Half WORD (16 bits) access, **W** -WORD (32 bits) access*

4.4.2 Detail Register Description

PMUGRF_GPIO0A_IOMUX
Address: Operational Base + offset (0x00000)
GPIO0A iomux control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x0	gpio0a7_sel GPIO0A[7] iomux select 2'b00: gpio 2'b01: sdmmc_dectn 2'b10: pmu_debug5 2'b11: reserved
13:12	RW	0x0	gpio0a6_sel GPIO0A[6] iomux select 2'b00: gpio 2'b01: pwm_3a 2'b10: pmu_debug4 2'b11: reserved
11:10	RW	0x0	gpio0a5_sel GPIO0A[5] iomux select 2'b00: gpio 2'b01: emmc_pwren 2'b10: pmu_debug3 2'b11: reserved
9:8	RW	0x0	gpio0a4_sel GPIO0A[4] iomux select 2'b00: gpio 2'b01: sdio_intn 2'b10: pmu_debug2 2'b11: reserved

Bit	Attr	Reset Value	Description
7:6	RW	0x0	gpio0a3_sel GPIO0A[3] iomux select 2'b00: gpio 2'b01: sdio_wrprt 2'b10: pmu_debug1 2'b11: reserved
5:4	RW	0x0	gpio0a2_sel GPIO0A[2] iomux select 2'b00: gpio 2'b01: wifi_26m 2'b10: pmu_debug0 2'b11: reserved
3:2	RW	0x0	gpio0a1_sel GPIO0A[1] iomux select 2'b00: gpio 2'b01: ddrio_pwroff 2'b10: tcpd_ccdben 2'b11: reserved
1:0	RW	0x0	gpio0a0_sel GPIO0A[0] iomux select 2'b00: gpio 2'b01: test_clkout0 2'b10: clk_32k 2'b11: reserved

PMUGRF_GPIO0B_IOMUX
Address: Operational Base + offset (0x00004)
GPIO0B iomux control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:12	RO	0x0	reserved

Bit	Attr	Reset Value	Description
11:10	RW	0x0	gpio0b5_sel GPIO0B[5] iomux select 2'b00: gpio 2'b01: tcpd_vbusfdis 2'b10: tcpdusb2_vbussource3 2'b11: reserved
9:8	RW	0x0	gpio0b4_sel GPIO0B4] iomux select 2'b00: gpio 2'b01: tcpd_vbusbdis 2'b10: reserved 2'b11: reserved
7:6	RW	0x0	gpio0b3_sel GPIO0B[3] iomux select 2'b00: gpio 2'b01: reserved 2'b10: reserved 2'b11: reserved
5:4	RW	0x1	gpio0b2_sel GPIO0B[2] iomux select 2'b00: gpio 2'b01: reserved 2'b10: reserved 2'b11: reserved
3:2	RW	0x1	gpio0b1_sel GPIO0B[1] iomux select 2'b00: gpio 2'b01: pmu1830_volsel 2'b10: reserved 2'b11: reserved
1:0	RW	0x0	gpio0b0_sel GPIO0B[0] iomux select 2'b00: gpio 2'b01: sdmmc_wrprt 2'b10: pmum0_wfi 2'b11: test_clkout2

PMUGRF_GPIO1A_IOMUX
Address: Operational Base + offset (0x00010)
GPIO1A iomux control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x0	gpio1a7_sel GPIO1A[7] iomux select 2'b00: gpio 2'b01: uart4m0_sin 2'b10: spi1ec_rxd 2'b11: reserved
13:12	RW	0x0	gpio1a6_sel GPIO1A[6] iomux select 2'b00: gpio 2'b01: tsadc_int 2'b10: reserved 2'b11: reserved
11:10	RW	0x0	gpio1a5_sel GPIO1A[5] iomux select 2'b00: gpio 2'b01: ap_pwroff 2'b10: reserved 2'b11: reserved
9:8	RW	0x0	gpio1a4_sel GPIO1A[4] iomux select 2'b00: gpio 2'b01: isp0_prelighttrig 2'b10: isp1_prelighttrig 2'b11: reserved
7:6	RW	0x0	gpio1a3_sel GPIO1A[3] iomux select 2'b00: gpio 2'b01: isp0_flashtrigout 2'b10: isp1_flashtrigout 2'b11: reserved

Bit	Attr	Reset Value	Description
5:4	RW	0x0	gpio1a2_sel GPIO1A[2] iomux select 2'b00: gpio 2'b01: isp0_flashtrigin 2'b10: isp1_flashtrigin 2'b11: tcpd_cc1vconn
3:2	RW	0x0	gpio1a1_sel GPIO1A[1] iomux select 2'b00: gpio 2'b01: isp0_shuttertrig 2'b10: isp1_shuttertrig 2'b11: tcpd_cc0vconn
1:0	RW	0x0	gpio1a0_sel GPIO1A[0] iomux select 2'b00: gpio 2'b01: isp0_shutteren 2'b10: isp1_shutteren 2'b11: tcpd_vbussink

PMUGRF_GPIO1B_IOMUX
Address: Operational Base + offset (0x00014)
GPIO1B iomux control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x0	gpio1b7_sel GPIO1B[7] iomux select 2'b00: gpio 2'b01: spi3pmu_rxd 2'b10: i2c0pmu_scl 2'b11: reserved

Bit	Attr	Reset Value	Description
13:12	RW	0x0	gpio1b6_sel GPIO1B[6] iomux select 2'b00: gpio 2'b01: pwm_3b 2'b10: reserved 2'b11: reserved
11:10	RW	0x0	gpio1b5_sel GPIO1B[5] iomux select 2'b00: gpio 2'b01: reserved 2'b10: reserved 2'b11: reserved
9:8	RW	0x0	gpio1b4_sel GPIO1B[4] iomux select 2'b00: gpio 2'b01: i2c4sensor_scl 2'b10: reserved 2'b11: reserved
7:6	RW	0x0	gpio1b3_sel GPIO1B[3] iomux select 2'b00: gpio 2'b01: i2c4sensor_sda 2'b10: reserved 2'b11: reserved
5:4	RW	0x0	gpio1b2_sel GPIO1B[2] iomux select 2'b00: gpio 2'b01: pmum0jtag_tms 2'b10: spi1ec_csn0 2'b11: reserved
3:2	RW	0x0	gpio1b1_sel GPIO1B[1] iomux select 2'b00: gpio 2'b01: pmum0jtag_tck 2'b10: spi1ec_clk 2'b11: reserved
1:0	RW	0x0	gpio1b0_sel GPIO1B[0] iomux select 2'b00: gpio 2'b01: uart4m0_sout 2'b10: spi1ec_txd 2'b11: reserved

PMUGRF_GPIO1C_IOMUX
Address: Operational Base + offset (0x00018)

GPIO1C iomux control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x0	gpio1c7_sel GPIO1C[7] iomux select 2'b00: gpio 2'b01: tcpdusb2_vbussource1 2'b10: reserved 2'b11: reserved
13:12	RW	0x0	gpio1c6_sel GPIO1C[6] iomux select 2'b00: gpio 2'b01: tcpdusb2_vbussource0 2'b10: reserved 2'b11: reserved
11:10	RW	0x0	gpio1c5_sel GPIO1C[5] iomux select 2'b00: gpio 2'b01: i2c8dcdc_scl 2'b10: reserved 2'b11: reserved
9:8	RW	0x0	gpio1c4_sel GPIO1C[4] iomux select 2'b00: gpio 2'b01: i2c8dcdc_sda 2'b10: reserved 2'b11: reserved
7:6	RW	0x0	gpio1c3_sel GPIO1C[3] iomux select 2'b00: gpio 2'b01: pwm_2 2'b10: reserved 2'b11: reserved

Bit	Attr	Reset Value	Description
5:4	RW	0x0	gpio1c2_sel GPIO1C[2] iomux select 2'b00: gpio 2'b01: spi3pmu_csn0 2'b10: reserved 2'b11: reserved
3:2	RW	0x0	gpio1c1_sel GPIO1C[1] iomux select 2'b00: gpio 2'b01: spi3pmu_clk 2'b10: reserved 2'b11: reserved
1:0	RW	0x0	gpio1c0_sel GPIO1C[0] iomux select 2'b00: gpio 2'b01: spi3pmu_txd 2'b10: i2c0pmu_scl 2'b11: reserved

PMUGRF_GPIO1D_IOMUX
Address: Operational Base + offset (0x0001c)
GPIO1D iomux control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:2	RO	0x0	reserved
1:0	RW	0x0	gpio1d0_sel GPIO1D[0] iomux select 2'b00: gpio 2'b01: tcpdusb2_vbussource2 2'b10: reserved 2'b11: reserved

PMUGRF_GPIO0A_P
Address: Operational Base + offset (0x00040)
GPIO0A PU/PD control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0xdd5f	gpio0a_p GPIO0A PE/PS programmation section, every GPIO bit corresponding to 2bits[PS:PE] 2'b00: Z(Noraml operaton); 2'b11: weak 1(pull-up); 2'b01: weak 0(pull-down); 2'b10: Z(Noraml operaton);

PMUGRF_GPIO0B_P
Address: Operational Base + offset (0x00044)
GPIO0B PU/PD control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

Bit	Attr	Reset Value	Description
15:0	RW	0x0557	gpio0b_p GPIO0A PE/PS programmation section, every GPIO bit corresponding to 2bits[PS:PE] 2'b00: Z(Noraml operaton); 2'b11: weak 1(pull-up); 2'b01: weak 0(pull-down); 2'b10: Z(Noraml operaton);

PMUGRF_GPIO1A_P
Address: Operational Base + offset (0x00050)
GPIO1A PU/PD control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x6aaa	gpio1a_p GPIO1A PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

PMUGRF_GPIO1B_P
Address: Operational Base + offset (0x00054)
GPIO1B PU/PD control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x6955	gpio1b_p GPIO1B PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

PMUGRF_GPIO1C_P
Address: Operational Base + offset (0x00058)
GPIO1C PU/PD control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

Bit	Attr	Reset Value	Description
15:0	RW	0xa599	gpio1c_p GPIO1C PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

PMUGRF_GPIO1D_P
Address: Operational Base + offset (0x0005c)
GPIO0D PU/PD control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0002	gpio1d_p GPIO1D PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

PMUGRF_GPIO0A_E
Address: Operational Base + offset (0x00080)
GPIO0A drive strength control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0000	gpio0a_e GPIO0A drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

PMUGRF_GPIO0B_E
Address: Operational Base + offset (0x00088)
GPIO0D drive strength control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	gpio0b_e GPIO0B drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

PMUGRF_GPIO1A_E
Address: Operational Base + offset (0x000a0)
GPIO1A drive strength control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x4000	gpio1a_e GPIO1A drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

PMUGRF_GPIO1B_E
Address: Operational Base + offset (0x000a8)
GPIO1D drive strength control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0015	gpio1b_e GPIO1B drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

PMUGRF_GPIO1C_E
Address: Operational Base + offset (0x000b0)
GPIO1C drive strength control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

Bit	Attr	Reset Value	Description
15:0	RW	0x5000	gpio1c_e GPIO1C drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

PMUGRF_GPIO1D_E
Address: Operational Base + offset (0x000b8)
GPIO1D drive strength control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0001	gpio1d_e GPIO1D drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

PMUGRF_GPIO0L_SR
Address: Operational Base + offset (0x00100)
GPIO0 A/B SR control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RW	0x00	gpio0b_sr GPIO0B slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast
7:0	RW	0x00	gpio0a_sr GPIO0A slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast

PMUGRF_GPIO1L_SR
Address: Operational Base + offset (0x00108)
GPIO1 A/B SR control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

Bit	Attr	Reset Value	Description
15:8	RW	0x00	gpio1b_sr GPIO1B slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast
7:0	RW	0x00	gpio1a_sr GPIO1A slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast

PMUGRF_GPIO1H_SR
Address: Operational Base + offset (0x0010c)
GPIO1C/D SR control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RW	0x00	gpio0d_sr GPIO0D slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast
7:0	RW	0x0f	gpio1c_sr GPIO1C slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast

PMUGRF_GPIO0A_SMT
Address: Operational Base + offset (0x00120)
GPIO0A smit control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0000	gpio0a_smt GPIO0A drive strength control, every GPIO bit corresponding to 2bits 2'b00: smit disable 2'b01: smit enable 2'b10: reserved 2'b11: reserved

PMUGRF_GPIO0B_SMT
Address: Operational Base + offset (0x00124)
GPIO0B smit control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	gpio0b_smt GPIO0B drive strength control, every GPIO bit corresponding to 2bits 2'b00: smit disable 2'b01: smit enable 2'b10: reserved 2'b11: reserved

PMUGRF_GPIO1A_SMT
Address: Operational Base + offset (0x00130)
GPIO1A smit control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0000	gpio1a_smt GPIO1A drive strength control, every GPIO bit corresponding to 2bits 2'b00: smit disable 2'b01: smit enable 2'b10: reserved 2'b11: reserved

PMUGRF_GPIO1B_SMT
Address: Operational Base + offset (0x00134)
GPIO1B smit control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0000	gpio1b_smt GPIO1B drive strength control, every GPIO bit corresponding to 2bits 2'b00: smit disable 2'b01: smit enable 2'b10: reserved 2'b11: reserved

PMUGRF_GPIO1C_SMT
Address: Operational Base + offset (0x00138)
GPIO1C smit control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	gpio1c_smt GPIO1C drive strength control, every GPIO bit corresponding to 2bits 2'b00: smit disable 2'b01: smit enable 2'b10: reserved 2'b11: reserved

PMUGRF_GPIO1D_SMT
Address: Operational Base + offset (0x0013c)
GPIO1D smit control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x0000	gpio1d_smt GPIO1D drive strength control, every GPIO bit corresponding to 2bits 2'b00: smit disable 2'b01: smit enable 2'b10: reserved 2'b11: reserved

PMUGRF_GPIO0L_HE
Address: Operational Base + offset (0x00160)
GPIO0 A/B HE control

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RW	0x00	gpio0b_sr GPIO0B slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast
7:0	RW	0x00	gpio0a_sr GPIO0A slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast

PMUGRF_GPIO1L_HE
Address: Operational Base + offset (0x00168)
GPIO1 A/B HE control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;

Bit	Attr	Reset Value	Description
15:8	RW	0x00	gpio0b_sr GPIO0B slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast
7:0	RW	0x00	gpio0a_sr GPIO0A slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast

PMUGRF_GPIO1H_HE
Address: Operational Base + offset (0x0016c)
GPIO1C/D HE control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RW	0x00	gpio0d_sr GPIO0D slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast
7:0	RW	0x0f	gpio1c_sr GPIO1C slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast

PMUGRF_SOC_CON0
Address: Operational Base + offset (0x00180)
SoC control register 0

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:10	RO	0x0	reserved
9	RW	0x1	pmu1830_vol pmu IO 1.8v/3.0v select. 0: 3.0v ; 1: 1.8v ;
8	RW	0x1	pmu1830_volsel pmu GPIO1 1.8v/3.0v control source select. 0: controlled by IO_GPIO0B1 ; 1: controlled by PMUGRF.SOC_CON0.pmu1830_vol
7	RO	0x0	reserved
6	RW	0x0	pclk_alive_niu_en pd_alive pclk_niu gating. 1: gating ; 0: not gating .
5	RW	0x1	pwm3_sel Use 2 optional IOs for pwm3. 0: pwm3a 1: pwm3b
4	RW	0x0	cru_pmu_pclk_gate 1: gate clock ; 0: not gate .
3	RW	0x0	pmu_noc_obsrv
2	RW	0x0	pmu_mcu_niu_obsrv

Bit	Attr	Reset Value	Description
1	RW	0x0	pmu_noc_stall When pmu noc meet illegal access, the noc will 0: error reponse 1: stall
0	RW	0x0	chip_32k_src chip 32K clock source select 0: from external 1: from internal, pvtm

PMUGRF_SOC_CON10
Address: Operational Base + offset (0x001a8)
SoC control register 10

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x61a8	sdmmc_dettime0 sdmmc_dettime[15:0]

PMUGRF_SOC_CON11
Address: Operational Base + offset (0x001ac)
SoC control register 11

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:4	RO	0x0	reserved
3:0	RW	0x0	sdmmc_dettime1 sdmmc_dettime[19:16]

PMUGRF_PMUPVTM_CON0
Address: Operational Base + offset (0x00240)
pmu pvtm configuration register0

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:2	RW	0x0000	pvtm_clkout_div clk_pvtm_out_div=clk_pvtm_out/pvtm_clkout_div
1	RW	0x0	pvtm_osc_en pmu pvtm osc enable
0	RW	0x0	pvtm_start pmu pvtm start

PMUGRF_PMUPVTM_CON1
Address: Operational Base + offset (0x00244)
pmu pvtm configuration register1

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pvtm_core_cal_cnt pd_core pvtm calculator counter

PMUGRF_PMUPVTM_STATUS0
Address: Operational Base + offset (0x00248)
pmu pvtm status register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	pvtm_freq_done pvtm frequency calculate done status

PMUGRF_PMUPVTM_STATUS1
Address: Operational Base + offset (0x0024c)
pmu pvtm status register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pvtm_freq_cnt pvtm frequency count

PMUGRF_OSC_E
Address: Operational Base + offset (0x00250)
OSC control register

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:16	RW	0x0	write_enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; When bit 18=1, bit 2 can be written by software . When bit 18=0, bit 2 cannot be written by software;
15:3	RO	0x0	reserved
2:0	RW	0x6	osc_e 24M OSC drive strenth

PMUGRF_OS_REG0
Address: Operational Base + offset (0x00300)

os register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg0 os register

PMUGRF_OS_REG1

Address: Operational Base + offset (0x00304)

os register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg1 os register

PMUGRF_OS_REG2

Address: Operational Base + offset (0x00308)

os register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg2 os register

PMUGRF_OS_REG3

Address: Operational Base + offset (0x0030c)

os register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	os_reg3 os register

Chapter 5 Cortex-A72

5.1 Overview

The RK3399 has a dual-core Cortex-A72 cluster with 1M L2 memory. Cortex-A72 processor, which is a high_performance, low-power processor that implements the ARMv8-A architecture.

The Cortex-A72 processor includes following features:

- Full implementation of the ARMv8-A architecture instruction set
- Support for both AArch32 and AArch64 Execution status.
- Support for all exception levels, EL0, EL1, EL2, and EL3, in each execution states.
- Support A32 instruction set, previously called the ARM instruction set.
- Support T32 instruction set, previously called the Thumb instruction set.
- Support A64 instruction set.
- Superscalar, variable-length, out-of-order pipeline.
- Dynamic branch prediction with Branch Target Buffer (BTB) and Global History Buffer (GHB) RAMs, a return stack, and an indirect predictor.
- 48-entry fully-associative L1 instruction Translation Lookaside Buffer (TLB) with native support for 4KB, 64KB, and 1MB page sizes.
- 32-entry fully-associative L1 data TLB with native support for 4KB, 64KB, and 1MB page sizes.
- Level 2 (L2) memory system providing cluster memory coherency, with L2 cache.
- Support advanced SIMD and Floating-point Extension for integer and floating-point vector operations.
- Support ARMv8 Cryptography Extensions.
- Support AMBA 4 ACE bus architecture.

The configuration details of little cluster and big cluster are shown in following tables

Table 5-1 CPU Configuration

Number of CPU	2
L1 I cache size	48K
L1 D cache size	32K
L2 cache size	1M
L2 data RAM output latency	3 cycles
L2 data RAM input latency	2 cycles
CPU cache protection	No
SCU L2 cache protection	No
BUS master interface	ACE
NEON and floating point support	Yes
Cryptography extension	Yes

5.2 Block Diagram

The Cortex-A72 sub system is shown in Figure 8-1. As illustrated, dual-core Cortex-A72 connects to system bus through asynchronous bridges which can handle with CDC (clock domain crossing) issue.

The Cortex-A72 is connected with system counter, which can run under a constant frequency clock, for PPI interrupt generation.

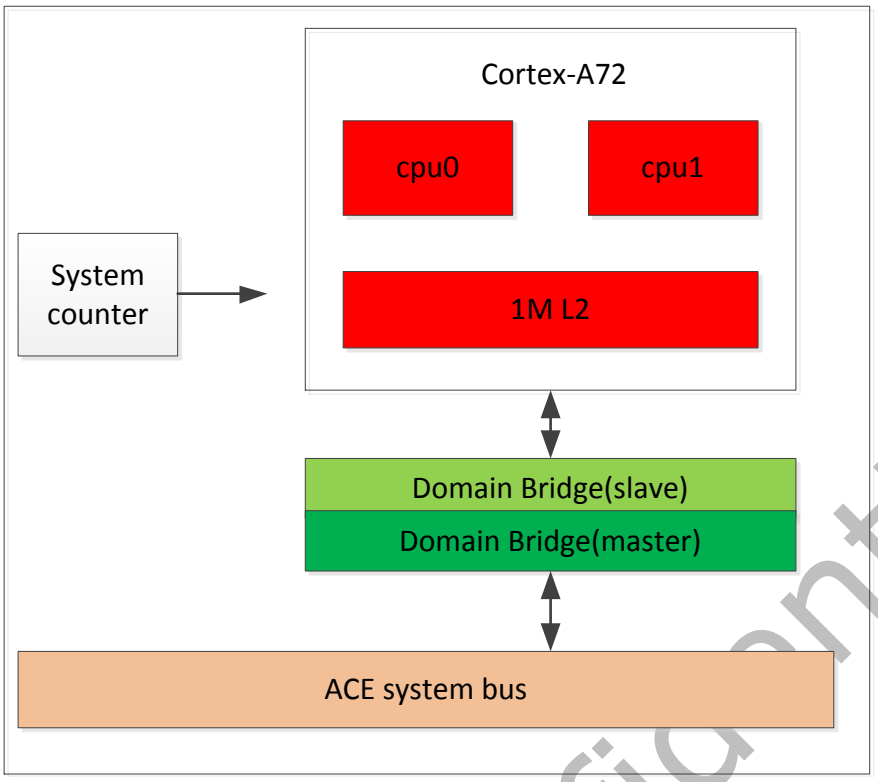


Fig. 5-1 Block Diagram

Chapter 6 Cortex-A53

6.1 Overview

The RK3399 has a quad-core Cortex-A53 cluster with 512K L2 memory. Cortex-A53 processor, which is a mid-range, low-power processor that implements the ARMv8-A architecture.
The Cortex-A53 processor includes following features:

- Full implementation of the ARMv8-A architecture instruction set
- Support for both AArch32 and AArch64 Execution status.
- Support for all exception levels, EL0, EL1, EL2, and EL3, in each execution states.
- Support A32 instruction set, previously called the ARM instruction set.
- Support T32 instruction set, previously called the Thumb instruction set.
- Support A64 instruction set.
- In-order pipeline with symmetric dual-issue of most instructions.
- Harvard Level 1(L1) memory system with a Memory Management Unit (MMU).
- Level 2 (L2) memory system providing cluster memory coherency, with L2 cache.
- Support advanced SIMD and Floating-point Extension for integer and floating-point vector operations.
- Support ARMv8 Cryptography Extensions.
- Support AMBA 4 ACE bus architecture.

The configuration details of little cluster and big cluster are shown in following tables

Table 6-1 CPU Configuration

Number of CPU	4
L1 I cache size	32K
L1 D cache size	32K
L2 cache size	512K
L2 data RAM output latency	3 cycles
L2 data RAM input latency	2 cycles
CPU cache protection	No
SCU L2 cache protection	No
BUS master interface	ACE
NEON and floating point support	Yes
Cryptography extension	Yes

6.2 Block Diagram

The Cortex-A53 sub system is shown in Figure 9-1. As illustrated, dual-core Cortex-A53 connects to system bus through asynchronous bridges which can handle with CDC (clock domain crossing) issue.
The Cortex-A53 is connected with system counter, which can run under a constant frequency clock, for PPI interrupt generation.

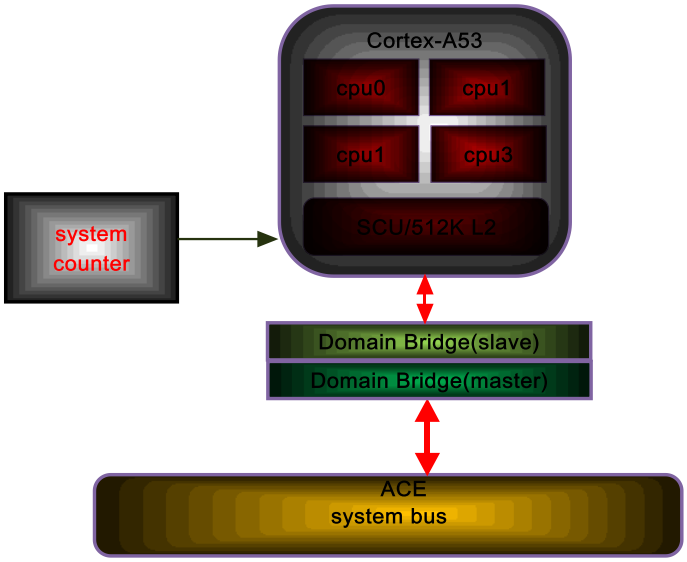


Fig. 6-1 Block Diagram

Chapter 7 Embedded Processor (Cortex-M0)

7.1 Overview

The Cortex-M0 processor is a very low gate count, highly energy efficient processor that is intended for microcontroller and deeply embedded applications that require an area optimized processor.

The processor features and benefits are:

- A low gate count processor that features
  - The ARMv6-M Thumb instruction set
  - Thumb-2 technology
  - Compliant 24-bit SysTick timer
  - Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling
  - Low power sleep-mode entry using Wait For Interrupt (WFI), Wait For Event (WFE) instructions, or the return from interrupt sleep-on-exit feature
- NVIC that features
  - 32 external interrupt inputs, each with four levels of priority
  - Dedicated Non-Maskable Interrupt (NMI) input
  - Optional Wake-up Interrupt Controller (WIC), providing ultra-low power sleep mode support
- Optional debug support
  - Four hardware breakpoints
  - Two watch points
  - Support Serial Wire debug connection
  - single 32-bit AMBA-3 AHB-Lite system interface

7.2 Block Diagram

Cortex-M0 Integration architecture is shown below.

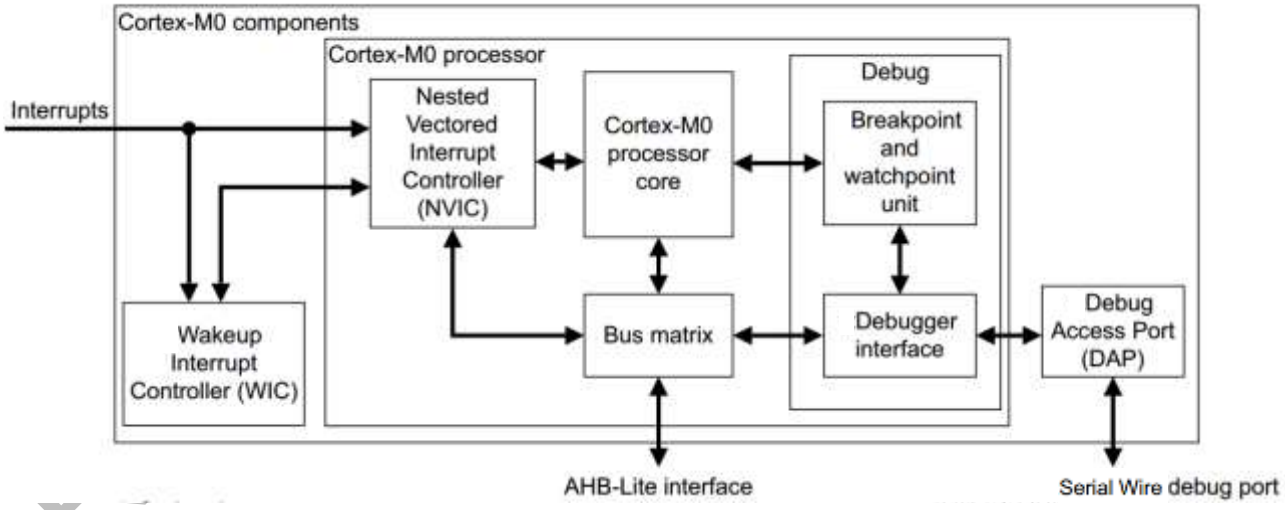


Fig. 7-1 Cortex-M0 Integration Architecture

There are two Cortex-M0 Integration instances in the SOC system, one in PERILP power domain, mainly for normal access, named "PERILPM0"; another is in PMU power domain, mainly for power management, named "PMUM0".

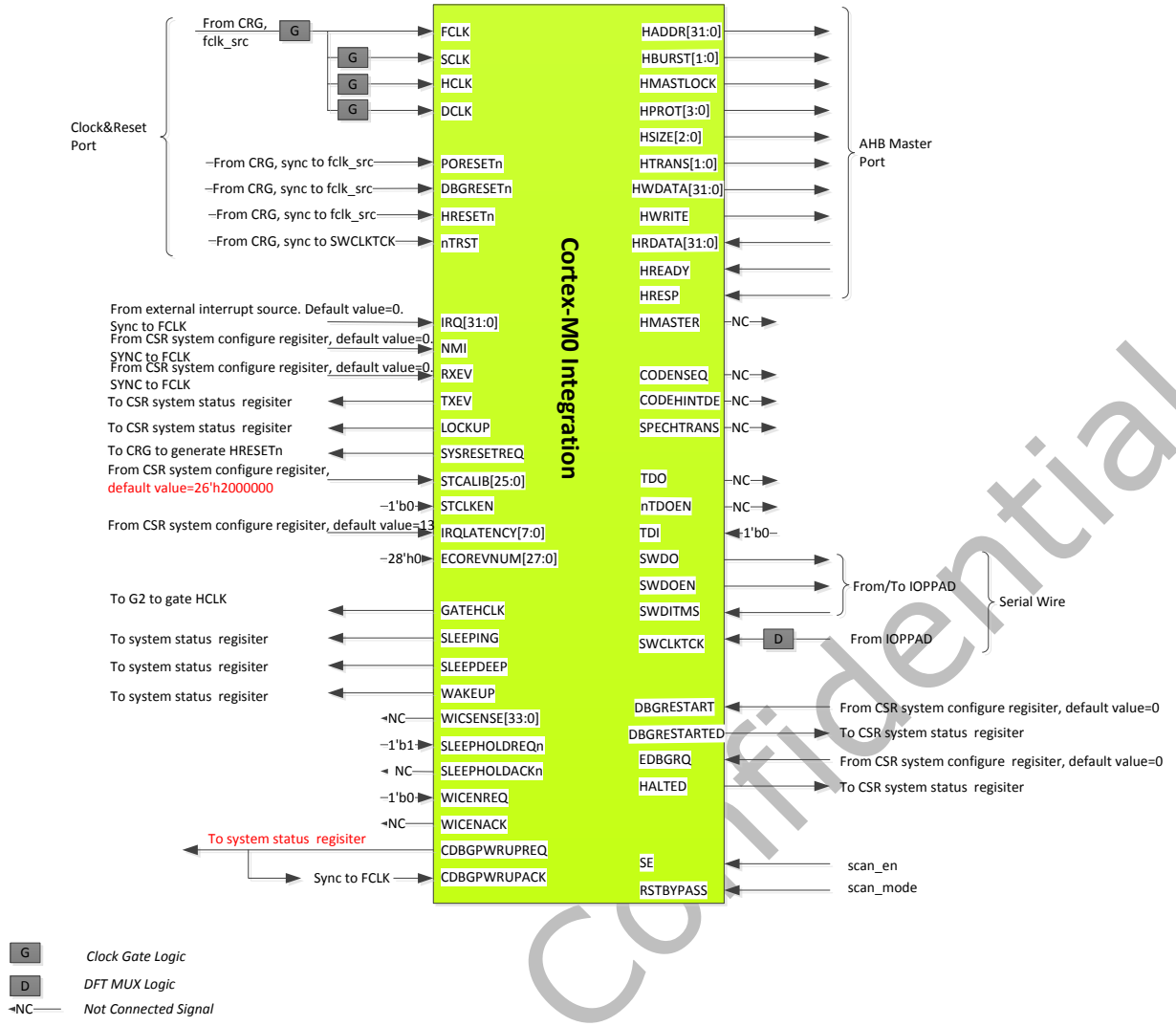


Fig. 7-2 PERILPM0 Architecture

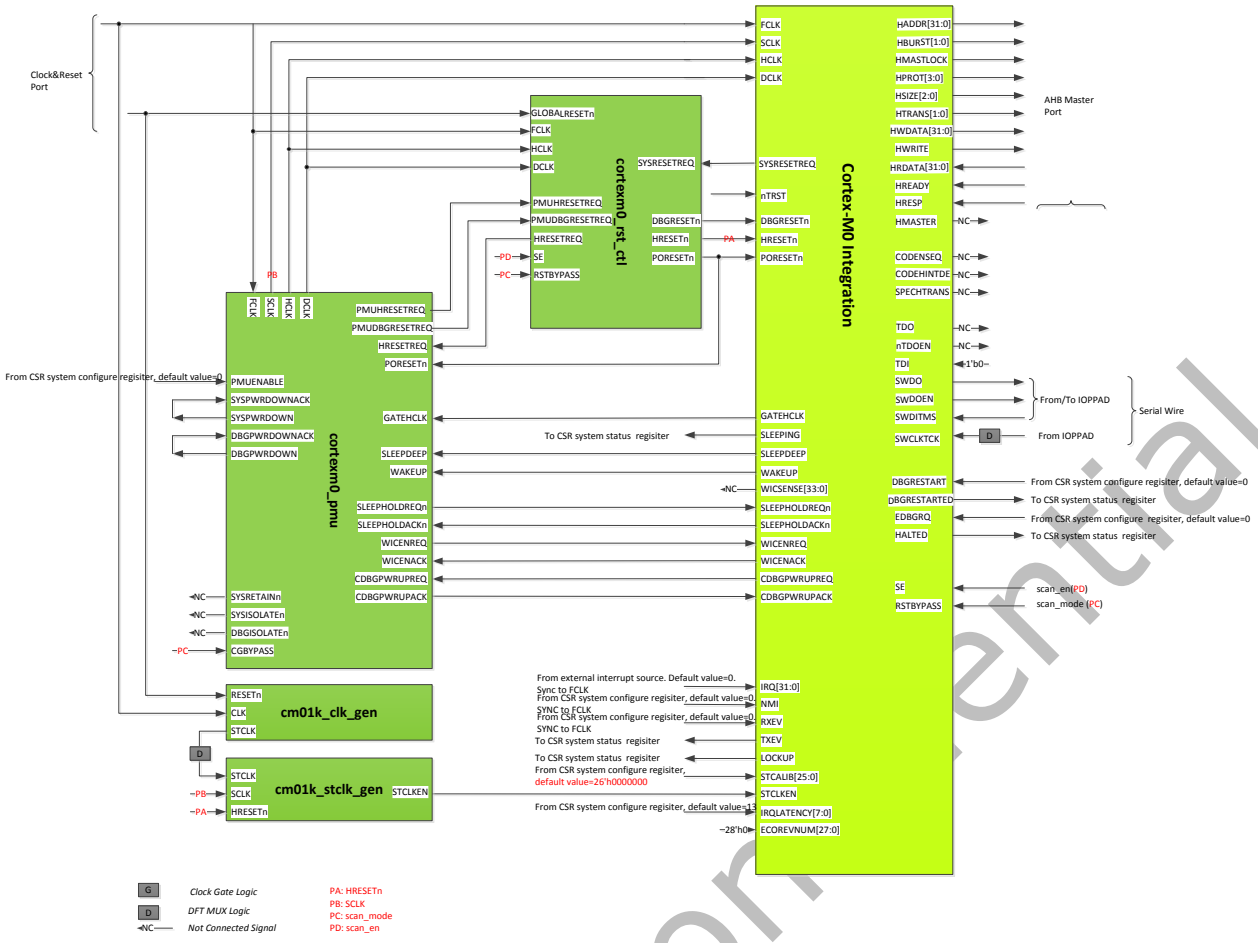


Fig. 7-3 PMUM0 Architecture

7.3 Interface Description

Table 7-1 Cortex-M0 Interface Description

Module Pin	Direction	Pad Name	IOMUX Setting
perilpm0_jtag_tck	I	IO_SDMMCclkout_MCUJTAGtck_HDCPJTAGtck_SDMMCgpio4b4	GRF_GPIO4B_IOMUX[9:8]=2'b10
perilpm0_jtag_tms	I/O	IO_SDMMCcmd_MCUJTAGtms_HDCPJTAGtms_SDMMCgpio4b5	GRF_GPIO4B_IOMUX[11:10]=2'b10
pmum0_jtag_tck	I	IO_PMUM0JTAGtck_SPI1ECclk_PMU1830gpio1b1	PMUGRF_GPIO1B_IOMUX[3:2]=2'b01
pmum0_jtag_tms	I/O	IO_PMUM0JTAGtms_SPI1ECcsn0_PMU1830gpio1b2	PMUGRF_GPIO1B_IOMUX[5:4]=2'b01
perilpm0_sleeping	O	IO_I2Sclk_TRACEctl_LPM0wfi_AUDIOgpio4a0	GRF_GPIO4A_IOMUX[1:0]=2'b11
pmum0_sleeping	O	IO_SDMMCwrprt_PMUM0wfi_TESTclkout2_PMU18gpio0b0	GRF_GPIO0B_IOMUX[1:0]=2'b10

Notes: I=input, O=output, I/O=input/output, bidirectional

7.4 Application Notes

7.4.1 Clock and Reset Generation

The clock and reset generation for PERILPM0 and PMUM0 are different, please refer to "Chapter CRU" for more detailed information.

7.4.2 Memory Remap for PERILPM0

The memory map is divided into different memory types for different usage.
To facilitate the memory remap between different processors, the source space can be remap to another. In addition, these remap operation could not take effect until the CortexM0 is soft reset.

Table 7-2 PERILPM0 Address Remap

Before Remap	Memory Type	Usage	After Remap
0xA0000000 - 0xDFFFFFFF	Device XN	Peripherals	[31:28]: sgrf_perilp_m0_con7[15:12] [27:12]: sgrf_perilp_m0_con6[15:0] [11:00]: 0
0x80000000 - 0x9FFFFFFF	Normal WT	Off chip RAM	[31:28]: sgrf_perilp_m0_con7[11:8] [27:12]: sgrf_perilp_m0_con5[15:0] [11:00]: 0
0x60000000 - 0x7FFFFFFF	Normal WBWA	Off chip RAM	[31:28]: sgrf_perilp_m0_con7[11:8] [27:12]: sgrf_perilp_m0_con5[15:0] [11:00]: 0
0x40000000 - 0x5FFFFFFF	Device XN	Peripherals	Before Remap + 0xB8000000
0x20000000 - 0x3FFFFFFF	Normal WBWA	On chip RAM	[31:28]: sgrf_perilp_m0_con7[7:4] [27:12]: sgrf_perilp_m0_con4[15:0] [11:00]: 0
0x00000000 - 0x1FFFFFFF	Normal WT	ROM or flash	[31:28]: sgrf_perilp_m0_con7[3:0] [27:12]: sgrf_perilp_m0_con3[15:0] [11:00]: 0

Notes:

- *XN means execute-never.*
- *WT means write-through.*
- *WBWA means write-back-write-allocate.*
- *WT means write-through.*

7.4.3 Memory Remap for PMUM0

The memory map is divided into different memory types for different usage.
To facilitate the memory remap between different processors, the source space can be remap to another. In addition, these remap operation could not take effect until the CortexM0 is soft reset.

Table 7-3 PMUM0 Address Remap

Before Remap	Memory Type	Usage	After Remap
0xA0000000 - 0xDFFFFFFF	Device XN	Peripherals	[31:28]: sgrf_pmu_con7[15:12] [27:12]: sgrf_pmu_con6[15:0] [11:00]: 0
0x80000000 - 0x9FFFFFFF	Normal WT	Off chip RAM	[31:28]: sgrf_pmu_con7[11:8] [27:12]: sgrf_pmu_con5[15:0] [11:00]: 0
0x60000000 - 0x7FFFFFFF	Normal WBWA	Off chip RAM	[31:28]: sgrf_pmu_con7[11:8] [27:12]: sgrf_pmu_con5[15:0] [11:00]: 0
0x40000000 - 0x5FFFFFFF	Device XN	Peripherals	Before Remap + 0xB8000000
0x20000000 - 0x3FFFFFFF	Normal WBWA	On chip RAM	[31:28]: sgrf_pmu_con7[7:4] [27:12]: sgrf_pmu_con4[15:0] [11:00]: 0
0x00000000 - 0x1FFFFFFF	Normal WT	ROM or flash	[31:28]: sgrf_pmu_con7[3:0] [27:12]: sgrf_pmu_con3[15:0] [11:00]: 0

Notes:

- *XN means execute-never.*
- *WT means write-through.*
- *WBWA means write-back-write-allocate.*
- *WT means write-through.*

7.4.4 Miscellaneous Signals for PERILPM0

System Configure Signals

Table 7-4 PERILPM0 System Configure Signals

Signal Name	Source	Def	Description
sgrf_perilp_cm0s_rsthold	sgrf_perilp_m0_con0[5]	0	Reset hold control. 0: reset can be asserted 1: reset cannot be asserted, so M0 RESETn will be high
sgrf_con_dbgen_m0_peril	sgrf_perilp_m0_con0[1]	0	SerialWire Debug enable. 0: disable

Signal Name	Source	Def	Description
p			1: enable
sgrf_con_perilp_m0_jtag_rstreqn	sgrf_soc_con0[13]	0	Always be 0
sgrf_con_m0_perilp_sysrstreq_en	sgrf_soc_con0[14]	0	Enable for SYSRESETREQ
sgrf_con_perim0_secure_ctrl	sgrf_soc_con6[13]	1	Master security attribute: 0: secure 1: no-secure
grf_con_m0_perilp_stcalib[25:0]	{sgrf_perilp_m0_con2[9:0], sgrf_perilp_m0_con1[15:0]}	0	[25]: NOREF. Indicates that no alternative reference clock source has been integrated. Tie HIGH if STCLKEN has been tied off. [24]: SKEW. Tie this LOW if the system timer clock, the external reference clock, or SCLK as indicated by STCALIB[25], can guarantee an exact multiple of 10ms. Otherwise, tie this signal HIGH. [23:0]: TENMS. Provides an integer value to compute a 10ms (100Hz) delay from either the reference clock, or SCLK if the reference clock is not implemented.
grf_con_m0_perilp_irqlatency[7:0]	sgrf_perilp_m0_con8[7:0]	0	Minimum number of cycles between an interrupt that becomes pended in the NVIC, and the vector fetch for that interrupt being issued
sgrf_con_nmi_m0_perilp	sgrf_perilp_m0_con0[0]	0	Non-maskable interrupt
sgrf_con_dbgrestart_m0_perilp	sgrf_perilp_m0_con0[2]	0	External restart request
sgrf_con_edbgrq_m0_perilp	sgrf_perilp_m0_con0[3]	0	External debug request
sgrf_con_rxev_m0_perilp	sgrf_perilp_m0_con0[4]	0	A HIGH level on this input causes the architecture defined Event Register to be set in the Cortex-M0 processor. This causes a WFE instruction to complete. It also awakens the processor if it is sleeping as the result of encountering a WFE instruction when the Event Register is clear.

System Status Signals

Table 7-5 PERILPM0 System Status Signals

Signal Name	Destination	Def	Description
m0_perilp_sysresetreq	grf_soc_status2[9]	0	System reset request 0: no effect 1: requests a system level reset.
grf_stat_txev_m0_perilp	grf_soc_status2[6]	0	A single SCLK cycle HIGH level is generated on this output every time an SEV instruction is executed on the Cortex-M0 processor.
grf_stat_m0_perilp_dbgrestarted	grf_soc_status2[5]	1	Handshake for DBGRESTART
grf_stat_m0_perilp_core_halted	grf_soc_status2[4]	0	Indicates that the processor is in debug state. HALTED remains asserted for as long as the processor remains in debug state.
grf_stat_m0_perilp_core_lockup	grf_soc_status2[3]	0	Indicates that the processor is in the architected lock-up state, as the result of an unrecoverable exception.
grf_stat_m0_perilp_sleepdeep	grf_soc_status2[2]	0	Active only when SLEEPING is HIGH. Indicates that the SLEEPDEEP bit in the NVIC is set to 1.
grf_stat_m0_perilp_sleeping	grf_soc_status2[1]	0	Indicates the processor is idle, waiting for an interrupt on either the IRQ, NMI, or internal SysTick, or HIGH level on RXEV.
grf_stat_m0_perilp_wakeup	grf_soc_status2[0]	0	Active HIGH signal to the PMU that indicates a wake-up event has occurred and the processor system domain requires its clocks and power restored.

7.4.5 Miscellaneous Signals for PMUM0

System Configure Signals

Table 7-6 PMuM0 System Configure Signals

Signal Name	Source	Def	Description
sgrf_con_m0_stcalib[25:0]	{sgrf_pmu_con2[9:0],sgrf_pmu_con1[15:0]}	0	[25]: NOREF.Indicates that no alternative reference clock source has been integrated. Tie HIGH if STCLKEN has been tied off. [24]: SKEW. Tie this LOW if the system timer clock, the external reference clock, or SCLK as indicated by STCALIB[25], can guarantee an exact multiple of 10ms. Otherwise, tie this signal HIGH. [23:0]: TENMS. Provides an integer value to compute a 10ms (100Hz) delay from either the reference clock, or SCLK if the reference clock is not implemented.
sgrf_con_irqlatency_m0[7:0]	sgrf_pmu_con8[7:0]	0	Minimum number of cycles between an interrupt that becomes pended in the NVIC, and the vector fetch for that interrupt being issued
sgrf_pmu_cm0_nmi	sgrf_pmu_con0[0]	0	Non-maskable interrupt
sgrf_pmu_enable	sgrf_pmu_con0[1]	0	Internal PMU enable 0: disable 1: enable
sgrf_mcu_dbgrestart	sgrf_pmu_con0[2]	0	External restart request.
sgrf_mcu_edbgrq	sgrf_pmu_con0[3]	0	External debug request.
sgrf_mcu_rxev	sgrf_pmu_con0[4]	0	A HIGH level on this input causes the architecture defined Event Register to be set in the Cortex-M0 processor. This causes a WFE instruction to complete. It also awakens the processor if it is sleeping as the result of encountering a WFE instruction when the Event Register is clear.
sgrf_mcu_dbgen	sgrf_pmu_con0[5]	0	SerialWire Debug enable. 0: disable 1: enable
sgrf_pmu_cm0s_rsthold	sgrf_pmu_con0[6]	0	Reset hold control. 0: reset can be asserted 1: reset cannot be asserted, so M0 RESETn will be high
sgrf_pmu_cm0_mst_ctrl	sgrf_pmu_con0[7]	1	Master security attribute: 0: secure 1: no-secure

System Status Signals

Table 7-7 PMUM0 System Status Signals

Signal Name	Destination	Def	Description
grf_stat_mcu_txev	pmugrf_soc_status0[5]	0	A single SCLK cycle HIGH level is generated on this output every time an SEV instruction is executed on the Cortex-M0 processor.
grf_stat_mcu_dbgrestarted	pmugrf_soc_status0[4]	1	Handshake for DBGRESTART
grf_stat_mcu_core_halted	pmugrf_soc_status0[3]	0	Indicates that the processor is in debug state. HALTED remains asserted for as long as the processor remains in debug state.
grf_stat_mcu_core_lockup	pmugrf_soc_status0[2]	0	Indicates that the processor is in the architected lock-up state, as the result of an unrecoverable exception.
grf_stat_mcu_sleeping	pmugrf_soc_status0[1]	0	Active only when SLEEPING is HIGH. Indicates that the SLEEPDEEP bit in the NVIC is set to 1.
mcu_sleepdeep	pmugrf_soc_status0[0]	0	Indicates the processor is idle, waiting for an interrupt on either the IRQ, NMI, or internal SysTick, or HIGH level on RXEV.

7.4.6 Interrupt Source Arbiter for PERILPM0

The processor supports 32 external interrupt inputs, IRQ[31:0].

Every interrupt input has 8 interrupt sources, except IRQ[18]~IRQ[31] which has no interrupt source.
For IRQ[0]~IRQ[17]: Every interrupt source will be active and output to IRQ[i](i=0~17) by asserting the corresponding bit in INTR_ARB_MASKi(i=0~17). For example, if INTR_ARB_MASK1[1] is asserted to 1, then IRQ[1] is determined by dp_irq. The software can find out the acting interrupt source by reading INTR_ARB_FLAGi. For example, if INTR_ARB_FLAG1[1] is equal to 1, then it is considered that the dp_irq is active now.
INTR_ARB_MASKi(i=0~17) is write/read available, and the base address is (0xff798000 + 0x00+4*i).
INTR_ARB_FLAGi (i=0~17) is read only, and the base address is (0xff798000 + 0x80+4*i).
The relationship between IRQ[31:0], interrupt source, INTR_ARB_MASKi and INTR_ARB_FLAGi is shown below.

Table 7-8 Interrupt Source for PERILPM0

IRQ [31:0]	Int Source ID	Int Source	Int Arbiter Mask	Int Arbiter Flag
IRQ[0]	0	crypto0_int	INTR_ARB_MASK0[0]	INTR_ARB_FLAG0[0]
	1	dcf_done_int	INTR_ARB_MASK0[1]	INTR_ARB_FLAG0[1]
	2	dcf_error_int	INTR_ARB_MASK0[2]	INTR_ARB_FLAG0[2]
	3	ddrc0_int	INTR_ARB_MASK0[3]	INTR_ARB_FLAG0[3]
	4	ddrc1_int	INTR_ARB_MASK0[4]	INTR_ARB_FLAG0[4]
	5	dmac0_perilp_irq_abort	INTR_ARB_MASK0[5]	INTR_ARB_FLAG0[5]
	6	dmac0_perilp_irq	INTR_ARB_MASK0[6]	INTR_ARB_FLAG0[6]
	7	dmac1_perilp_irq_abort	INTR_ARB_MASK0[7]	INTR_ARB_FLAG0[7]
IRQ[1]	8	dmac1_perilp_irq	INTR_ARB_MASK1[0]	INTR_ARB_FLAG1[0]
	9	dp_irq	INTR_ARB_MASK1[1]	INTR_ARB_FLAG1[1]
	10	edp_irq	INTR_ARB_MASK1[2]	INTR_ARB_FLAG1[2]
	11	emmccore_int	INTR_ARB_MASK1[3]	INTR_ARB_FLAG1[3]
	12	gmac_int	INTR_ARB_MASK1[4]	INTR_ARB_FLAG1[4]
	13	gmac_pmt_int	INTR_ARB_MASK1[5]	INTR_ARB_FLAG1[5]
	14	gpio0_int	INTR_ARB_MASK1[6]	INTR_ARB_FLAG1[6]
	15	gpio1_int	INTR_ARB_MASK1[7]	INTR_ARB_FLAG1[7]
IRQ[2]	16	gpio2_intr	INTR_ARB_MASK2[0]	INTR_ARB_FLAG2[0]
	17	gpio3_intr	INTR_ARB_MASK2[1]	INTR_ARB_FLAG2[1]
	18	gpio4_intr	INTR_ARB_MASK2[2]	INTR_ARB_FLAG2[2]
	19	gpu_irqgpu	INTR_ARB_MASK2[3]	INTR_ARB_FLAG2[3]
	20	gpu_irqjob	INTR_ARB_MASK2[4]	INTR_ARB_FLAG2[4]
	21	gpu_irqmmu	INTR_ARB_MASK2[5]	INTR_ARB_FLAG2[5]
	22	hdcp22_irq	INTR_ARB_MASK2[6]	INTR_ARB_FLAG2[6]
	23	hdmi_irq	INTR_ARB_MASK2[7]	INTR_ARB_FLAG2[7]
IRQ[3]	24	hdmi_wakeup_irq	INTR_ARB_MASK3[0]	INTR_ARB_FLAG3[0]
	25	host0_arb_int	INTR_ARB_MASK3[1]	INTR_ARB_FLAG3[1]
	26	host0_ehci_int	INTR_ARB_MASK3[2]	INTR_ARB_FLAG3[2]
	27	host0_linestate_irq	INTR_ARB_MASK3[3]	INTR_ARB_FLAG3[3]
	28	host0_ohci_int	INTR_ARB_MASK3[4]	INTR_ARB_FLAG3[4]
	29	host1_arb_int	INTR_ARB_MASK3[5]	INTR_ARB_FLAG3[5]
	30	host1_ehci_int	INTR_ARB_MASK3[6]	INTR_ARB_FLAG3[6]
	31	host1_linestate_irq	INTR_ARB_MASK3[7]	INTR_ARB_FLAG3[7]
IRQ[4]	32	host1_ohci_int	INTR_ARB_MASK4[0]	INTR_ARB_FLAG4[0]
	33	hsic_int	INTR_ARB_MASK4[1]	INTR_ARB_FLAG4[1]
	34	i2c3_int	INTR_ARB_MASK4[2]	INTR_ARB_FLAG4[2]
	35	i2c2_int	INTR_ARB_MASK4[3]	INTR_ARB_FLAG4[3]
	36	i2c7_int	INTR_ARB_MASK4[4]	INTR_ARB_FLAG4[4]
	37	i2c6_int	INTR_ARB_MASK4[5]	INTR_ARB_FLAG4[5]
	38	i2c5_int	INTR_ARB_MASK4[6]	INTR_ARB_FLAG4[6]
	39	i2s0_int	INTR_ARB_MASK4[7]	INTR_ARB_FLAG4[7]
IRQ[5]	40	i2s1_int	INTR_ARB_MASK5[0]	INTR_ARB_FLAG5[0]
	41	i2s2_int	INTR_ARB_MASK5[1]	INTR_ARB_FLAG5[1]
	42	iep_intr	INTR_ARB_MASK5[2]	INTR_ARB_FLAG5[2]
	43	isp0_irq	INTR_ARB_MASK5[3]	INTR_ARB_FLAG5[3]
	44	isp1_irq	INTR_ARB_MASK5[4]	INTR_ARB_FLAG5[4]
	45	mipi_dsi_host0_irq	INTR_ARB_MASK5[5]	INTR_ARB_FLAG5[5]

IRQ [31:0]	Int Source ID	Int Source	Int Arbiter Mask	Int Arbiter Flag
	46	mipi_dsi_host1_irq	INTR_ARB_MASK5[6]	INTR_ARB_FLAG5[6]
	47	errirq_cci	INTR_ARB_MASK5[7]	INTR_ARB_FLAG5[7]
IRQ[6]	48	noc_intr	INTR_ARB_MASK6[0]	INTR_ARB_FLAG6[0]
	49	pcie_sys_int	INTR_ARB_MASK6[1]	INTR_ARB_FLAG6[1]
	50	pcie_legacy_int	INTR_ARB_MASK6[2]	INTR_ARB_FLAG6[2]
	51	pcie_client_int	INTR_ARB_MASK6[3]	INTR_ARB_FLAG6[3]
	52	spi2_int	INTR_ARB_MASK6[4]	INTR_ARB_FLAG6[4]
	53	spi1_int	INTR_ARB_MASK6[5]	INTR_ARB_FLAG6[5]
	54	pmu_int	INTR_ARB_MASK6[6]	INTR_ARB_FLAG6[6]
	55	rga_intr	INTR_ARB_MASK6[7]	INTR_ARB_FLAG6[7]
IRQ[7]	56	i2c4_int	INTR_ARB_MASK7[0]	INTR_ARB_FLAG7[0]
	57	i2c0_int	INTR_ARB_MASK7[1]	INTR_ARB_FLAG7[1]
	58	i2c8_int	INTR_ARB_MASK7[2]	INTR_ARB_FLAG7[2]
	59	i2c1_int	INTR_ARB_MASK7[3]	INTR_ARB_FLAG7[3]
	60	spi3_int	INTR_ARB_MASK7[4]	INTR_ARB_FLAG7[4]
	61	pwm_int	INTR_ARB_MASK7[5]	INTR_ARB_FLAG7[5]
	62	saradc_int	INTR_ARB_MASK7[6]	INTR_ARB_FLAG7[6]
	63	sd_detectn_irq	INTR_ARB_MASK7[7]	INTR_ARB_FLAG7[7]
IRQ[8]	64	sdio_int	INTR_ARB_MASK8[0]	INTR_ARB_FLAG8[0]
	65	sdmmc_int	INTR_ARB_MASK8[1]	INTR_ARB_FLAG8[1]
	66	spdif_int	INTR_ARB_MASK8[2]	INTR_ARB_FLAG8[2]
	67	spi4_int	INTR_ARB_MASK8[3]	INTR_ARB_FLAG8[3]
	68	spi0_int	INTR_ARB_MASK8[4]	INTR_ARB_FLAG8[4]
	69	stimer_intr0	INTR_ARB_MASK8[5]	INTR_ARB_FLAG8[5]
	70	stimer_intr1	INTR_ARB_MASK8[6]	INTR_ARB_FLAG8[6]
	71	stimer_intr2	INTR_ARB_MASK8[7]	INTR_ARB_FLAG8[7]
IRQ[9]	72	stimer_intr3	INTR_ARB_MASK9[0]	INTR_ARB_FLAG9[0]
	73	stimer_intr4	INTR_ARB_MASK9[1]	INTR_ARB_FLAG9[1]
	74	stimer_intr5	INTR_ARB_MASK9[2]	INTR_ARB_FLAG9[2]
	75	stimer_intr6	INTR_ARB_MASK9[3]	INTR_ARB_FLAG9[3]
	76	stimer_intr7	INTR_ARB_MASK9[4]	INTR_ARB_FLAG9[4]
	77	stimer_intr8	INTR_ARB_MASK9[5]	INTR_ARB_FLAG9[5]
	78	stimer_intr9	INTR_ARB_MASK9[6]	INTR_ARB_FLAG9[6]
	79	stimer_intr10	INTR_ARB_MASK9[7]	INTR_ARB_FLAG9[7]
IRQ[10]	80	stimer_intr11	INTR_ARB_MASK10[0]	INTR_ARB_FLAG10[0]
	81	timer_intr0	INTR_ARB_MASK10[1]	INTR_ARB_FLAG10[1]
	82	timer_intr1	INTR_ARB_MASK10[2]	INTR_ARB_FLAG10[2]
	83	timer_intr2	INTR_ARB_MASK10[3]	INTR_ARB_FLAG10[3]
	84	timer_intr3	INTR_ARB_MASK10[4]	INTR_ARB_FLAG10[4]
	85	timer_intr4	INTR_ARB_MASK10[5]	INTR_ARB_FLAG10[5]
	86	timer_intr5	INTR_ARB_MASK10[6]	INTR_ARB_FLAG10[6]
	87	timer_intr6	INTR_ARB_MASK10[7]	INTR_ARB_FLAG10[7]
IRQ[11]	88	timer_intr7	INTR_ARB_MASK11[0]	INTR_ARB_FLAG11[0]
	89	timer_intr8	INTR_ARB_MASK11[1]	INTR_ARB_FLAG11[1]
	90	timer_intr9	INTR_ARB_MASK11[2]	INTR_ARB_FLAG11[2]
	91	timer_intr10	INTR_ARB_MASK11[3]	INTR_ARB_FLAG11[3]
	92	timer_intr11	INTR_ARB_MASK11[4]	INTR_ARB_FLAG11[4]
	93	perf_int_a53	INTR_ARB_MASK11[5]	INTR_ARB_FLAG11[5]
	94	perf_int_a72	INTR_ARB_MASK11[6]	INTR_ARB_FLAG11[6]
	95	pmutimer_int0	INTR_ARB_MASK11[7]	INTR_ARB_FLAG11[7]
IRQ[12]	96	pmutimer_int1	INTR_ARB_MASK12[0]	INTR_ARB_FLAG12[0]
	97	tsadc_int	INTR_ARB_MASK12[1]	INTR_ARB_FLAG12[1]
	98	uart1_int	INTR_ARB_MASK12[2]	INTR_ARB_FLAG12[2]
	99	uart0_int	INTR_ARB_MASK12[3]	INTR_ARB_FLAG12[3]
	100	uart2_int	INTR_ARB_MASK12[4]	INTR_ARB_FLAG12[4]
	101	uart3_int	INTR_ARB_MASK12[5]	INTR_ARB_FLAG12[5]
	102	uart4_int	INTR_ARB_MASK12[6]	INTR_ARB_FLAG12[6]
	103	usb3otg0_bvalid_irq	INTR_ARB_MASK12[7]	INTR_ARB_FLAG12[7]
IRQ[13]	104	usb3otg0_id_irq	INTR_ARB_MASK13[0]	INTR_ARB_FLAG13[0]
	105	usb3otg0_int	INTR_ARB_MASK13[1]	INTR_ARB_FLAG13[1]
	106	usb3otg0_linestate_irq	INTR_ARB_MASK13[2]	INTR_ARB_FLAG13[2]

IRQ [31:0]	Int Source ID	Int Source	Int Arbiter Mask	Int Arbiter Flag
	107	usb3otg0_rxdet_irq	INTR_ARB_MASK13[3]	INTR_ARB_FLAG13[3]
	108	usb3otg1_bvalid_irq	INTR_ARB_MASK13[4]	INTR_ARB_FLAG13[4]
	109	usb3otg1_id_irq	INTR_ARB_MASK13[5]	INTR_ARB_FLAG13[5]
	110	usb3otg1_int	INTR_ARB_MASK13[6]	INTR_ARB_FLAG13[6]
	111	usb3otg1_linestate_irq	INTR_ARB_MASK13[7]	INTR_ARB_FLAG13[7]
IRQ[14]	112	usb3otg1_rxdet_irq	INTR_ARB_MASK14[0]	INTR_ARB_FLAG14[0]
	113	vcodec_dec_int	INTR_ARB_MASK14[1]	INTR_ARB_FLAG14[1]
	114	vcodec_enc_int	INTR_ARB_MASK14[2]	INTR_ARB_FLAG14[2]
	115	vcodec_mmu_int	INTR_ARB_MASK14[3]	INTR_ARB_FLAG14[3]
	116	vdu_dec_irq	INTR_ARB_MASK14[4]	INTR_ARB_FLAG14[4]
	117	vdu_mmu_irq	INTR_ARB_MASK14[5]	INTR_ARB_FLAG14[5]
	118	vopbig_irq	INTR_ARB_MASK14[6]	INTR_ARB_FLAG14[6]
	119	voplit_irq	INTR_ARB_MASK14[7]	INTR_ARB_FLAG14[7]
IRQ[15]	120	wdt0_intr	INTR_ARB_MASK15[0]	INTR_ARB_FLAG15[0]
	121	wdt1_intr	INTR_ARB_MASK15[1]	INTR_ARB_FLAG15[1]
	122	wdt2_int	INTR_ARB_MASK15[2]	INTR_ARB_FLAG15[2]
	123	usb3otg0_pme_generation	INTR_ARB_MASK15[3]	INTR_ARB_FLAG15[3]
	124	usb3otg0_host_legacy_smi_interrupt	INTR_ARB_MASK15[4]	INTR_ARB_FLAG15[4]
	125	usb3otg0_host_sys_err	INTR_ARB_MASK15[5]	INTR_ARB_FLAG15[5]
	126	usb3otg1_pme_generation	INTR_ARB_MASK15[6]	INTR_ARB_FLAG15[6]
	127	usb3otg1_host_legacy_smi_interrupt	INTR_ARB_MASK15[7]	INTR_ARB_FLAG15[7]
IRQ[16]	128	usb3otg1_host_sys_err	INTR_ARB_MASK16[0]	INTR_ARB_FLAG16[0]
	129	vopbig_irq_ddr	INTR_ARB_MASK16[1]	INTR_ARB_FLAG16[1]
	130	voplit_irq_ddr	INTR_ARB_MASK16[2]	INTR_ARB_FLAG16[2]
	131	ddr_mon_intr	INTR_ARB_MASK16[3]	INTR_ARB_FLAG16[3]
	132	spi5_int	INTR_ARB_MASK16[4]	INTR_ARB_FLAG16[4]
	133	tcpd_int0	INTR_ARB_MASK16[5]	INTR_ARB_FLAG16[5]
	134	tcpd_int1	INTR_ARB_MASK16[6]	INTR_ARB_FLAG16[6]
	135	crypto1_int	INTR_ARB_MASK16[7]	INTR_ARB_FLAG16[7]
IRQ[17]	136	gasket_irq	INTR_ARB_MASK17[0]	INTR_ARB_FLAG17[0]
	137	pcie_rc_mode_elec_idle_irq	INTR_ARB_MASK17[1]	INTR_ARB_FLAG17[1]
	138	\		
	139	\		
	140	perilp_mailbox_int[0]	INTR_ARB_MASK17[4]	INTR_ARB_FLAG17[4]
	141	perilp_mailbox_int[1]	INTR_ARB_MASK17[5]	INTR_ARB_FLAG17[5]
	142	perilp_mailbox_int[2]	INTR_ARB_MASK17[6]	INTR_ARB_FLAG17[6]
	143	perilp_mailbox_int[3]	INTR_ARB_MASK17[7]	INTR_ARB_FLAG17[7]
IRQ[18]~ IRQ[31]	\	Connect to 0	\	\

7.4.7 Interrupt Source Arbiter for PMUM0

The processor supports 32 external interrupt inputs, IRQ[31:0].
Every interrupt input has 8 interrupt sources, except IRQ[18]~IRQ[30] which has only one interrupt source and IRQ[31] which has no interrupt source.
For IRQ[0]~IRQ[17]: Every interrupt source will be active and output to IRQ[i](i=0~17) by asserting the corresponding bit in INTR_ARB_MASKi(i=0~17). For example, if INTR_ARB_MASK1[1] is asserted to 1, then IRQ[1] is determined by dp_irq. The software can find out the acting interrupt source by reading INTR_ARB_FLAGi. For example, if INTR_ARB_FLAG1[1] is equal to 1, then it is considered that the dp_irq is active now.
INTR_ARB_MASKi(i=0~17) is write/read available, and the base address is (0xff79c000 + 0x00+4*i).
INTR_ARB_FLAGi (i=0~17) is read only, and the base address is (0xff79c000 + 0x80+4*i).
The relationship between IRQ[31:0], interrupt source, INTR_ARB_MASKi and INTR_ARB_FLAGi is shown below.

Table 7-9 Interrupt Source for PERILPM0

IRQ [31:0]	Int Arbiter ID	Int Arbiter Source	Int Arbiter Mask	Int Arbiter Flag
IRQ[0]	0	crypto0_int	INTR_ARB_MASK0[0]	INTR_ARB_FLAG0[0]
	1	dcf_done_int	INTR_ARB_MASK0[1]	INTR_ARB_FLAG0[1]
	2	dcf_error_int	INTR_ARB_MASK0[2]	INTR_ARB_FLAG0[2]
	3	ddrc0_int	INTR_ARB_MASK0[3]	INTR_ARB_FLAG0[3]
	4	ddrc1_int	INTR_ARB_MASK0[4]	INTR_ARB_FLAG0[4]
	5	dmac0_perilp_irq_abort	INTR_ARB_MASK0[5]	INTR_ARB_FLAG0[5]
	6	dmac0_perilp_irq	INTR_ARB_MASK0[6]	INTR_ARB_FLAG0[6]
	7	dmac1_perilp_irq_abort	INTR_ARB_MASK0[7]	INTR_ARB_FLAG0[7]
IRQ[1]	8	dmac1_perilp_irq	INTR_ARB_MASK1[0]	INTR_ARB_FLAG1[0]
	9	dp_irq	INTR_ARB_MASK1[1]	INTR_ARB_FLAG1[1]
	10	edp_irq	INTR_ARB_MASK1[2]	INTR_ARB_FLAG1[2]
	11	emmccore_int	INTR_ARB_MASK1[3]	INTR_ARB_FLAG1[3]
	12	gmac_int	INTR_ARB_MASK1[4]	INTR_ARB_FLAG1[4]
	13	gmac_pmt_int	INTR_ARB_MASK1[5]	INTR_ARB_FLAG1[5]
	14	gpio0_int	INTR_ARB_MASK1[6]	INTR_ARB_FLAG1[6]
	15	gpio1_int	INTR_ARB_MASK1[7]	INTR_ARB_FLAG1[7]
IRQ[2]	16	gpio2_intr	INTR_ARB_MASK2[0]	INTR_ARB_FLAG2[0]
	17	gpio3_intr	INTR_ARB_MASK2[1]	INTR_ARB_FLAG2[1]
	18	gpio4_intr	INTR_ARB_MASK2[2]	INTR_ARB_FLAG2[2]
	19	gpu_irqgpu	INTR_ARB_MASK2[3]	INTR_ARB_FLAG2[3]
	20	gpu_irqjob	INTR_ARB_MASK2[4]	INTR_ARB_FLAG2[4]
	21	gpu_irqmmu	INTR_ARB_MASK2[5]	INTR_ARB_FLAG2[5]
	22	hdcp22_irq	INTR_ARB_MASK2[6]	INTR_ARB_FLAG2[6]
	23	hdmi_irq	INTR_ARB_MASK2[7]	INTR_ARB_FLAG2[7]
IRQ[3]	24	hdmi_wakeup_irq	INTR_ARB_MASK3[0]	INTR_ARB_FLAG3[0]
	25	host0_arb_int	INTR_ARB_MASK3[1]	INTR_ARB_FLAG3[1]
	26	host0_ehci_int	INTR_ARB_MASK3[2]	INTR_ARB_FLAG3[2]
	27	host0_linestate_irq	INTR_ARB_MASK3[3]	INTR_ARB_FLAG3[3]
	28	host0_ohci_int	INTR_ARB_MASK3[4]	INTR_ARB_FLAG3[4]
	29	host1_arb_int	INTR_ARB_MASK3[5]	INTR_ARB_FLAG3[5]
	30	host1_ehci_int	INTR_ARB_MASK3[6]	INTR_ARB_FLAG3[6]
	31	host1_linestate_irq	INTR_ARB_MASK3[7]	INTR_ARB_FLAG3[7]
IRQ[4]	32	host1_ohci_int	INTR_ARB_MASK4[0]	INTR_ARB_FLAG4[0]
	33	hsic_int	INTR_ARB_MASK4[1]	INTR_ARB_FLAG4[1]
	34	i2c3_int	INTR_ARB_MASK4[2]	INTR_ARB_FLAG4[2]
	35	i2c2_int	INTR_ARB_MASK4[3]	INTR_ARB_FLAG4[3]
	36	i2c7_int	INTR_ARB_MASK4[4]	INTR_ARB_FLAG4[4]
	37	i2c6_int	INTR_ARB_MASK4[5]	INTR_ARB_FLAG4[5]
	38	i2c5_int	INTR_ARB_MASK4[6]	INTR_ARB_FLAG4[6]
	39	i2s0_int	INTR_ARB_MASK4[7]	INTR_ARB_FLAG4[7]
IRQ[5]	40	i2s1_int	INTR_ARB_MASK5[0]	INTR_ARB_FLAG5[0]
	41	i2s2_int	INTR_ARB_MASK5[1]	INTR_ARB_FLAG5[1]
	42	iep_intr	INTR_ARB_MASK5[2]	INTR_ARB_FLAG5[2]
	43	isp0_irq	INTR_ARB_MASK5[3]	INTR_ARB_FLAG5[3]
	44	isp1_irq	INTR_ARB_MASK5[4]	INTR_ARB_FLAG5[4]
	45	mipi_dsi_host0_irq	INTR_ARB_MASK5[5]	INTR_ARB_FLAG5[5]
	46	mipi_dsi_host1_irq	INTR_ARB_MASK5[6]	INTR_ARB_FLAG5[6]
	47	errirq_cci	INTR_ARB_MASK5[7]	INTR_ARB_FLAG5[7]
IRQ[6]	48	noc_intr	INTR_ARB_MASK6[0]	INTR_ARB_FLAG6[0]
	49	pcie_sys_int	INTR_ARB_MASK6[1]	INTR_ARB_FLAG6[1]
	50	pcie_legacy_int	INTR_ARB_MASK6[2]	INTR_ARB_FLAG6[2]
	51	pcie_client_int	INTR_ARB_MASK6[3]	INTR_ARB_FLAG6[3]
	52	spi2_int	INTR_ARB_MASK6[4]	INTR_ARB_FLAG6[4]
	53	spi1_int	INTR_ARB_MASK6[5]	INTR_ARB_FLAG6[5]
	54	pmu_int	INTR_ARB_MASK6[6]	INTR_ARB_FLAG6[6]
	55	rga_intr	INTR_ARB_MASK6[7]	INTR_ARB_FLAG6[7]
IRQ[7]	56	i2c4_int	INTR_ARB_MASK7[0]	INTR_ARB_FLAG7[0]
	57	i2c0_int	INTR_ARB_MASK7[1]	INTR_ARB_FLAG7[1]
	58	i2c8_int	INTR_ARB_MASK7[2]	INTR_ARB_FLAG7[2]
	59	i2c1_int	INTR_ARB_MASK7[3]	INTR_ARB_FLAG7[3]

IRQ [31:0]	Int Arbiter ID	Int Arbiter Source	Int Arbiter Mask	Int Arbiter Flag
	60	spi3_int	INTR_ARB_MASK7[4]	INTR_ARB_FLAG7[4]
	61	pwm_int	INTR_ARB_MASK7[5]	INTR_ARB_FLAG7[5]
	62	saradc_int	INTR_ARB_MASK7[6]	INTR_ARB_FLAG7[6]
	63	sd_detectn_irq	INTR_ARB_MASK7[7]	INTR_ARB_FLAG7[7]
IRQ[8]	64	sdio_int	INTR_ARB_MASK8[0]	INTR_ARB_FLAG8[0]
	65	sdmmc_int	INTR_ARB_MASK8[1]	INTR_ARB_FLAG8[1]
	66	spdif_int	INTR_ARB_MASK8[2]	INTR_ARB_FLAG8[2]
	67	spi4_int	INTR_ARB_MASK8[3]	INTR_ARB_FLAG8[3]
	68	spi0_int	INTR_ARB_MASK8[4]	INTR_ARB_FLAG8[4]
	69	stimer_intr0	INTR_ARB_MASK8[5]	INTR_ARB_FLAG8[5]
	70	stimer_intr1	INTR_ARB_MASK8[6]	INTR_ARB_FLAG8[6]
	71	stimer_intr2	INTR_ARB_MASK8[7]	INTR_ARB_FLAG8[7]
IRQ[9]	72	stimer_intr3	INTR_ARB_MASK9[0]	INTR_ARB_FLAG9[0]
	73	stimer_intr4	INTR_ARB_MASK9[1]	INTR_ARB_FLAG9[1]
	74	stimer_intr5	INTR_ARB_MASK9[2]	INTR_ARB_FLAG9[2]
	75	stimer_intr6	INTR_ARB_MASK9[3]	INTR_ARB_FLAG9[3]
	76	stimer_intr7	INTR_ARB_MASK9[4]	INTR_ARB_FLAG9[4]
	77	stimer_intr8	INTR_ARB_MASK9[5]	INTR_ARB_FLAG9[5]
	78	stimer_intr9	INTR_ARB_MASK9[6]	INTR_ARB_FLAG9[6]
	79	stimer_intr10	INTR_ARB_MASK9[7]	INTR_ARB_FLAG9[7]
IRQ[10]	80	stimer_intr11	INTR_ARB_MASK10[0]	INTR_ARB_FLAG10[0]
	81	timer_intr0	INTR_ARB_MASK10[1]	INTR_ARB_FLAG10[1]
	82	timer_intr1	INTR_ARB_MASK10[2]	INTR_ARB_FLAG10[2]
	83	timer_intr2	INTR_ARB_MASK10[3]	INTR_ARB_FLAG10[3]
	84	timer_intr3	INTR_ARB_MASK10[4]	INTR_ARB_FLAG10[4]
	85	timer_intr4	INTR_ARB_MASK10[5]	INTR_ARB_FLAG10[5]
	86	timer_intr5	INTR_ARB_MASK10[6]	INTR_ARB_FLAG10[6]
	87	timer_intr6	INTR_ARB_MASK10[7]	INTR_ARB_FLAG10[7]
IRQ[11]	88	timer_intr7	INTR_ARB_MASK11[0]	INTR_ARB_FLAG11[0]
	89	timer_intr8	INTR_ARB_MASK11[1]	INTR_ARB_FLAG11[1]
	90	timer_intr9	INTR_ARB_MASK11[2]	INTR_ARB_FLAG11[2]
	91	timer_intr10	INTR_ARB_MASK11[3]	INTR_ARB_FLAG11[3]
	92	timer_intr11	INTR_ARB_MASK11[4]	INTR_ARB_FLAG11[4]
	93	perf_int_a53	INTR_ARB_MASK11[5]	INTR_ARB_FLAG11[5]
	94	perf_int_a72	INTR_ARB_MASK11[6]	INTR_ARB_FLAG11[6]
	95	pmutimer_int0	INTR_ARB_MASK11[7]	INTR_ARB_FLAG11[7]
IRQ[12]	96	pmutimer_int1	INTR_ARB_MASK12[0]	INTR_ARB_FLAG12[0]
	97	tsadc_int	INTR_ARB_MASK12[1]	INTR_ARB_FLAG12[1]
	98	uart1_int	INTR_ARB_MASK12[2]	INTR_ARB_FLAG12[2]
	99	uart0_int	INTR_ARB_MASK12[3]	INTR_ARB_FLAG12[3]
	100	uart2_int	INTR_ARB_MASK12[4]	INTR_ARB_FLAG12[4]
	101	uart3_int	INTR_ARB_MASK12[5]	INTR_ARB_FLAG12[5]
	102	uart4_int	INTR_ARB_MASK12[6]	INTR_ARB_FLAG12[6]
	103	usb3otg0_bvalid_irq	INTR_ARB_MASK12[7]	INTR_ARB_FLAG12[7]
IRQ[13]	104	usb3otg0_id_irq	INTR_ARB_MASK13[0]	INTR_ARB_FLAG13[0]
	105	usb3otg0_int	INTR_ARB_MASK13[1]	INTR_ARB_FLAG13[1]
	106	usb3otg0_linestate_irq	INTR_ARB_MASK13[2]	INTR_ARB_FLAG13[2]
	107	usb3otg0_rxdet_irq	INTR_ARB_MASK13[3]	INTR_ARB_FLAG13[3]
	108	usb3otg1_bvalid_irq	INTR_ARB_MASK13[4]	INTR_ARB_FLAG13[4]
	109	usb3otg1_id_irq	INTR_ARB_MASK13[5]	INTR_ARB_FLAG13[5]
	110	usb3otg1_int	INTR_ARB_MASK13[6]	INTR_ARB_FLAG13[6]
	111	usb3otg1_linestate_irq	INTR_ARB_MASK13[7]	INTR_ARB_FLAG13[7]
IRQ[14]	112	usb3otg1_rxdet_irq	INTR_ARB_MASK14[0]	INTR_ARB_FLAG14[0]
	113	vcodec_dec_int	INTR_ARB_MASK14[1]	INTR_ARB_FLAG14[1]
	114	vcodec_enc_int	INTR_ARB_MASK14[2]	INTR_ARB_FLAG14[2]
	115	vcodec_mmu_int	INTR_ARB_MASK14[3]	INTR_ARB_FLAG14[3]
	116	vdu_dec_irq	INTR_ARB_MASK14[4]	INTR_ARB_FLAG14[4]
	117	vdu_mmu_irq	INTR_ARB_MASK14[5]	INTR_ARB_FLAG14[5]
	118	vopbig_irq	INTR_ARB_MASK14[6]	INTR_ARB_FLAG14[6]
	119	voplit_irq	INTR_ARB_MASK14[7]	INTR_ARB_FLAG14[7]
IRQ[15]	120	wdt0_intr	INTR_ARB_MASK15[0]	INTR_ARB_FLAG15[0]

IRQ [31:0]	Int Arbiter ID	Int Arbiter Source	Int Arbiter Mask	Int Arbiter Flag
	121	wdt1_intr	INTR_ARB_MASK15[1]	INTR_ARB_FLAG15[1]
	122	wdt2_int	INTR_ARB_MASK15[2]	INTR_ARB_FLAG15[2]
	123	usb3otg0_pme_generation	INTR_ARB_MASK15[3]	INTR_ARB_FLAG15[3]
	124	usb3otg0_host_legacy_smi_interrupt	INTR_ARB_MASK15[4]	INTR_ARB_FLAG15[4]
	125	usb3otg0_host_sys_err	INTR_ARB_MASK15[5]	INTR_ARB_FLAG15[5]
	126	usb3otg1_pme_generation	INTR_ARB_MASK15[6]	INTR_ARB_FLAG15[6]
	127	usb3otg1_host_legacy_smi_interrupt	INTR_ARB_MASK15[7]	INTR_ARB_FLAG15[7]
IRQ[16]	128	usb3otg1_host_sys_err	INTR_ARB_MASK16[0]	INTR_ARB_FLAG16[0]
	129	vopbig_irq_ddr	INTR_ARB_MASK16[1]	INTR_ARB_FLAG16[1]
	130	voplit_irq_ddr	INTR_ARB_MASK16[2]	INTR_ARB_FLAG16[2]
	131	ddr_mon_intr	INTR_ARB_MASK16[3]	INTR_ARB_FLAG16[3]
	132	spi5_int	INTR_ARB_MASK16[4]	INTR_ARB_FLAG16[4]
	133	tcpd_int0	INTR_ARB_MASK16[5]	INTR_ARB_FLAG16[5]
	134	tcpd_int1	INTR_ARB_MASK16[6]	INTR_ARB_FLAG16[6]
	135	crypto1_int	INTR_ARB_MASK16[7]	INTR_ARB_FLAG16[7]
IRQ[17]	136	gasket_irq	INTR_ARB_MASK17[0]	INTR_ARB_FLAG17[0]
	137	pcie_rc_mode_elec_idle_irq	INTR_ARB_MASK17[1]	INTR_ARB_FLAG17[1]
	138	\		
	139	\		
	140	pmu_mailbox_int[0]	INTR_ARB_MASK17[4]	INTR_ARB_FLAG17[4]
	141	pmu_mailbox_int[1]	INTR_ARB_MASK17[5]	INTR_ARB_FLAG17[5]
	142	pmu_mailbox_int[2]	INTR_ARB_MASK17[6]	INTR_ARB_FLAG17[6]
	143	pmu_mailbox_int[3]	INTR_ARB_MASK17[7]	INTR_ARB_FLAG17[7]
IRQ[18]	\	gpio0_int	\	\
IRQ[19]	\	gpio1_int	\	\
IRQ[20]	\	pmu_int	\	\
IRQ[21]	\	i2c_sensor_int	\	\
IRQ[22]	\	i2c_pmu_int	\	\
IRQ[23]	\	i2c_dcdc_int	\	\
IRQ[24]	\	spi_pmu_int	\	\
IRQ[25]	\	rkpwm_pmu_int	\	\
IRQ[26]	\	timer_pmu_int0	\	\
IRQ[27]	\	timer_pmu_int1	\	\
IRQ[28]	\	uartm0_int	\	\
IRQ[29]	\	wdt_m0_pmu_int	\	\
IRQ[30]	\	|pmu_mailbox_int[3:0]	\	\
IRQ[31]	\	\	\	\

Chapter 8 Interconnect

8.1 Overview

The chip-level interconnect consists of main interconnect, peri interconnects and cci500. It enables communication among the modules and subsystems in the device..
The main interconnect supports the following features:

- Cross-bar exchange network
- A special internal slave for accessing the configuration register
- Little-endian platform
- Embedded memory scheduler for DDR transaction generation
- QoS management for optimizing the transaction flow
- Transaction statistics for analyzing the transaction flow
- Security protection mechanism to compatible with the TrustZone technology
- The peri interconnect belong to peripheral system which is responsible for peripheral devices control such as usb device, uart, spi etc.
- CCI500 is used for cache coherency management between Cortex-A72/A53 big cluster and little cluster

8.2 Block Diagram

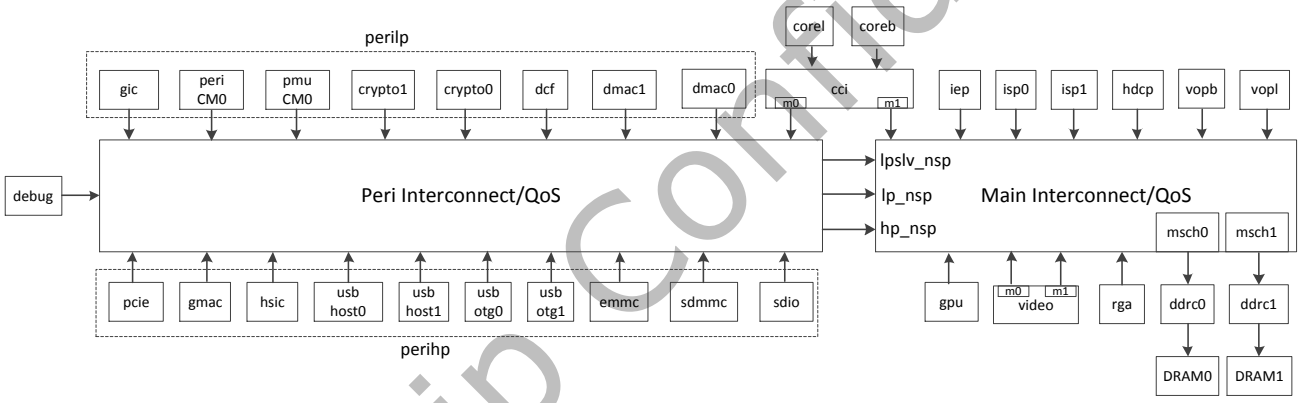


Fig. 8-1 Interconnect diagram

8.3 Function Description

8.3.1 QoS management

The main interconnect is connected with all the related IPs of the system, the interface between the IP and the interconnect is called as NIU(native interface unit). All the master NIU are list as bellowing and they all have one QoS Generator except debug master:

Table 8-1 Master NIUs

Master NIU	Description	Master ID
cci_m0	corel/coreb master, access to any peripheral device	0
cci_m1	corel/coreb master, access to main memory	32
debug	Jtag Debug master, access to any peripheral and	1
dmac0	dmac0 master	5
dmac1	dmac1 master	6
dcf	dcf master	4
crypto0	crypto0 master	3
crypto1	crypto1 master	20
pmu CM0	pmu Cortex-M0	13
peri CM0	peripheral Cortex-M0	12
gic	gic master	8
sdio	sdio master	14
sdmmc	sdmmc master	15

Master NIU	Description	Master ID
emmc	emmc master	7
pcie	pcie master	11
hsic	hsic master	10
gmac	gmac master	9
usb otg0	usb 3.0 otg0 master	16
usb otg1	usb 3.0 otg1 master	17
usb host0	usb 2.0 host0 master	18
usb host1	usb 2.0 host1 master	19
gpu	gpu master	33
video m0	video master 0	39
video m1	video master 1	40
rga	rga master	38
iep	iep master	35
vop-big	vop big master	41
vop-little	vop little master	42
isp0	isp0 master	36
isp1	isp1 master	37
hdcp	hdcp master	34

The interconnect offers 4 modes of qos management:

- None, QoSGenerator is disabled, and priority information are stuck at 0.
- Fixed, QoSGenerator drives apply a fixed urgency to read transactions, and a (possibly different) urgency to write transactions.
- Limiter, QoSGenerator behaves as in fixed mode, but limits the traffic bandwidth coming from that socket, possibly stalling requests if the initiator attempts to exceed its budget.
- Regulator, QoSGenerator promotes are demotes hurry, depending the bandwidth obtained by the initiator is below or beyond a bandwidth budget. As transactions exceeding the bandwidth limit are sent (even though demoted), the regulator mode may be considered as a softer version of the limiter mode.

Limiter Behavior

When configured in bandwidth limiter, the unit uses a 23 bit counter to measure the average bandwidth. This counter has a 1/256 byte resolution and works as follows:

- Adds the number of byte rounded up to 16 (1 -> 16) and then multiplied by 256 to the current value, each time a request is sent.
- Subtracts the Bandwidth register value every cycle. If the Counter becomes negative, force it to 0.
- If the Counter value is greater than the Saturation register value multiplied by 16*256, any incoming request is stalled until this condition disappears. Note that the Counter cannot wrap-around because the maximum value it can reach is: SaturationMax*16*256 + BurstMax*256 = 1023*4K+4K*256 = 5116K or 223 = 8192K.

The following example will show the Counter behavior: 32 byte bursts, F=400MHz, BW=200MB/s, T=0.32us. The Bandwidth register will be set to 256*200/400 = 128, and the Saturation register to 128*0.32*400/4096 = 4 (which corresponds to 64 bytes).

Regulator Behavior

When configured in bandwidth regulator, the unit uses a 23 bit counter to measure the average bandwidth. This counter has a 1/256 byte resolution and works as follows:

- Adds the number of byte rounded up to 16 and then multiplied by 256 to the current value, each time a response is received. If the result is greater than the Saturation register value multiplied by 16*256, saturation to this value is applied.
- Subtracts the Bandwidth register value every cycle. If the Counter becomes negative, force it to 0.
- If the Counter value is less than or equal to the Saturation register value multiplied by 16*256/2, the SocketMst Hurry signal will be set to the HurryHigh register, and HurryLow otherwise. Note that Urgency and Press will be also set to the same value.

The following example will show the Counter behavior: 1Kbyte bursts, F=500MHz, BW=2GB/s,T=2.048us. The Bandwidth register will be set to 256*2000/500 = 1024, and the Saturation register to 1024*2.048*500/4096 = 256 (which corresponds to 4 Kbytes).

QoS Generator Programming

Bandwidth: This log2 (socket.wData/8)+8 bits register defines the bandwidth in 1/256th byte per cycle unit. This allows a 2 MByte/s resolution at 500MHz. When thebandwidth is given in MByte/s, the value of this register will
be equal to 256*BWMB/s / FMHz.

Saturation: This 10 bits register defines the number of byte used for bandwidth measurement. It is expressed in 16bytes unit (up to 16 Kbyte). Usually the integration window is given in us or in cycle: the value of this register will beequal to Bandwidh*Tus*FMHz/(256*16)or Bandwidh*Ncycle/(256*16).

The QoS management for peri-interconnect and main-interconnect inside each interconnect is independent. When master in peri-interconnect access main-interconnect, the QoS will be propagated to main-interconnect according to QoS configuration for 'perilpslv_nsp' (perilp master, cci_m0 and debug access slave register), 'perilp_nsp'(perilp master, cci_m0 and debug access data memory) and 'perihp_nsp'(perihp master access data memory). The masters in main-interconnect does not access peri-interconnect.

The default setting of master NIUs are listing below:

Table 8-2 QoS Generator

Master NIU	Bandwidth (MB/s@MHz)	Priority0/1	Register Base Address	Valid Bandwidth Bits
cci_m0	100@600	2	0xffa50000	13
cci_m1	100@600	2	0xffad8000	13
debug	N/A	N/A	N/A	N/A
dmac0	100@300	1	0xffa64200	12
dmac1	100@300	1	0xffa64280	12
dcf	100@300	1	0xffa64180	11
crypto0	100@150	1	0xffa64100	11
crypto1	100@150	1	0xffa64080	11
pmu CM0	100@200	1	0xffa68000	11
peri CM0	100@150	1	0xffa64300	11
gic	100@200	1	0xffa78000	12
sdio	100@100	1	0xffa76000	11
sdmmc	100@150	1	0xffa74000	11
emmc	100@300	1	0xffa58000	12
pcie	1000@300	1	0xffa60080	13
hsic	100@150	1	0xffa60000	11
gmac	100@300	1	0xffa5c000	12
usb otg0	100@300	1	0xffa70000	12
usb otg1	100@300	1	0xffa70080	12
usb host0	100@150	1	0xffa60100	11
usb host1	100@150	1	0xffa60180	11
gpu	1000@500	1	0xffae0000	13
video m0	100@400	2	0xffab8000	12
video m1_r	150@400	2	0xffac0000	13
video m1_w	150@400	2	0xffac0080	12
rga_r	800@400	1	0xffab0000	13
rga_w	800@400	1	0xffab0080	12
iep	100@400	1	0xffa98000	12
vop-big_r	1000@400	3	0xffac8000	13
vop-big_w	1000@400	3	0xffac8080	13
vop-little	1000@400	3	0xffad0000	13
isp0_m0	100@400	3	0xffaa0000	12
isp0_m1	100@400	3	0xffaa0080	12
isp1_m0	100@400	3	0xffaa8000	12

Master NIU	Bandwidth (MB/s@MHz)	Priority0/1	Register Base Address	Valid Bandwidth Bits
isp1_m1	100@400	3	0xffaa8080	12
hdcp	100@400	3	0xffa90000	11
perihp_nsp	100@400	2	0xffad8080	13
perilp_nsp	100@400	2	0xffad8180	13
perilpslv_nsp	100@400	2	0xffad8100	11

Note:

- All master NIU QoS generator mode is 'Regulator' and saturation is 1024.
- The bandwidth must be calculated based on actual operating frequency and the frequency listed above may not be sign off frequency of each master.
- For video_m1, rga and vop-big, they have two QoS generators, one for read and the other one for write.
- For isp0 and isp1, they have two QoS generators each for their internal two masters.
- Refer to chapter Interconnect for detail register. All generators have the same register except the valid bits of 'Bandwidth' filed may be different.

8.3.2 Error detection, logging, and reporting

The interconnect hardware components can generate errors in particular circumstances:

- Generic master NIUs, when decoding addresses or applying security criteria.
- Generic or specific slave NIUs that are incapable of processing a particular master transaction.
- The slave IP itself, which can also return error responses to transactions.

These errors are stored in error logger. The error logger can also be programmed to generate interrupt when there is error happens.
In RK3399, there are 4 error loggers listed below:

Table 8-3 Error Logger

Error Logger	Path	Register Base Address
slv_err_logger0	All masters except pmu CM0 access all slaves pmu CM0 access all slaves outside pmu power domain	0xffa64000
slv_err_logger1	pmu CM0 access all slaves inside pmu power domain	0xffa68080
msch_err_logger0	All masters access memory schedule0	0xffa87c80
msch_err_logger1	All masters access memory schedule1	0xffa8fc80

Refer to chapter Interconnect for detail register.

8.3.3 Memory Scheduler

Memory scheduler is a special NIU of the interconnect, it mainly deal with the transaction inside the interconnect and convert it to the transaction which the ddr protocol controller can recognize.
Following table shows the software configurable setting for the memory scheduler when the system connected to different size of ddr device.
The DEVICE CONF is a configurable register inside interconnect.
R: indicates Row bits
B: indicates Bank bits
C: indicates Column bits
0: rank bit

Table 8-4 'ddrconf' item

DEVICE CONF	Item
0	00RRRRRRRRRRRRRRRRBBBCCCCCCC----
1	0RRRRRRRRRRRRRRRRBBBCCCCCCCC----
2	0RRRRRRRRRRRRRRRRBBBCCCCCCCCC----
3	0RRRRRRRRRRRRRRRRBBBCCCCCCCCCC----

DEVICE CONF	Item
4	0RRRRRRRRRRRRRRBBBCCRCCCCCC----
5	0RRRRRRRRRRRRRRBBBCCCRCCCCCC----
6	0RCRRRRRRRRRRRRRBBBCCCCCCCC----
7	0CRRRRRRRRRRRRRRBBBCCCCCCCC----

In order to get best performance, some DDR controller and DRAM related timing parameters must be programmed properly in memory schedule registers. The default DRAM timing is shown below. In RK3399，there are two same memory schedule to support two channel DDR system and each memory schedule has one memory schedule register(Base address for memory schedule 0 is 0xffa84000 and for memory schedule 1 is 0xffa8c000). Refer to chapter Interconnect for details.

Table 8-5 Default DRAM Timing(memory schecule 400MHz)

Parameter	Value	Parameter	Value
BurstSize	32	RdToWr	5 ns
ActToAct	55 ns	WrToRd	17.5 ns
Rrd	10 ns	WrToMaskedWrite	15 ns
Faw	10 ns	BusRdToRd	5 ns
FawBank	4	BusRdToWr	5 ns
RdToMiss	22.5 ns	BusWrToRd	5 ns
WrToMiss	50	BusWrToWr	5 ns
BurstPenalty	5 ns	ReadLatency	100 ns

8.3.4 Probe

The interconnect provides a service called probe to trace packet and compute traffic statics, There are totally 14 probes to monitor the memory schedule traffic statics and each can be programmed by their register. They are listed below.

Table 8-6 Probe

Probe Name	Monitor Path	Register Base Address
cci_probe_msch0	cci_m1 to memory schedule 0	0xffa86000
gpu_probe_msch0e	gpu to memory schedule 0	0xffa86400
perihp_probe_msch0	perihp master NIU to memory schedule 0	0xffa86800
perilp_probe_msch0	perilp master NIU,debug and cci_m0 to memory schedule 0	0xffa86c00
video_probe_msch0	video to memory schedule 0	0xffa87000
vio0_probe_msch0	iep,isp0 and vop-big to memory schedule 0	0xffa87400
vio1_probe_msch0	rga,isp1,vop-little and hdcp to memory schedule 0	0xffa87800
cci_probe_msch1	cci_m1 to memory schedule 1	0xffa8e000
gpu_probe_msch1	gpu to memory schedule 1	0xffa8e400
perihp_probe_msch1	perihp master NIU to memory schedule 1	0xffa8e800
perilp_probe_msch1	perilp master NIU,debug and cci_m0 to memory schedule 1	0xffa8ec00
video_probe_msch1	video to memory schedule 1	0xffa8f000
vio0_probe_msch1	iep,isp0 and vop-big to memory schedule 1	0xffa8f400
vio1_probe_msch1	rga,isp1,vop-little and hdcp to memory schedule 1	0xffa8f800

Refer to chapter 8.4 for detail register.

8.3.5 CCI500

The CCI-500 Cache Coherent Interconnect is an infrastructure component that supports the following features:

- Data coherency between ACE masters.
- Input and Output (IO) coherency with ACE-Lite masters.
- Crossbar interconnects functionality between the masters and up to six slaves.
- A snoop filter to reduce snoop power and improve performance for snoop misses.
- DVM message transport between masters for communication between MMUs.
- Quality of Service (QoS) features for shaping traffic profiles.
- A Performance Monitoring Unit (PMU) to count performance-related events.
- Support for ARM TrustZone® to provide Secure, Non-secure, and protected states.
- A Programmers View (PV) to control coherency and interconnect functionality.

Snoop filter

The CCI-500 contains an inclusive snoop filter that records the addresses of data stored in the ACE master caches. This means that the filter can respond to the snoop in the case of a miss, and snoop appropriate masters only in the case of a hit. Snoop filter entries are maintained by observing transactions from ACE masters to determine when entries have to be allocated and de-allocated.

The snoop filter can respond to many of the coherency requests without it being necessary to broadcast to all ACE interfaces. For example, if the address is not in any cache, the snoop filter responds with a miss and directs the request to memory. If the address is in a processor cache, then it is considered to be a hit and the snoop is directed to the appropriate ACE port containing that address in its cache.

The snoop filter is 8-way set associative and is usually configured to contain between 1.5 and 2 times the number of tags in the attached processor caches. In the case of a way conflict, the existing entry is evicted, and the snoop filter issues a CleanInvalid snoop to the processors that might be holding the evicted lines. This is known as a back-invalidation, and is expected to be a rare occurrence if you configure the snoop filter size as ARM recommends.

The snoop filter is updated by monitoring transactions from the attached masters, which allocate and de-allocate data into their caches. In the ACE protocol, the de-allocation of clean data is indicated using the Evict transaction. You must ensure that masters connected to the CCI-500 issue Evict transactions when they de-allocate clean data. For ARM processors, you can control the issuing of Evict transactions using bit[3] of the L2 Auxiliary Control Register.

Snoop connectivity and control

The CCI-500 has a fully-connected snoop interconnect and a snoop filter for efficient management of snoop request transactions.

You can control whether each interface is enabled for snoop requests and DVM message requests using Snoop Control Registers.

A shareable read request from an ACE master, that allocates data to the cache of the master, also allocates an entry in the snoop filter to record that the master has a copy of that data. For requests for which it might be necessary to retrieve or invalidate data in the cache of another master, the CCI-500 looks up the address in the snoop filter. If the snoop filter indicates that a master has a copy of that data, then either:

- A snoop request is issued, if snoops to the master are enabled.
- The snoop filter entry is updated, if snoops to the master are disabled.

If the snoop filter indicates that no ACE master contains that address, then the request is directed to the appropriate master interface. DVM requests are broadcast through all slave interfaces that are enabled for DVM messages and do not interact with the snoop filter.

The programmable bits of the Snoop Control Registers are LOW at reset. You must program them HIGH for each master in the shareable domain before the CCI-500 receives shareable transactions or DVM messages. Before disabling a master, you must disable snoop and DVM messages for the master by programming the relevant bits of the Snoop Control Registers LOW.

If snoops are sent to interfaces where the master is disabled or not present, the system is likely to deadlock. A hardware mechanism of disabling snoops is provided to prevent software errors causing deadlocks in cases where masters are not present or do not support DVMs. Each slave interface has an ACCHANNELENSx signal input that controls whether snoops and DVM messages can be issued from that interface. This input overrides any programmable settings.

Cache maintenance operations

The CCI-500 supports snooping of cache-maintenance operations based on the Snoop Control Register.
You can use snooping and cache maintenance to manage Level 1 and Level 2 caches within the same domain as the CCI-500. The CCI-500 does not support the propagation of cache maintenance operations downstream of its master interfaces.

QoS value as a priority indicator

The CCI-500 uses the QoS value as a priority indicator for arbitration of requests. The QoS value can be from an input to a slave interface, or it can be overwritten by a programmed value.
The CCI-500 uses the QoS value when selecting the request to admit into the main transaction queue. Requests with the highest QoS have the highest priority unless an anti-starvation mechanism is activated.
The CCI-500 uses a Least Recently Granted (LRG) scheme when two or more transactions share the highest priority. The arbiter has starvation avoidance mechanisms to prevent high bandwidth requests from stalling lower priority requests indefinitely.
The CCI-500 propagates QoS values. This determines the service rates when downstream interconnect and slave devices are sensitive to the QoS value. The NIC-400 Network Interconnect is sensitive to the QoS value.
You can override the ARQOS and AWQOS input signals from each slave interface by using a programmable register. The value from this register is only applied if the relevant static input signal, QOSOVERRIDE[6:0], is HIGH. CCI-500-generated transactions use the QoS value of the trigger transaction or the override value if the QOSOVERRIDE signal is set

8.4 Register Description

8.4.1 QoS Registers Summary

Name	Offset	Size	Reset Value	Description
QOS_Id_CoreId	0x0000	W	0x0d867004	Core ID register
QOS_Id_RevisionId	0x0004	W	0x0001aa00	Revision ID register
QOS_Priority	0x0008	W	0x80000005	Priority register
QOS_Mode	0x000c	W	0x00000003	Mode register
QOS_Bandwidth	0x0010	W	0x0000018a	Bandwidth register
QOS_Saturation	0x0014	W	0x00000040	Saturation register
QOS_ExtControl	0x0018	W	0x00000000	External inputs control

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

8.4.2 QoS Detail Register Description

QOS_Id_CoreId
Address: Operational Base + offset (0x0000)
Core ID register

Bit	Attr	Reset Value	Description
31:8	RO	0x0d8670	CoreChecksum Field containing a checksum of the parameters of the IP.
7:0	RO	0x04	CoreTypeId Field identifying the type of IP.

QOS_Id_RevisionId
Address: Operational Base + offset (0x0004)
Revision ID register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RO	0x0001aa00	RevisionId Constant.

QOS_Priority
Address: Operational Base + offset (0x0008)
Priority register

Bit	Attr	Reset Value	Description
31	RO	0x1	Mark Backward compatibility marker when 0.
30:4	RO	0x0	reserved
3:2	RW	0x1	P1 In Programmable or Bandwidth Limiter mode, the priority level for read transactions. In Bandwidth regulator mode, the priority level when the used throughput is below the threshold. In Bandwidth Regulator mode, P1 should have a value equal or greater than P0.
1:0	RW	0x1	P0 In Programmable or Bandwidth Limiter mode, the priority level for write transactions. In Bandwidth Regulator mode, the priority level when the used throughput is above the threshold. In Bandwidth Regulator mode, P0 should have a value equal or lower than P1.

QOS_Mode
Address: Operational Base + offset (0x000c)
Mode register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1:0	RW	0x3	Mode 0 = Programmable mode: a programmed priority is assigned to each read or write, 1 = Bandwidth Limiter Mode: a hard limit restricts throughput, 2 = Bypass mode: (<See SoC-specific QoS generator documentation>), 3 = Bandwidth Regulator mode: priority decreases when throughput exceeds a threshold.

QOS_Bandwidth
Address: Operational Base + offset (0x0010)
Bandwidth register

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved

Bit	Attr	Reset Value	Description
11:0	RW	0x18a	Bandwidth Field0000 Abstract In Bandwidth Limiter or Bandwidth Regulator mode, the bandwidth threshold in units of 1/256th bytes per cycle. For example, 80 MBps on a 250 MHz interface is value 0x0052. The valid bits may be different for different master NIU.

QOS_Saturation
Address: Operational Base + offset (0x0014)
Saturation register

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RW	0x040	Saturation In Bandwidth Limiter or Bandwidth Regulator mode, the maximum data count value, in units of 16 bytes. This determines the window of time over which bandwidth is measured. For example, to measure bandwidth within a 1000 cycle window on a 64-bit interface is value 0x1F4.

QOS_ExtControl
Address: Operational Base + offset (0x0018)
External inputs control

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2	RW	0x0	IntClkEn n/a
1	RW	0x0	ExtThrEn n/a
0	RW	0x0	SocketQosEn n/a

8.4.3 Error Logger Registers Summary

slv_err_logger0/ slv_err_logger0:

Name	Offset	Size	Reset Value	Description
ERRLOG_Id_CoreId	0x0000	W	0x0000000d	Contain CoreTypeId and CoreChecksum
ERRLOG_Id_RevisionId	0x0004	W	0x00000000	IP Revision ID
ERRLOG_FaultEn	0x0008	W	0x00000000	Error interrupt enable
ERRLOG_ErrVld	0x000c	W	0x00000000	Error staus register
ERRLOG_ErrClr	0x0010	W	0x00000000	Error interrupt status clear register
ERRLOG_ErrLog0	0x0014	W	0x80000000	Transport protocol header information register
ERRLOG_ErrLog1	0x0018	W	0x00000000	Route ID register
ERRLOG_ErrLog3	0x0020	W	0x00000000	Address register

Name	Offset	Size	Reset Value	Description
ERRLOG_ErrLog5	0x0028	W	0x00000000	LSB user bits in transport protocol header
ERRLOG_ErrLog6	0x002c	W	0x00000000	MSB user bits in transport protocol header
ERRLOG_ErrLog7	0x0030	W	0x00000000	Securrity flag in transport protocol header
ERRLOG_StallEn	0x0038	W	0x00000000	Error logger mode selection

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

msch_err_logger0/msch_err_logger1

Name	Offset	Size	Reset Value	Description
ERRLOG_Id_CoreId	0x0000	W	0xbb25140d	This may be different for each error logger.
ERRLOG_Id_RevisionId	0x0004	W	0x0001aa00	It is the same for each error logger.
ERRLOG_FaultEn	0x0008	W	0x00000000	Error interrupt enable
ERRLOG_ErrVld	0x000c	W	0x00000000	Error staus register
ERRLOG_ErrClr	0x0010	W	0x00000000	Error interrupt status clear register
ERRLOG_ErrLog0	0x0014	W	0x80000000	Transport protocol header information register
ERRLOG_ErrLog1	0x0018	W	0x00000000	Route ID register
ERRLOG_ErrLog3	0x0020	W	0x00000000	Address register
ERRLOG_ErrLog5	0x0028	W	0x00000000	User bits in transport protocol header
ERRLOG_ErrLog7	0x0030	W	0x00000000	Securrity flag in transport protocol header
ERRLOG_StallEn	0x0038	W	0x00000000	Error logger mode selection

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

8.4.4 Error Logger Detail Register Description

slv_err_logger0/ slv_err_logger0:
ERRLOG_Id_CoreId
Address: Operational Base + offset (0x0000)
Contain CoreTypeId and CoreChecksum

Bit	Attr	Reset Value	Description
31:8	RO	0x000000	CoreChecksum Field containing a checksum of the parameters of the IP. For slv_err_logger0, this filed's value is always 0x43F8FA. For slv_err_logger1, this filed's value is always 0xB5413E.
7:0	RO	0x0d	CoreTypeId Field identifying the type of IP. It is the same for both slv_err_logger0 and slv_err_logger1.

ERRLOG_Id_RevisionId
Address: Operational Base + offset (0x0004)
IP Revision ID

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RO	0x0001aa00	RevisionId Constant.

ERRLOG_FaultEn
Address: Operational Base + offset (0x0008)
Error interrupt enable

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	FaultEn When set to 1, enables error reporting output signal Fault. Fault is asserted when register ErrVld is set to 1, and driven to 0 when FaultEn is cleared to 0.

ERRLOG_ErrVld
Address: Operational Base + offset (0x000c)
Error staus register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RO	0x0	ErrVld When set to 1, indicates that an error is logged in the ErrLog registers.

ERRLOG_ErrClr
Address: Operational Base + offset (0x0010)
Error interrupt status clear register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	ErrClr When set to 1, clears register ErrVld. Reading ErrClr always returns 0.

ERRLOG_ErrLog0
Address: Operational Base + offset (0x0014)
Transport protocol header information register

Bit	Attr	Reset Value	Description
31	RO	0x1	Format Always 1.
30:28	RO	0x0	reserved
27:16	RO	0x000	Len1 Contains packet header field Len1
15:11	RO	0x0	reserved
10:8	RO	0x0	ErrCode Contains packet header field ErrCode if the field exists, otherwise 0.
7:5	RO	0x0	reserved

Bit	Attr	Reset Value	Description
4:1	RO	0x0	Opc Contains packet header field Opc.
0	RO	0x0	Lock Contains packet header bit Lock.

ERRLOG_ErrLog1
Address: Operational Base + offset (0x0018)
Route ID register

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:0	RO	0x00000	ErrLog1 Contains transport protocol packet header field RouteID of the logged error. Unused bits are read as 0.

ERRLOG_ErrLog3
Address: Operational Base + offset (0x0020)
Address register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ErrLog3 Contains transport protocol packet header field Addr of the logged error. Unused bits are read as 0.

ERRLOG_ErrLog5
Address: Operational Base + offset (0x0028)
LSB user bits in transport protocol header

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	ReqUserL Low 16 LSB AXI user bits for cci_m0 and pcie master. It is read as 0 for the other master.Unused bits are read as 0.
15:10	RO	0x00	Mid Master ID Master ID for each master.
9:0	RO	0x000	AxiId AXI ID for AXI master. It is read as 0 for AHB Master. Unused bits are read as 0.

ERRLOG_ErrLog6
Address: Operational Base + offset (0x002c)
MSB user bits in transport protocol header

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RO	0x00	ReqUserH High 8 LSB AXI user bits for cci_m0 and pcie master. It is read as 0 for the other master.Unused bits are read as 0.

ERRLOG_ErrLog7
Address: Operational Base + offset (0x0030)
Securrity flag in transport protocol header

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RO	0x0	ErrLog7 Contains transport protocol packet header field Security of the logged error.

ERRLOG_StallEn
Address: Operational Base + offset (0x0038)
Error logger mode selection

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	StallEn When set to 1, enables stall mode. When set to 0, only the first error packet is stored in the error logger.

msch_err_logger0/msch_err_logger1
ERRLOG_Id_CoreId
Address: Operational Base + offset (0x0000)
This may be different for each error logger.

Bit	Attr	Reset Value	Description
31:8	RO	0xbb2514	CoreChecksum Field containing a checksum of the parameters of the IP.
7:0	RO	0x0d	CoreTypeId Field identifying the type of IP. It is the same for bothe msch_err_logger0 and msch_err_logger1.

ERRLOG_Id_RevisionId
Address: Operational Base + offset (0x0004)
It is the same for each error logger.

Bit	Attr	Reset Value	Description
31:0	RO	0x0001aa00	RevisionId Constant.

ERRLOG_FaultEn
Address: Operational Base + offset (0x0008)
Error interrupt enable

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	FaultEn When set to 1, enables error reporting output signal Fault. Fault is asserted when register ErrVld is set to 1, and driven to 0 when FaultEn is cleared to 0.

ERRLOG_ErrVld
Address: Operational Base + offset (0x000c)
Error staus register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RO	0x0	ErrVld When set to 1, indicates that an error is logged in the ErrLog registers.

ERRLOG_ErrClr
Address: Operational Base + offset (0x0010)
Error interrupt status clear register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	ErrClr When set to 1, clears register ErrVld. Reading ErrClr always returns 0.

ERRLOG_ErrLog0
Address: Operational Base + offset (0x0014)
Transport protocol header information register

Bit	Attr	Reset Value	Description
31	RO	0x1	Format Always 1.
30:28	RO	0x0	reserved
27:16	RO	0x000	Len1 Contains packet header field Len1
15:11	RO	0x0	reserved
10:8	RO	0x0	ErrCode Contains packet header field ErrCode if the field exists, otherwise 0.
7:5	RO	0x0	reserved
4:1	RO	0x0	Opc Contains packet header field Opc.
0	RO	0x0	Lock Contains packet header bit Lock.

ERRLOG_ErrLog1
Address: Operational Base + offset (0x0018)
Route ID register

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21:0	RO	0x000000	ErrLog1 Contains transport protocol packet header field RouteID of the logged error. Unused bits are read as 0.

ERRLOG_ErrLog3
Address: Operational Base + offset (0x0020)
Address register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ErrLog3 Contains up to 32 LSBs of transport protocol packet header field Addr of the logged error. Unused bits are read as 0.

ERRLOG_ErrLog5
Address: Operational Base + offset (0x0028)
User bits in transport protocol header

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:10	RO	0x00	Mid Master ID Master ID for each master.
9:0	RO	0x000	AxiId AXI ID for AXI master. It is read as 0 for AHB Master. Unused bits are read as 0.

ERRLOG_ErrLog7
Address: Operational Base + offset (0x0030)
Securrity flag in transport protocol header

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RO	0x0	ErrLog7 Contains transport protocol packet header field Security of the logged error.

ERRLOG_StallEn
Address: Operational Base + offset (0x0038)
Error logger mode selection

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	StallEn When set to 1, enables stall mode. When set to 0, only the first error packet is stored in the error logger.

8.4.5 Memory Schedule Registers Summary

Name	Offset	Size	Reset Value	Description
MSCH_Id_CoreId	0x0000	W	0x0d867004	Core ID register
MSCH_Id_RevisionId	0x0004	W	0x0001aa00	Revision ID register
MSCH_DeviceConf	0x0008	W	0x00000000	ddr configuration pointers
MSCH_DeviceSize	0x000c	W	0x00000000	ddr configuration sizes.

Name	Offset	Size	Reset Value	Description
MSCH_DdrTimingA0	0x0010	W	0x28140916	DdrTimingA bank 0
MSCH_DdrTimingB0	0x0014	W	0x00040702	DdrTimingB bank 0
MSCH_DdrTimingC0	0x0018	W	0x00000002	DdrTimingC bank 0
MSCH_DevToDev0	0x001c	W	0x00000222	Timing values concerning device to device data bus ownership c
MSCH_DdrMode	0x0110	W	0x0000004c	ddr mode definition.
MSCH_AgingX0	0x1000	W	0x00000000	Aging threshold multiplicator.

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*
Base address for memory schedule 0 is 0xffa84000 and for memory schedule 1 is 0xffa8c0000.

8.4.6 Memory schedule Detail Register Description

MSCH_Id_CoreId
Address: Operational Base + offset (0x0000)
Core ID register

Bit	Attr	Reset Value	Description
31:8	RO	0x00dc1b	CoreChecksum Field containing a checksum of the parameters of the IP. For memory schedule 0 , this value is 0x00dc1b For memory schedule 1 , this value is 0xc2f11d
7:0	RO	0x18	CoreTypeId Field identifying the type of IP.

MSCH_Id_RevisionId
Address: Operational Base + offset (0x0004)
Revision ID register

Bit	Attr	Reset Value	Description
31:0	RO	0x0001aa00	RevisionId Constant.

MSCH_DeviceConf
Address: Operational Base + offset (0x0008)
ddr configuration pointers

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:6	RW	0x00	Rank1 Rank1 selector of predefined ddrConf configuration
5:0	RW	0x00	Rank0 Rank0 selector of predefined ddrConf configuration

MSCH_DeviceSize
Address: Operational Base + offset (0x000c)
ddr configuration sizes.

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved

Bit	Attr	Reset Value	Description
15:8	RW	0x00	Rank1 Rank0 size.
7:0	RW	0x00	Rank0 Rank0 size.

MSCH_DdrTimingA0
Address: Operational Base + offset (0x0010)
DdrTimingA bank 0

Bit	Attr	Reset Value	Description
31:24	RW	0x28	ReadLatency Maximun delay between a read request and the first data response.
23:22	RO	0x0	reserved
21:16	RW	0x14	WrToMiss Minimum number of scheduler clock cycles between the last DRAM Write command and a new Read or Write command in another page of the same bank. The field must be set to the following value, rounded to an integer number of scheduler clock cycles: (WL ×tCkD + tWR + tRP + tRCD) / tCkG
15:14	RO	0x0	reserved
13:8	RW	0x09	RdToMiss Minimum number of scheduler clock cycles between the last DRAM Read command and a new Read or Write command in another page of the same bank. The field must be set to the following value, rounded to an integer number of scheduler clock cycles: (tRTP + tRP + tRCD –BL ×tCkD / 2) / tCkG
7:6	RO	0x0	reserved
5:0	RW	0x16	ActToAct Minimum number of scheduler clock cycles between two consecutive DRAM Activate commands on the same bank. The field must be set to the following value, rounded to an integer number of scheduler clock cycles: tRC / tCkG

MSCH_DdrTimingB0
Address: Operational Base + offset (0x0014)
DdrTimingB bank 0

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

Bit	Attr	Reset Value	Description
29:24	RW	0x12	Faw Field0000 Abstract Number of cycle of the FAW period. The field must be set to the following value, rounded to an integer number of scheduler clock cycles: tFAW / tCkG
23:20	RO	0x0	reserved
19:16	RW	0x4	Rrd Number of cycle between two consecutive Activate commands on different Banks of the same device. The field must be set to the following value, rounded to an integer number of scheduler clock cycles: tRRD / tCkG
15:13	RO	0x0	reserved
12:8	RW	0x07	WrToRd Minimum number of scheduler clock cycles between the last DRAM Write command and a Read command. The field must be set to the following value, rounded to an integer of scheduler clock cycles: (WL ×tCkD + tWTR) / tCkG, for DDR2 and DDR3 memories. (WL ×tCkD + tWTR_S) / tCkG, for DDR4 memories. ((WL + 1) ×tCkD + tWTR) / tCkG, for LPDDR4 memories.
7:5	RO	0x0	reserved
4:0	RW	0x02	RdToWr Minimum number of scheduler clock cycles between the last DRAM Read command and a Write command. The field must be set to the following value, rounded to an integer number of scheduler clock cycles: 2 ×tCkD / tCkG, for DDR2 memories. (RL –WL + 2) ×tCkD / tCKG, for DDR3 and DDR4 memories. (RL + RoundUp(tDQSCK(max) / tCKD) + tRPST - WL + tWPRE) ×tCkD / tCKG , for LPDDR4 memories.

MSCH_DdrTimingC0

Address: Operational Base + offset (0x0018)

DdrTimingC bank 0

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13:8	RW	0x06	WrToMwr Number of scheduler clock cycles between the last write data to the first data of a masked write command on the same bank. This field must be set to 3xBurstPenalty, and must be set to zero for the other DRAM.
7:4	RO	0x0	reserved

Bit	Attr	Reset Value	Description
3:0	RW	0x2	BurstPenalty DRAM burst duration on the DRAM data bus in scheduler clock cycles. The field must be set to Nd /Ns, where: Nd is the number of DRAM cycles needed to process a DRAM burst of determined size, expressed in bytes. Ns is the minimum number of scheduler cycles to process a DRAM burst of the same size.

MSCH_DevToDev0
Address: Operational Base + offset (0x001c)
Timing values concerning device to device data bus ownership c

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved
14:12	RW	0x2	BusWrToWr number of cycle between the last write data to a device and the first write data of another device. The field must be set according to the third-party DDR controller specification.
11	RO	0x0	reserved
10:8	RW	0x2	BusWrToRd number of cycle between the last write data to a device and the first read data of another device. The field must be set according to the third-party DDR controller specification.
7	RO	0x0	reserved
6:4	RW	0x2	BusRdToWr number of cycle between the last read data of a device and the first write data to another device. The field must be set according to the third-party DDR controller specification.
3	RO	0x0	reserved
2:0	RW	0x2	BusRdToRd number of cycle between the last read data of a device and the first read data of another device. The field must be set according to the third-party DDR controller specification.

MSCH_DdrMode
Address: Operational Base + offset (0x0110)
ddr mode definition.

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RO	0x00	ForceOrderState ForceOrderState

Bit	Attr	Reset Value	Description
15:8	RW	0x00	ForceOrder When bit n of register field ForceOrder is set to 1, DRAM commands are executed in the order they arrive at scheduler port n. When field bits are set to 1, and BypassFiltering is also set to 1, command execution order is guaranteed for the corresponding scheduler port.
7	RO	0x0	reserved
6:5	RW	0x2	MwrSize Register MwrSize sets LPDDR4 data width, which is used for masked-write split control. The field must be set to non-zero for LPDDR3 memories. 2'b00: Reserved 2'b01: LPDDR4, 16 bits. 2'b10: LPDDR4, 32 bits. 2'b11: LPDDR4, 32 bits.
4:3	RW	0x1	BurstSize Register field BurstSize sets the DDR burst size, in bytes, as shown by the following table. 2'b00:16 2'b01:32 2'b10:64 2'b11:128 NOTE: For LPDDR4 memories, the field must be set to the number of bytes required by BL16 transactions.
2	RW	0x1	FawBank Register field FawBank indicates the number of banks of a given device involved in the FAW period during which four banks can be active. It must be set to 0 for 2-bank memories, and 1 for memories with four banks or more.
1	RW	0x0	BypassFiltering When register field BypassFiltering is set to 1, arbiter filters are bypassed and timing register outputs are internally set to an idle value.The field can be useful during DRAM initialization, when training or calibration sequences are performed, and scheduler arbitration is not needed. When the field is set to 0, scheduler arbitration is fully functional, this is the functional usage mode. NOTE: When the field is set to 1, the final arbitration level continues to elect transactions among those presented to the arbiter. Set field ForceOrder to ensure that transactions are executed in order, for instance during DRAM initialization.

Bit	Attr	Reset Value	Description
0	RW	0x0	AutoPrecharge When set to one, pages are automatically closed after each access, when set to zero, pages are left opened until an access in a different page occurs

MSCH_AgingX0
Address: Operational Base + offset (0x1000)
Aging threshold multiplicator.

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2:0	RW	0x4	AgingX0 Aging threshold multiplicator.

8.4.7 Probe Registers Summary

Name	Offset	Size	Reset Value	Description
PROBE_Id_CoreId	0x0000	W	0x0d867006	Core ID register
PROBE_Id_RevisionId	0x0004	W	0x0001aa00	Revision ID register
PROBE_MainCtl	0x0008	W	0x00000000	Register MainCtl contains probe global control bits.
PROBE_CfgCtl	0x000c	W	0x00000000	Register CfgCtl contains global enable and active bits.
PROBE_StatPeriod	0x0024	W	0x00000000	Statistics Period
PROBE_StatGo	0x0028	W	0x00000000	Statistics start to dump
PROBE_Counters_0_Src	0x0138	W	0x00000000	Register CntSrc indicates the event source.
PROBE_Counters_0_Val	0x013c	W	0x00000000	Registers Counters_M_Val contain the statistics counter values.
PROBE_Counters_1_Src	0x014c	W	0x00000000	Register CntSrc indicates the event source.
PROBE_Counters_1_Val	0x0150	W	0x00000000	Registers Counters_M_Val contain the statistics counter values.
PROBE_Counters_2_Src	0x0160	W	0x00000000	Register CntSrc indicates the event source.
PROBE_Counters_2_Val	0x0164	W	0x00000000	Registers Counters_M_Val contain the statistics counter values.
PROBE_Counters_3_Src	0x0174	W	0x00000000	Register CntSrc indicates the event source.
PROBE_Counters_3_Val	0x0178	W	0x00000000	Registers Counters_M_Val contain the statistics counter values.

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

8.4.8 Probe Detail Register Description

PROBE_Id_CoreId
Address: Operational Base + offset (0x0000)
Core ID register

Bit	Attr	Reset Value	Description
31:8	RO	0x0d8670	CoreChecksum Field containing a checksum of the parameters of the IP.
7:0	RO	0x06	CoreTypeId Field identifying the type of IP.

PROBE_Id_RevisionId
Address: Operational Base + offset (0x0004)
Revision ID register

Bit	Attr	Reset Value	Description
31:0	RO	0x0001aa00	RevisionId Constant.

PROBE_MainCtl
Address: Operational Base + offset (0x0008)
Register MainCtl contains probe global control bits.

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RW	0x0	FiltByteAlwaysChainableEn When set to 0, filters are mapped to all statistic counters when counting bytes or enabled bytes. Therefore, only filter events mapped to even counters can be counted using a pair of chained counters.When set to 1, filters are mapped only to even statistic counters when counting bytes or enabled bytes. Thus events from any filter can be counted using a pair of chained counters.
6	RO	0x0	IntrusiveMode When set to 1, register field IntrusiveMode enables trace operation in Intrusive flow-control mode. When set to 0, the register enables trace operation in Overflow flow-control mode
5	RW	0x0	StatCondDump When set, register field StatCondDump enables the dump of a statistics frame to the range of counter values set for registers StatAlarmMin, StatAlarmMax, and AlarmMode. This field also renders register StatAlarmStatus inoperative. When parameter statisticsCounterAlarm is set to False, the StatCondDump register bit is reserved.
4	RW	0x0	Reserved
3	RW	0x0	StatEn When set to 1, register field StatEn enables statistics profiling. The probe sendS statistics results to the output for signal ObsTx. All statistics counters are cleared when the StatEn bit goes from 0 to 1. When set to 0, counters are disabled.
2	RW	0x0	PayloadEn Register field PayloadEn, when set to 1, enables traces to contain headers and payload. When set ot 0, only headers are reported.
1	RO	0x0	TraceEn Register field TraceEn enables the probe to send filtered packets (Trace) on the ObsTx observation output.

Bit	Attr	Reset Value	Description
0	RW	0x0	ErrEn Register field ErrEn enables the probe to send on the ObsTx output any packet with Error status, independently of filtering mechanisms, thus constituting a simple supplementary global filter.

PROBE_CfgCtl
Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RO	0x0	Active Register field Active is used to inform software that the probe is active. Probe configuration is not allowed during the active state. This bit is raised when bit GlobalEn is set, and is cleared a few cycles after setting GlobalEn to zero (probe is Idle).
0	RW	0x0	GlobalEn Set register field GlobalEn to 1 enable the tracing and statistics collection sub-systems of the packet probe.

PROBE_StatPeriod
Address: Operational Base + offset (0x0024)
Statistics Period

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x00	StatPeriod Register StatPeriod is a 5-bit register that sets a period, within a range of 2 cycles to 2 gigacycles, during which statistics are collected before being dumped automatically. Setting the register implicitly enables automatic mode operation for statistics collection. The period is calculated with the formula: N_Cycle = 2**StatPeriodWhen register StatPeriod is set to its default value 0, automatic dump mode is disabled, and register StatGo is activated for manual mode operation. Note: When parameter statisticsCollection is set to False, StatPeriod is reserved.

PROBE_StatGo
Address: Operational Base + offset (0x0028)
Statistics start to dump

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	StatGo Writing a 1 to the 1-bit pulse register StatGo generates a statistics dump.The register is active when statistics collection operates in manual mode, that is, when register StatPeriod is set to 0.NOTE The written value is not stored in StatGo. A read always returns 0.

PROBE_Counters_0_Src

Address: Operational Base + offset (0x0138)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x00	IntEvent Internal packet event 5'h00 OFF Counter disabled. 5'h01 CYCLE8 Probe clock cycles. 5'h02 IDLE Idle cycles during which no packet data is observed. 5'h03 XFER Transfer cycles during which packet data is transferred. 5'h04 BUSY Busy cycles during which the packet data is made available by the transmitting agent but the receiving agent is not ready to receive it. 5'h05 WAIT Wait cycles during a packet in which the transmitting agent suspends the transfer of packet data. 5'h06 PKT Packets. 5'h08 BYTE Total number of payload bytes. 5'h09 PRESS Clock cycles with pressure level > 0. 5'h0A PRESS Clock cycles with pressure level > 1. 5'h0B PRESS Clock cycles with pressure level > 2. 5'h10 CHAIN Carry from counter 2m to counter 2m + 1.

PROBE_Counters_0_Val
Address: Operational Base + offset (0x013c)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RO	0x0000	Counters_0_Val Register Val is a read-only register that is always present. The register containsthe statistics counter value either pending StatAlarm output, or when statisticscollection is suspended subsequent to triggers or signal statSuspend.

PROBE_Counters_1_Src
Address: Operational Base + offset (0x014c)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved

Bit	Attr	Reset Value	Description
4:0	RW	0x00	IntEvent Internal packet event Event | source type | Event description 5'h00 OFF Counter disabled. 5'h01 CYCLE8 Probe clock cycles. 5'h02 IDLE Idle cycles during which no packet data is observed. 5'h03 XFER Transfer cycles during which packet data is transferred. 5'h04 BUSY Busy cycles during which the packet data is made available by the transmitting agent but the receiving agent is not ready to receive it. 5'h05 WAIT Wait cycles during a packet in which the transmitting agent suspends the transfer of packet data. 5'h06 PKT Packets. 5'h08 BYTE Total number of payload bytes. 5'h09 PRESS Clock cycles with pressure level > 0. 5'h0A PRESS Clock cycles with pressure level > 1. 5'h0B PRESS Clock cycles with pressure level > 2. 5'h10 CHAIN Carry from counter 2m to counter 2m + 1.

PROBE_Counters_1_Val
Address: Operational Base + offset (0x0150)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RO	0x0000	Counters_0_Val Register Val is a read-only register that is always present. The register containsthe statistics counter value either pending StatAlarm output, or when statisticscollection is suspended subsequent to triggers or signal statSuspend.

PROBE_Counters_2_Src
Address: Operational Base + offset (0x0160)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved

Bit	Attr	Reset Value	Description
4:0	RW	0x00	IntEvent Internal packet event Event | source type | Event description 5'h00 OFF Counter disabled. 5'h01 CYCLE8 Probe clock cycles. 5'h02 IDLE Idle cycles during which no packet data is observed. 5'h03 XFER Transfer cycles during which packet data is transferred. 5'h04 BUSY Busy cycles during which the packet data is made available by the transmitting agent but the receiving agent is not ready to receive it. 5'h05 WAIT Wait cycles during a packet in which the transmitting agent suspends the transfer of packet data. 5'h06 PKT Packets. 5'h08 BYTE Total number of payload bytes. 5'h09 PRESS Clock cycles with pressure level > 0. 5'h0A PRESS Clock cycles with pressure level > 1. 5'h0B PRESS Clock cycles with pressure level > 2. 5'h10 CHAIN Carry from counter 2m to counter 2m + 1.

PROBE_Counters_2_Val
Address: Operational Base + offset (0x0164)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RO	0x0000	Counters_0_Val Register Val is a read-only register that is always present. The register containsthe statistics counter value either pending StatAlarm output, or when statisticscollection is suspended subsequent to triggers or signal statSuspend.

PROBE_Counters_3_Src
Address: Operational Base + offset (0x0174)

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved

Bit	Attr	Reset Value	Description
4:0	RW	0x00	IntEvent Internal packet event Event | source type | Event description 5'h00 OFF Counter disabled. 5'h01 CYCLE8 Probe clock cycles. 5'h02 IDLE Idle cycles during which no packet data is observed. 5'h03 XFER Transfer cycles during which packet data is transferred. 5'h04 BUSY Busy cycles during which the packet data is made available by the transmitting agent but the receiving agent is not ready to receive it. 5'h05 WAIT Wait cycles during a packet in which the transmitting agent suspends the transfer of packet data. 5'h06 PKT Packets. 5'h08 BYTE Total number of payload bytes. 5'h09 PRESS Clock cycles with pressure level > 0. 5'h0A PRESS Clock cycles with pressure level > 1. 5'h0B PRESS Clock cycles with pressure level > 2. 5'h10 CHAIN Carry from counter 2m to counter 2m + 1.

PROBE_Counters_3_Val
Address: Operational Base + offset (0x0178)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RO	0x0000	Counters_0_Val Register Val is a read-only register that is always present. The register contains the statistics counter value either pending StatAlarm output, or when statistics collection is suspended subsequent to triggers or signal statSuspend.

8.4.9 CCI500 Registers Summary

Name	Offset	Size	Reset Value	Description
CCI500_SYS_CTRL	0x00000	W	0x00000000	Control Override Register
CCI500_SECURE_CTRL	0x00008	W	0x00000000	Secure Access Register
CCI500_STATUS	0x0000c	W	0x00000000	Status Register
CCI500_ERROR_STATUS	0x00010	W	0x00000000	Imprecise Error Register
CCI500_PFMMON_CTRL	0x00100	W	0x00000000	Performance Monitor Control Register (PMCR)
CCI500_INTERFACE_MONITOR_CTRL	0x00104	W	0x00000000	Snoop Control Register for slave interface x
CCI500_SNOOP_CTRL_S0	0x01000	W	0x00000000	
CCI500_SHAREABLE_OVERRIDE_S0	0x01004	W	0x00000000	Shareable Override Register

Name	Offset	Size	Reset Value	Description
CCI500_RD_CHAN_QOS_OVERRIDE_S0	0x01100	W	0x00000000	Read Channel QoS Value Override Register for slave interface x
CCI500_WR_CHAN_QOS_OVERRIDE_S0	0x01104	W	0x00000000	Write Channel QoS Value Override slave interface x
CCI500_MAX_OT_S0	0x01110	W	0x00000000	Maximum Outstanding Transactions Registers
CCI500_SNOOP_CTRL_S1	0x02000	W	0x00000000	
CCI500_SHAREABLE_OVERRIDE_S1	0x02004	W	0x00000000	Shareable Override Register
CCI500_RD_CHAN_QOS_OVERRIDE_S1	0x02100	W	0x00000000	Read Channel QoS Value Override Register for slave interface x
CCI500_WR_CHAN_QOS_OVERRIDE_S1	0x02104	W	0x00000000	Write Channel QoS Value Override slave interface x
CCI500_MAX_OT_S1	0x02110	W	0x00000000	Maximum Outstanding Transactions Registers
CCI500_SLAVE_INTERFACE_MONITOR_S0	0x90000	W	0x00000000	Slave Interface Monitor Registers
CCI500_SLAVE_INTERFACE_MONITOR_S1	0x90004	W	0x00000000	Slave Interface Monitor Registers
CCI500_MASTER_INTERFACE_MONITOR_M0	0x90100	W	0x00000000	Master Interface Monitor Registers
CCI500_MASTER_INTERFACE_MONITOR_M1	0x90104	W	0x00000000	Master Interface Monitor Registers

*Notes: Size : **B** - Byte (8 bits) access, **HW** - Half WORD (16 bits) access, **W** -WORD (32 bits) access*

8.4.10 CCI500 Detail Register Description

CCI500_SYS_CTRL

Address: Operational Base + offset (0x00000)

Control Override Register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	RW	0x0	Disable_Clock_Gating Disable regional clock gating 0: Regional clock gating operates in the CCI-500 1: Disables regional clock gating in the CCI-500
2	RW	0x0	snoop_filter_disable Disable the snoop filter 0: Snoop filter operation is defined by the power state input, PSTATE. 1: Disable snoop filter operation

Bit	Attr	Reset Value	Description
1	RW	0x0	dvm_disable DVM message disable 0: Send speculative fetches according to the Speculation Control Register 1: Disable speculative fetches from all master interfaces
0	RW	0x0	snoop_disable snoop_disable control 0: Snoop masters according to the Snoop Control Registers 1: Disable all snoops, but not DVM messages

CCI500_SECURE_CTRL
Address: Operational Base + offset (0x00008)
Secure Access Register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	Debug_monitor_security_override 0: Enable Non-secure access to the PMU and Interface Monitor Registers. 1: Disable Non-secure access to the PMU and Interface Monitor Registers, unless overridden by bit[0]
0	RW	0x0	non_secure_override Non-secure register access override 0: Disable Non-secure access to CCI-400 registers 1: Enable Non-secure access to CCI-400 registers

CCI500_STATUS
Address: Operational Base + offset (0x0000c)
Status Register

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8	RW	0x0	SF_RAM_state_change_pending Snoop filter RAM power state change pending. This bit reads back the PREQ input. 0b0: No change pending, any previous requests have been accepted or denied. 0b1: State change is pending and might be accepted or denied
7:5	RW	0x0	SF_RAM_state_request This is the last requested power state of the snoop filter RAMs Encoding as SF_RAM_state.

Bit	Attr	Reset Value	Description
4:2	RW	0x0	SF_RAM_state The snoop filter RAM power states are 0b000: Off. 0b001: Static snoop filter RAM retention. 0b010: Reserved. 0b011: Dynamic snoop filter RAM retention. 0b100: On. 0b101-0b111 Reserved
1	RW	0x0	SF_RAM_initialization Indicates when the snoop filter RAM is initialized. Shareable requests are not serviced during this period. 0: Snoop filter RAM initialization is complete. 1: Snoop filter RAM initialization is in progress.
0	RW	0x0	Change_pending Indicates whether any changes to the Snoop Control Registers or the Control Override Register are pending in the CCI-500: 0: No change pending 1: Change pending

CCI500_ERROR_STATUS
Address: Operational Base + offset (0x00010)
Imprecise Error Register

Bit	Attr	Reset Value	Description
31:23	RO	0x0	reserved
22	RW	0x0	imprecise_err_slv6 Imprecise error indicator for slave interface 6 0b0: No error from the time this bit was last reset. 0b1: An error response has been received, but not signaled precisely.
21	RW	0x0	imprecise_err_slv5 Imprecise error indicator for slave interface 5 0b0: No error from the time this bit was last reset. 0b1: An error response has been received, but not signaled precisely.
20	RW	0x0	imprecise_err_slv4 Imprecise error indicator for slave interface 4 0b0: No error from the time this bit was last reset. 0b1: An error response has been received, but not signaled precisely.

Bit	Attr	Reset Value	Description
19	RW	0x0	imprecise_err_slv3 Imprecise error indicator for slave interface 3 0b0: No error from the time this bit was last reset. 0b1: An error response has been received, but not signaled precisely.
18	RW	0x0	imprecise_err_slv2 Imprecise error indicator for slave interface 2 0b0: No error from the time this bit was last reset. 0b1: An error response has been received, but not signaled precisely.
17	RW	0x0	imprecise_err_slv1 Imprecise error indicator for slave interface 1 0b0: No error from the time this bit was last reset. 0b1: An error response has been received, but not signaled precisely.
16	RW	0x0	imprecise_err_slv0 Imprecise error indicator for slave interface 0. 0b0: No error from the time this bit was last reset. 0b1: An error response has been received, but not signaled precisely.
15:6	RO	0x0	reserved
5	RW	0x0	imprecise_err_mst5 Imprecise error indicator for master interface 5 0: No error from the time this bit was last reset. 1: An error response has been received, but not signalled precisely.
4	RW	0x0	imprecise_err_mst4 Imprecise error indicator for master interface 4 0: No error from the time this bit was last reset. 1: An error response has been received, but not signalled precisely.

Bit	Attr	Reset Value	Description
3	RW	0x0	imprecise_err_mst3 Imprecise error indicator for master interface 3 0: No error from the time this bit was last reset. 1: An error response has been received, but not signalled precisely.
2	RW	0x0	imprecise_err_mst2 Imprecise error indicator for master interface 2 0: No error from the time this bit was last reset. 1: An error response has been received, but not signalled precisely.
1	RW	0x0	imprecise_err_mst1 Imprecise error indicator for master interface 1 0: No error from the time this bit was last reset. 1: An error response has been received, but not signalled precisely.
0	RW	0x0	imprecise_err_mst0 Imprecise error indicator for master interface 0: 0: No error from the time this bit was last reset. 1: An error response has been received, but not signalled precisely.

CCI500_PFMMON_CTRL
Address: Operational Base + offset (0x00100)
Performance Monitor Control Register (PMCR)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:11	RW	0x00	counter_num Specifies the number of counters implemented.
10:6	RO	0x0	reserved
5	RW	0x0	DP Disables cycle counter, CCNT, if non-invasive debug is prohibited: 0b0 Count is not disabled when NIDEN input is LOW. 0b1 Count is disabled when NIDEN input is LOW.

Bit	Attr	Reset Value	Description
4	RW	0x0	EX Enable export of the events to the event bus, EVNTBUS, for an external monitoring block to trace events: 0b0 Do not export EVNTBUS. 0b1 Export EVNTBUS.
3:2	RO	0x0	reserved
1	RW	0x0	RST Performance counter reset: 0b0 No action. 0b1 Reset all performance counters to zero, not including CCNT.
0	RW	0x0	CEN Enable bit: 0b0 Disable all counters, including CCNT. 0b1 Enable all counters, including CCNT.

CCI500_INTERFACE_MONITOR_CTRL
Address: Operational Base + offset (0x00104)
Snoop Control Register for slave interface x

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	Enable_Interface_Monitors 0b0 Interface Monitor counters and flags are set to 0. 0b1 Enable all Interface Monitors.

CCI500_SNOOP_CTRL_S0
Address: Operational Base + offset (0x01000)

Bit	Attr	Reset Value	Description
31	RW	0x0	Support_DVMs Slave interface supports DVM messages. This is overridden to 0x0 if you set the Control Override Register bit[1]
30	RW	0x0	Support_Snoops Slave interface supports snoop requests. This is overridden to 0x0 if you set the Control Override Register bit[0]
29:2	RO	0x0	reserved

Bit	Attr	Reset Value	Description
1	RW	0x0	Enable_DVMs Enable issuing of DVM message requests from this slave interface. RAZ/WI for interfaces not supporting DVM messages: 0b0: Disable DVM message requests. 0b1: Enable DVM message requests.
0	RW	0x0	enable_snoops Enable issuing of snoop requests from this slave interface. RAZ/WI for interfaces not supporting snoops: 0b0: Disable snoop requests. 0b1: Enable snoop requests.

CCI500_SHAREABLE_OVERRIDE_S0
Address: Operational Base + offset (0x01004)
Shareable Override Register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1:0	RW	0x0	Domain_Override Shareable override for slave interface: 0b00-0b01: Do not override AxDOMAIN inputs. 0b10: Override AxDOMAIN inputs to 0b00, meaning that all transactions are treated as non-shareable: ReadOnce becomes ReadNoSnoop. WriteUnique and WriteLineUnique become WriteNoSnoop. CleanShared, CleanInvalid, and MakeInvalid transactions do not generate snoops. 0b11 Override AxDOMAIN inputs to 0b01, meaning that all Normal transactions are treated as shareable: ReadNoSnoop becomes ReadOnce. WriteNoSnoop becomes WriteUnique. CleanShared, CleanInvalid, and MakeInvalid transactions generate snoops

CCI500_RD_CHAN_QOS_OVERRIDE_S0
Address: Operational Base + offset (0x01100)
Read Channel QoS Value Override Register for slave interface x

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved

Bit	Attr	Reset Value	Description
3:0	RW	0x0	arqos_override ARQOS value override for the slave interface

CCI500_WR_CHAN_QOS_OVERRIDE_S0
Address: Operational Base + offset (0x01104)
Write Channel QoS Value Override slave interface x

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x0	awqos_override AWQOS value override for the slave interface

CCI500_MAX_OT_S0
Address: Operational Base + offset (0x01110)
Maximum Outstanding Transactions Registers

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	max_OT The maximum number of OTs for the interface. This is a combined issuing limit. It represents the maximum number of transactions that the upstream master can issue when the AR and AW channels are considered as one issuing source.

CCI500_SNOOP_CTRL_S1
Address: Operational Base + offset (0x02000)

Bit	Attr	Reset Value	Description
31	RW	0x0	Support_DVMs Slave interface supports DVM messages. This is overridden to 0x0 if you set the Control Override Register bit[1]
30	RW	0x0	Support_Snoops Slave interface supports snoop requests. This is overridden to 0x0 if you set the Control Override Register bit[0]
29:2	RO	0x0	reserved
1	RW	0x0	Enable_DVMs Enable issuing of DVM message requests from this slave interface. RAZ/WI for interfaces not supporting DVM messages: 0b0: Disable DVM message requests. 0b1: Enable DVM message requests.

Bit	Attr	Reset Value	Description
0	RW	0x0	enable_snoops Enable issuing of snoop requests from this slave interface. RAZ/WI for interfaces not supporting snoops: 0b0: Disable snoop requests. 0b1: Enable snoop requests.

CCI500_SHAREABLE_OVERRIDE_S1
Address: Operational Base + offset (0x02004)
Shareable Override Register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1:0	RW	0x0	Domain_Override Shareable override for slave interface: 0b00-0b01: Do not override AxDOMAIN inputs. 0b10: Override AxDOMAIN inputs to 0b00, meaning that all transactions are treated as non-shareable: ReadOnce becomes ReadNoSnoop. WriteUnique and WriteLineUnique become WriteNoSnoop. CleanShared, CleanInvalid, and MakeInvalid transactions do not generate snoops. 0b11 Override AxDOMAIN inputs to 0b01, meaning that all Normal transactions are treated as shareable: ReadNoSnoop becomes ReadOnce. WriteNoSnoop becomes WriteUnique. CleanShared, CleanInvalid, and MakeInvalid transactions generate snoops

CCI500_RD_CHAN_QOS_OVERRIDE_S1
Address: Operational Base + offset (0x02100)
Read Channel QoS Value Override Register for slave interface x

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x0	arqos_override ARQOS value override for the slave interface

CCI500_WR_CHAN_QOS_OVERRIDE_S1
Address: Operational Base + offset (0x02104)
Write Channel QoS Value Override slave interface x

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved

Bit	Attr	Reset Value	Description
3:0	RW	0x0	awqos_override AWQOS value override for the slave interface

CCI500_MAX_OT_S1
Address: Operational Base + offset (0x02110)
Maximum Outstanding Transactions Registers

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	max_OT The maximum number of OTs for the interface. This is a combined issuing limit. It represents the maximum number of transactions that the upstream master can issue when the AR and AW channels are considered as one issuing source.

CCI500_SLAVE_INTERFACE_MONITOR_S0
Address: Operational Base + offset (0x90000)
Slave Interface Monitor Registers

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Outstanding_snoops Number of outstanding snoop requests or DVM messages. From request handshake to response or snoop data for a hit.
23:16	RW	0x00	Outstanding_writes Number of outstanding write transactions. From request handshake to response for ACE Lite interfaces or WACK for ACE interfaces.
15:8	RW	0x00	Outstanding_reads Number of outstanding read transactions. From request handshake to response or RACK for ACE interfaces.
7	RW	0x0	Stalled_CD_channel A transfer is stalled on the CD channel. CDVALID is HIGH. CDREADY is LOW. ACE slave only.
6	RW	0x0	Stalled_CR_channel A transfer is stalled on the CR channel. CRVALID is HIGH. CRREADY is LOW.
5	RW	0x0	Stalled_AC_channel A transfer is stalled on the AC channel. ACVALID is HIGH. ACREADY is LOW.

Bit	Attr	Reset Value	Description
4	RW	0x0	Stalled_B_channel A transfer is stalled on the B channel. BVALID is HIGH BREADY is LOW.
3	RW	0x0	Stalled_W_channel A transfer is stalled on the W channel. WVALID is HIGH. WREADY is LOW.
2	RW	0x0	Stalled_AW_channel A transfer is stalled on the AW channel. AWVALID is HIGH. AWREADY is LOW.
1	RW	0x0	Stalled_R_channel A transfer is stalled on the R channel. RVALID is HIGH. RREADY is LOW.
0	RW	0x0	Stalled_AR_channel A transfer is stalled on the AR channel.ARVALID is HIGH. ARREADY is LOW.

CCI500_SLAVE_INTERFACE_MONITOR_S1
Address: Operational Base + offset (0x90004)
Slave Interface Monitor Registers

Bit	Attr	Reset Value	Description
31:24	RW	0x00	Outstanding_snoops Number of outstanding snoop requests or DVM messages. From request handshake to response or snoop data for a hit.
23:16	RW	0x00	Outstanding_writes Number of outstanding write transactions. From request handshake to response for ACE Lite interfaces or WACK for ACE interfaces.
15:8	RW	0x00	Outstanding_reads Number of outstanding read transactions. From request handshake to response or RACK for ACE interfaces.
7	RW	0x0	Stalled_CD_channel A transfer is stalled on the CD channel. CDVALID is HIGH. CDREADY is LOW. ACE slave only.

Bit	Attr	Reset Value	Description
6	RW	0x0	Stalled_CR_channel A transfer is stalled on the CR channel. CRVALID is HIGH. CRREADY is LOW.
5	RW	0x0	Stalled_AC_channel A transfer is stalled on the AC channel. ACVALID is HIGH. ACREADY is LOW.
4	RW	0x0	Stalled_B_channel A transfer is stalled on the B channel. BVALID is HIGH BREADY is LOW.
3	RW	0x0	Stalled_W_channel A transfer is stalled on the W channel. WVALID is HIGH. WREADY is LOW.
2	RW	0x0	Stalled_AW_channel A transfer is stalled on the AW channel. AWVALID is HIGH. AWREADY is LOW.
1	RW	0x0	Stalled_R_channel A transfer is stalled on the R channel. RVALID is HIGH. RREADY is LOW.
0	RW	0x0	Stalled_AR_channel A transfer is stalled on the AR channel.ARVALID is HIGH. ARREADY is LOW.

CCI500_MASTER_INTERFACE_MONITOR_M0

Address: Operational Base + offset (0x90100)

Master Interface Monitor Registers

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x00	Outstanding_writes Number of outstanding write transactions. From request handshake to response.
15:8	RW	0x00	Outstanding_reads Number of outstanding read transactions. From request handshake to response.
7:5	RO	0x0	reserved
4	RW	0x0	Stalled_B_channel A transfer is stalled on the B channel. BVALID is HIGH BREADY is LOW.

Bit	Attr	Reset Value	Description
3	RW	0x0	Stalled_W_channel A transfer is stalled on the W channel. WVALID is HIGH. WREADY is LOW.
2	RW	0x0	Stalled_AW_channel A transfer is stalled on the AW channel. AWVALID is HIGH. AWREADY is LOW.
1	RW	0x0	Stalled_R_channel A transfer is stalled on the R channel. RVALID is HIGH. RREADY is LOW.
0	RW	0x0	Stalled_AR_channel A transfer is stalled on the AR channel.ARVALID is HIGH. ARREADY is LOW

CCI500_MASTER_INTERFACE_MONITOR_M1
Address: Operational Base + offset (0x90104)
Master Interface Monitor Registers

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x00	Outstanding_writes Number of outstanding write transactions. From request handshake to response.
15:8	RW	0x00	Outstanding_reads Number of outstanding read transactions. From request handshake to response.
7:5	RO	0x0	reserved
4	RW	0x0	Stalled_B_channel A transfer is stalled on the B channel. BVALID is HIGH BREADY is LOW.
3	RW	0x0	Stalled_W_channel A transfer is stalled on the W channel. WVALID is HIGH. WREADY is LOW.
2	RW	0x0	Stalled_AW_channel A transfer is stalled on the AW channel. AWVALID is HIGH. AWREADY is LOW.
1	RW	0x0	Stalled_R_channel A transfer is stalled on the R channel. RVALID is HIGH. RREADY is LOW.

Bit	Attr	Reset Value	Description
0	RW	0x0	Stalled_AR_channel A transfer is stalled on the AR channel.ARVALID is HIGH. ARREADY is LOW

8.5 Application Notes

8.5.1 QoS setting

The CPU read channel, VOP read channel, GPU write channel have the external QoS control. After reset each master port both have priority setting as 1. It's recommended that field 0 of QoS. ExtControl set to 1 to enable the external qos control. And priority setting of each master kept at 1.

8.5.2 Idle request

The main interconnect supports flushing the ongoing transaction when the software needed to do so.
If the GPU power domain need to disconnect from the main interconnect, Idle request has to be sent to GPU NIU, the NIU will respond a ack, and when it's ready to be disconnect, one Idle signal will be send out . Then, if GPU still have transaction to be sent to the memory scheduler, it will be stalled by the NIU.
If the GPU system power domain is disconnected as the above flow, then CPU want to access to the GPU system, it will response error or held to CPU according to the corresponding grf register setting.

The sequence is like following figure shows:

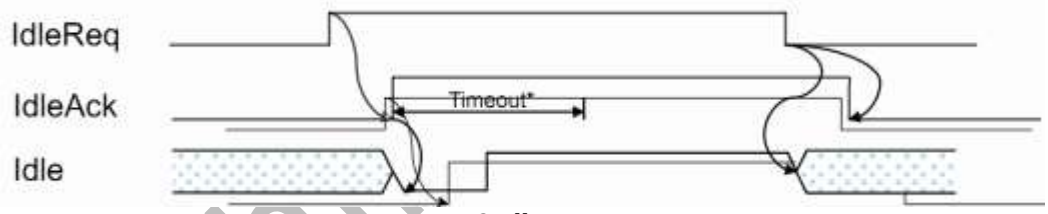


Fig. 7-2 Idle request

The idle request is set by GRF register.

8.5.3 Logging Errors

As described in section 11.3.2, there are four error loggers for different purpose. If there error happens, the software can read each error logger's register to find out more details.
Example:

- *slv_err_logger0* error reporting output is enabled by set *FaultEn* to '1';
- If *ErrVld* is set to 1 by interconnect, a noc fault interrupt will be generated;
- Read *Mid* in *Errlog5* to get the master of this error transaction, the *Mid* code is listed in Table 11-1;
- Read *Addr* in *Errlog3* to get the target slave of this error transaction;
- Read the other *Errlogx* register to get more information if needed;
- Set *ErrClr* to 1 to clear the error status.

8.5.4 Basic Packet Tracing

To trace packets, the packet probe must be programmed as follows:

- Select the interesting probe listed in section 11.3.4.
- Set field *TraceEn* of register *MainCtl* to 1 to enable forwarding of traced packets to the connected observer. Optionally set field *PayloadEn* of register *MainCtl* to 1 if the packet payload should be included in the trace.

- Set field *GlobalEn* of register *CfgCtl* to 1.

8.5.5 Counting packets over a fixed period

The following programming sequence counts packets at a given probe point using statistic counter 0.

- Select the interesting probe listed in section 11.3.4
- Set field *StatEn* to 1 in register *MainCtl*.
- Set register *Counters_0_Src* to 0x6 (PKT)to count packets.
- Specify the period during which the packets should be counted by setting register StatPeriod to: $\log_2$(interval expressed in number of probe clock cycles)
- Set field *GlobalEn* of register *CfgCtl* to 1 to enable packet counting.

Once time $2^{StatPeriod}$ has elapsed, the number of packets counted is dumped to the observer and can be read from *Counters_0_Val*.

8.5.6 Measuring bandwidth

The following programming sequence example shows how a packet probe can be used to measure bandwidth at a probe point.

Some important points to note about this example are:

- Statistics counters are chained together to support the maximum theoretical bandwidth. Counter 0 is configured to count bytes; counter 1 increments when counter 0 rolls over.
- The counter values are dumped to an observer after time $2^{StatPeriod}$.

The programming sequence is as follows:

- Select the interesting probe listed in section 11.3.4
- Set register *Counters_0_Src* to 0x8 (BYTES) to count bytes.
- Set register *Counters_1_Src* to 0x10 (CHAIN) to increment when counter 0 wraps.
- Specify the period during which the bytes should be counted by setting register *StatPeriod* to: $\log_2$(interval expressed in number of probe clock cycles).
- Set field *GlobalEn* of register *CfgCtl* to 1 to enable the counting of bytes.

Once time $2^{StatPeriod}$ has elapsed, the number of packets counted is dumped to the observer and can be read from *Counters_0_Val* and *Counters_0_Val*.

Chapter 9 DMC (Dynamic Memory Interface)

9.1 Overview

The DMC includes two section: multi-protocol DDR controller and multi-protocol DDR PHY. The DDR controller connects memory scheduler in interconnect by local bus, and interfaces to the DDR PHY via a DFI connection. The DDR Controller handles the transfer of memory data and also background tasks required for proper system operation, including memory maintenance, programming, training, calibration, system, and low power tasks.

The DDR PHY is a high-speed slice-based architecture with data and address slices. It encapsulates all functionality required to interface to external high-speed DDR DRAM devices into a single module. The DDR PHY provides control features to ease the customer implementation of digitally controlled features of the PHY such as initialization, training, and programmable configuration controls.

The DDR PHY Independent (PI) leveling core is included in PHY. The PI can operate PHY independent leveling and DRAM BIST without involvement of the DDR controller. A PI can be used in supporting various DRAM types. In PHY Independent mode, the PHY handles all PHY/DRAM communication and defines the final delays.

The DMC supports the following features:

- Complete, integrated DDR3/DDR3L/LPDDR3/LPDDR4 solution
- DFI 4.0 interface compatibility
- Support DFI interface 1:2 frequency ratio, such as using a 400MHz controller clock and 800MHz memory clock.
- Support dual channel, each channel up to 32 bits, totally support 64 bits data width
- Support interlace or non-interlace for dual channel
- Each channel has separately controller and PHY
- Support for x8, x16, and x32 memories, for a total memory data path width of 32 bits

- Up to 2 memory ranks for one channel; devices within a rank tie to a common chip select
- Up to 8 open memory banks, maximum of eight per rank
- Support totally 4G Bytes accessible address
- Support automatic power-down and self-refresh entry and exit
- Support software driven self-refresh entry and exit by programming controller register
- Support hardware driven self-refresh entry and exit by programming CIC register
- Support standby mode by clock gating when there is not any transmission
- Support DDR IO retention mode
- Programmable memory initialization
- Programmable per rank memory ODT (On-Die Termination) support for reads and writes
- Support training from controller or PHY:
  - DQS gate training
  - CA training
  - Write leveling
  - Read leveling
- Support controller interrupt
- Support hardware fast dynamic frequency change
- Support DDR monitor for debug:
  - AMBA 32-bit APB slave interface
  - Support to monitor DDR read or write address
  - Support to observe whether DDR access address within a specified range
  - Support to do the statistics about DDR read number, write number and active number
    - Hardware mode
    - Software mode
  - Support two channel separately monitor and observe
  - Support monitor interrupt

9.2 Block Diagram

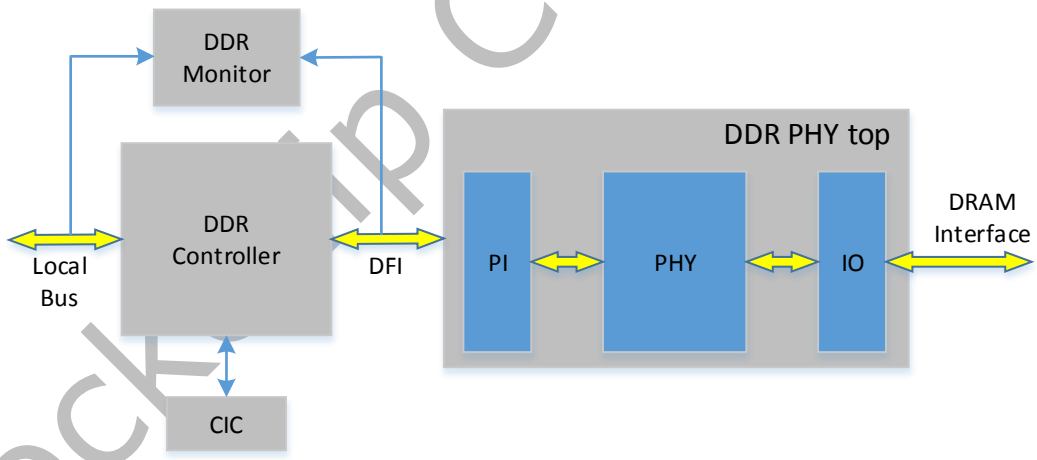


Fig. 9-1 DDR Architecture

9.3 Function Description

9.3.1 Controller Interface control (CIC)

The controller interface control (CIC) unit has three functions, the first function is to control external self-refresh. PMU can be configured to issue self-refresh enter or exit request. When CIC receives the request, it will generate the appropriate interface logic to let DDR controller send out self-refresh enter and exit command to DDR memory. And CIC will assert of de-assert a done status to PMU.

The second function of CIC is the standby mode of DDR controller and PHY. The standby mode is enable by programming CIC register. When there is not any bus access to DDR data and register, DDR controller will be idle. Once DDR controller idle for a period of time, CIC will generate the appropriate interface logic to gate the clock of DDR controller, DDR PHY and

memory scheduler.
The third function of CIC is to control the fast frequency change logic of DDR controller and PHY. The fast frequency change will be started by programming CIC register, and the flow of fast frequency change is controlled by CIC module. CIC will generate the appropriate interface logic to let DDR controller and PHY finish the fast frequency change flow.

9.3.2 DDR Monitor

The DDR Monitor Module has three functions, the first function is used when debug, it will monitor the DDR read or write address. The second function is also used when debug, it will observe whether DDR access address within a specified range. The third function is used to do the statistics about DDR bandwidth and utilization.

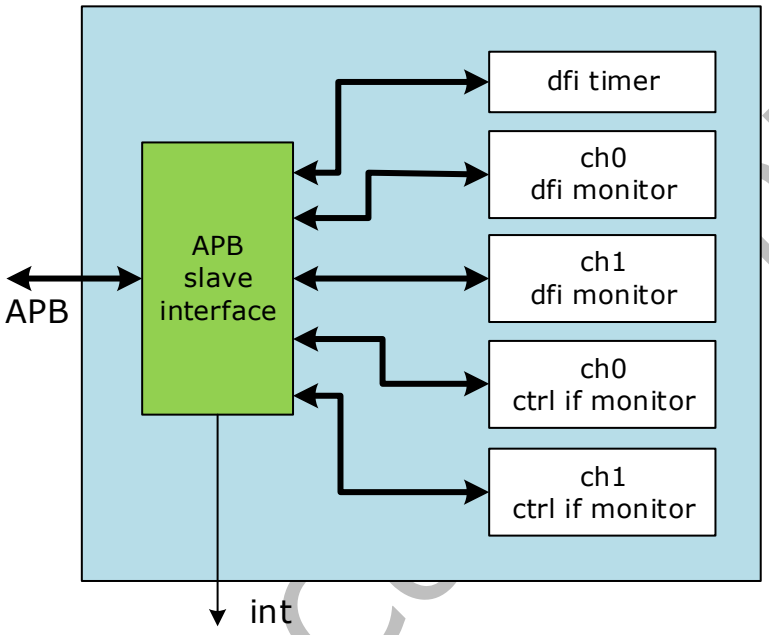


Fig. 9-2 DDR Monitor Block Diagram

The host processor gets access to DDR Monitor Register Block through the APB slave interface with 32-bit bus width, and asserts the active-high level interrupt.
DDR Monitor does the monitor and statistics by dfi monitor module and ctrl if monitor module.

9.4 Register Description

9.4.1 Registers Summary

1. DDR controller/phy register
The channel 0 controller base address is 0xffa80000.
The channel 1 controller base address is 0xffa88000.
The channel 0 PHY base address is 0xffa82000.
The channel 1 PHY base address is 0xffa8a000.

In this section, the access refers to the writeability of the parameter with the following definitions,
RW = Read/Write;
RD = Read Only;
WR = Write Only;
RW+ = Software Read/Write, Internal Writeable. These parameters may be read and written by software, but may also be changed by the internal logic;
RW_D = Read/Write. These parameters will be set to 0x0 at reset, but will change to a non-zero default value on the cycle following reset;

In this section, the register address increase by 1, but for cpu the address need multiply by 4.

Name	Register Address	Access	Controller Parameter(s)
DENALI_CTL_00	0x00	RD RW RW	VERSION DRAM_CLASS START
DENALI_CTL_01	0x01	RD RD RD RD	READ_DATA_FIFO_DEPTH MAX_CS_REG MAX_COL_REG MAX_ROW_REG
DENALI_CTL_02	0x02	RD RD RD RD	MEMCD_RMODW_FIFO_DEPTH WRITE_DATA_FIFO_PTR_WIDTH WRITE_DATA_FIFO_DEPTH READ_DATA_FIFO_PTR_WIDTH
DENALI_CTL_03	0x03	RD RD RD RD	DENALI0_WRFIFO_LOG2_DEPTH DENALI0_RMODWFIFO_LOG2_DEPTH DENALI0_CMDFIFO_LOG2_DEPTH MEMCD_RMODW_FIFO_PTR_WIDTH
DENALI_CTL_04	0x04	RW RD	DFS_CLOSE_BANKS DENALI0_WRCMD_SIDE_FIFO_LOG2_DEPTH
DENALI_CTL_05	0x05	RW	TINIT_F0
DENALI_CTL_06	0x06	RW	TINIT3_F0
DENALI_CTL_07	0x07	RW	TINIT4_F0
DENALI_CTL_08	0x08	RW	TINIT5_F0
DENALI_CTL_09	0x09	RW	TINIT_F1
DENALI_CTL_10	0x0a	RW	TINIT3_F1
DENALI_CTL_11	0x0b	RW	TINIT4_F1
DENALI_CTL_12	0x0c	RW	TINIT5_F1
DENALI_CTL_13	0x0d	RW	TINIT_F2
DENALI_CTL_14	0x0e	RW	TINIT3_F2
DENALI_CTL_15	0x0f	RW	TINIT4_F2
DENALI_CTL_16	0x10	RW RW	NO_AUTO_MRR_INIT TINIT5_F2
DENALI_CTL_17	0x11	RW RW RW RD	NO_MRW_INIT NO_MRW_BT_INIT DFI_INV_DATA_CS MRR_ERROR_STATUS
DENALI_CTL_18	0x12	RW RW RW RW	DFIBUS_BOOT_FREQ DFIBUS_FREQ_INIT PHY_INDEP_TRAIN_MODE NO_PHY_IND_TRAIN_INIT

Name	Register Address	Access	Controller Parameter(s)
DENALI_CTL_19	0x13	RW RW RW	DFIBUS_FR EQ_F2 DFIBUS_FR EQ_F1 DFIBUS_FR
DENALI_CTL_20	0x14	RW	TRST_PWRON
DENALI_CTL_21	0x15	RW	CKE_INACTIVE
DENALI_CTL_22	0x16	RW RW	TDLL_F1 TDLL_F0
DENALI_CTL_23	0x17	RW RW RW	WRLAT_F0 CASLAT_LIN_F0 TDLL_F2
DENALI_CTL_24	0x18	RW RW RW RW	ADDITIVE_LAT_F1 WRLAT_F1 CASLAT_LIN_F1 ADDITIVE_LAT_F0
DENALI_CTL_25	0x19	RW RW RW	TBST_INT_INTERVAL ADDITIVE_LAT_F2 WRLAT_F2 CASLAT_LIN_F2
DENALI_CTL_26	0x1a	RW RW RW	TRC_F0 TRRD_F0 TCCDMW TCCD
DENALI_CTL_27	0x1b	RW RW RW	TFAW_F0 TRP_F0 TWTR_F0 TRAS_MIN_F0
DENALI_CTL_28	0x1c	RW RW RW RW	TRAS_MIN_F1 TRC_F1 TRRD_F1 CA_DEFAULT_VAL_F0
DENALI_CTL_29	0x1d	RW RW RW RW	CA_DEFAULT_VAL_F1 TFAW_F1 TRP_F1 TWTR_F1
DENALI_CTL_30	0x1e	RW RW RW RW	TWTR_F2 TRAS_MIN_F2 TRC_F2 TRRD_F2
DENALI_CTL_31	0x1f	RW RW RW RW	TRTP_F0 CA_DEFAULT_VAL_F2 TFAW_F2 TRP_F2
DENALI_CTL_32	0x20	RW RW	TMOD_F0 TMRD_F0
DENALI_CTL_33	0x21	RW RW	TCKE_F0 TRAS_MAX_F0

Name	Register Address	Access	Controller Parameter(s)
DENALI_CTL_34	0x22	RW RW RW RW	TMOD_F1 TMRD_F1 TRTP_F1 TCKESR_F0
DENALI_CTL_35	0x23	RW RW	TCKE_F1 TRAS_MAX_F1
DENALI_CTL_36	0x24	RW RW RW RW	TMOD_F2 TMRD_F2 TRTP_F2 TCKESR_F1
DENALI_CTL_37	0x25	RW RW	TCKE_F2 TRAS_MAX_F2
DENALI_CTL_38	0x26	RW RW RW_D RW	RESERVED RESERVED TPPD TCKESR_F2
DENALI_CTL_39	0x27	RW RW RW RW	TRCD_F1 TWR_F0 TRCD_F0 WRITEINTERR
DENALI_CTL_40	0x28	RW RW RW RW	TMRR TWR_F2 TRCD_F2 TWR_F1
DENALI_CTL_41	0x29	RW RW RW	TCAMRD TCAENT TCACKEL
DENALI_CTL_42	0x2a	RW RW RW RW	TMRZ_F1 TMRZ_F0 TCACKEH TCAEXT
DENALI_CTL_43	0x2b	RW RW RW RW	TRAS_LOCKOUT CONCURRENTAP AP TMRZ_F2
DENALI_CTL_44	0x2c	RW_D RW RW RW	BSTLEN TDAL_F2 TDAL_F1 TDAL_F0
DENALI_CTL_44	0x2c	RW_D RW RW RW	BSTLEN TDAL_F2 TDAL_F1 TDAL_F0

Name	Register Address	Access	Controller Parameter(s)
DENALI_CTL_45	0x2d	RW	REG_DIMM_ENABLE
		RW	TRP_AB_F2
		RW	TRP_AB_F1
		RW	TRP_AB_F0
DENALI_CTL_46	0x2e	RW	NO_MEMORY_DM
		RW	RESERVED
		RW	RESERVED
		RW	ADDRESS_MIRRORING
DENALI_CTL_47	0x2f	RW	RESERVED
		RW	TREF_ENABLE
		RW	RESERVED
		WR	AREFRESH
DENALI_CTL_48	0x30	RW	TREF_F0
		RW	TRFC_F0
DENALI_CTL_49	0x31	RW	TREF_F1
		RW	TRFC_F1
DENALI_CTL_50	0x32	RW	TREF_F2
		RW	TRFC_F2
DENALI_CTL_51	0x33	RW	TREF_INTERVAL
DENALI_CTL_52	0x34	RW	TPDEX_F1
		RW	TPDEX_F0
DENALI_CTL_53	0x35	RW	TXPDLL_F0
		RW	TPDEX_F2
DENALI_CTL_54	0x36	RW	TXPDLL_F2
		RW	TXPDLL_F1
DENALI_CTL_55	0x37	RW	TCSCKE_F0
		RW	TMRRI_F2
		RW	TMRRI_F1
		RW	TMRRI_F0
DENALI_CTL_56	0x38	RW	TZQCKE_F0
		RW	TMRWCKEL_F0
		RW	TCKEHCS_F0
		RW	TCKELCS_F0
DENALI_CTL_57	0x39	RW	TMRWCKEL_F1
		RW	TCKEHCS_F1
		RW	TCKELCS_F1
		RW	TCSCKE_F1
DENALI_CTL_58	0x3a	RW	TCKEHCS_F2
		RW	TCKELCS_F2
		RW	TCSCKE_F2
		RW	TZQCKE_F1
DENALI_CTL_59	0x3b	RW	TXSR_F0
		RW	TZQCKE_F2
		RW	TMRWCKEL_F2
DENALI_CTL_60	0x3c	RW	TXSR_F1
		RW	TXSNR_F0

Name	Register Address	Access	Controller Parameter(s)
DENALI_CTL_61	0x3d	RW RW	TXSR_F2 TXSNR_F1
DENALI_CTL_62	0x3e	RW RW RW	TCKEHCMD_F0 TCKELCMD_F0 TXSNR_F2
DENALI_CTL_63	0x3f	RW RW RW RW	TCKELPD_F0 TESCKE_F0 TSR_F0 TCKCKEL_F0
DENALI_CTL_64	0x40	RW RW RW RW	TCKEHCMD_F1 TCKELCMD_F1 TCMDCKE_F0 TCSCKEH_F0
DENALI_CTL_65	0x41	RW RW RW RW	TCKELPD_F1 TESCKE_F1 TSR_F1 TCKCKEL_F1
DENALI_CTL_66	0x42	RW RW RW RW	TCKEHCMD_F2 TCKELCMD_F2 TCMDCKE_F1 TCSCKEH_F1
DENALI_CTL_67	0x43	RW RW RW RW	TCKELPD_F2 TESCKE_F2 TSR_F2 TCKCKEL_F2
DENALI_CTL_68	0x44	RW RW RW RW	SREFRESH_EXIT_NO_REFRESH PWRUP_SREFRESH_EXIT TCMDCKE_F2 TCSCKEH_F2
DENALI_CTL_69	0x45	RD WR RW RW	DFS_STATUS RESERVED CKE_DELAY ENABLE_QUICK_SREFRESH
DENALI_CTL_70	0x46	RW RW RW RW	DFS_RDLVL_EN DFS_WRLVL_EN DFS_CALVL_EN DFS_ZQ_EN
DENALI_CTL_71	0x47	RW RW	DFS_PROMOTE_THRESHOLD_F0 DFS_RDLVL_GATE_EN
DENALI_CTL_72	0x48	RW RW	DFS_PROMOTE_THRESHOLD_F2 DFS_PROMOTE_THRESHOLD_F1
DENALI_CTL_73	0x49	RW RD RD RD	RESERVED ZQ_CALINIT_CS_CL_STATUS ZQ_CALLATCH_STATUS ZQ_CALSTART_STATUS

Name	Register Address	Access	Controller Parameter(s)
DENALI_CTL_74	0x4a	RW RW RW RW	RESERVED RESERVED RESERVED RESERVED
DENALI_CTL_75	0x4b	RW RW	UPD_CTRLUPD_HIGH_THRESHOL D_F0
DENALI_CTL_76	0x4c	RW RW	UPD_CTRLUPD_SW_PROMOTE_TH RESHOLD_F0
DENALI_CTL_77	0x4d	RW RW	UPD_CTRLUPD_NORM_THRESHO LD_F1
DENALI_CTL_78	0x4e	RW RW	UPD_CTRLUPD_TIMEOUT_F1 UPD_CTRLUPD_HIGH_THRESHOLD
DENALI_CTL_79	0x4f	RW RW	UPD_PHYUPD_DFI_PROMOTE_TH RESHOLD_F1
DENALI_CTL_80	0x50	RW RW	UPD_CTRLUPD_HIGH_THRESHOL D_F2
DENALI_CTL_81	0x51	RW RW	UPD_CTRLUPD_SW_PROMOTE_TH RESHOLD_F2
DENALI_CTL_82	0x52	RW RW	TDFI_PHYMSTR_MAX_F0 UPD_PHYUPD_DFI_PROMOTE_THR
DENALI_CTL_83	0x53	RW RW	PHYMSTR_DFI_PROMOTE_THRESH OLD_F0
DENALI_CTL_84	0x54	RW RW	TDFI_PHYMSTR_RESP_F1 TDFI_PHYMSTR_MAX_F1
DENALI_CTL_85	0x55	RW RW	TDFI_PHYMSTR_MAX_F2 PHYMSTR_DFI_PROMOTE_THRESH
DENALI_CTL_86	0x56	RW RW	PHYMSTR_DFI_PROMOTE_THRESH OLD_F2 TDFI_PHYMSTR_RESP_F2
DENALI_CTL_87	0x57	RW RD RW	MRR_TEMPCHK_NORM_THRESHOL D_F0 PHYMSTR_ERROR_STATUS PHYMSTR_NO_AREF
DENALI_CTL_88	0x58	RW RW	MRR_TEMPCHK_TIMEOUT_F0 MRR_TEMPCHK_HIGH_THRESHOL
DENALI_CTL_89	0x59	RW RW	MRR_TEMPCHK_HIGH_THRESHO LD_F1 MRR_TEMPCHK_NORM_THRESHOL
DENALI_CTL_90	0x5a	RW RW	MRR_TEMPCHK_NORM_THRESHOL D_F2 MRR_TEMPCHK_TIMEOUT_F1
DENALI_CTL_91	0x5b	RW RW	MRR_TEMPCHK_TIMEOUT_F2 MRR_TEMPCHK_HIGH_THRESHO LD_F2
DENALI_CTL_92	0x5c	RW RW RW RW	CKSRE_F1 CKSRX_F0 CKSRE_F0 LOWPOWER_REFRESH_ENABLE

Name	Register Address	Access	Controller Parameter(s)
DENALI_CTL_93	0x5d	WR RW RW RW	LP_CMD CKSRX_F2 CKSRE_F2 CKSRX_F1
DENALI_CTL_94	0x5e	RW RW RW RW	LPI_SRPD_LITE_WAKEUP_F0 LPI_SR_MCCLK_GATE_WAKEUP_ F0 LPI_SR_WAKEUP_F0 LPI_PD_WAKEUP_F0
DENALI_CTL_95	0x5f	RW RW RW RW	LPI_PD_WAKEUP_F1 LPI_TIMER_WAKEUP_F0 LPI_SRPD_DEEP_MCCLK_GATE_ WAKEUP_F0 LPI_SRPD_DEEP_WAKEUP_F0
DENALI_CTL_96	0x60	RW RW RW RW	LPI_SRPD_DEEP_WAKEUP_F1 LPI_SRPD_LITE_WAKEUP_F1 LPI_SR_MCCLK_GATE_WAKEUP_ F1 LPI_SR_WAKEUP_F1
DENALI_CTL_97	0x61	RW RW RW RW	LPI_SR_WAKEUP_F2 LPI_PD_WAKEUP_F2 LPI_TIMER_WAKEUP_F1 LPI_SRPD_DEEP_MCCLK_GATE_ WAKEUP_F1
DENALI_CTL_98	0x62	RW RW RW RW	LPI_SRPD_DEEP_MCCLK_GATE_ WAKEUP_F2 LPI_SRPD_DEEP_WAKEUP_F2 LPI_SRPD_LITE_WAKEUP_F2 LPI_SR_MCCLK_GATE_WAKEUP_ F2
DENALI_CTL_99	0x63	RW RW RW	LPI_TIMER_COUNT LPI_WAKEUP_EN LPI_TIMER_WAKEUP_F2
DENALI_CTL_100	0x64	RD RW RW	LP_STATE TDFI_LP_RESP LPI_WAKEUP_TIMEOUT
DENALI_CTL_101	0x65	RW RW RW	LP_AUTO_MEM_GATE_EN LP_AUTO_EXIT_EN LP_AUTO_ENTRY_EN
DENALI_CTL_102	0x66	RW RW	LP_AUTO_SRPD_LITE_IDLE LP_AUTO_PD_IDLE
DENALI_CTL_103	0x67	RW RW RW	HW_PROMOTE_THRESHOLD_F0 LP_AUTO_SR_MC_GATE_IDLE LP_AUTO_SR_IDLE
DENALI_CTL_104	0x68	RW RW	HW_PROMOTE_THRESHOLD_F2 HW_PROMOTE_THRESHOLD_F1
DENALI_CTL_105	0x69	RW RW	LPC_PROMOTE_THRESHOLD_F1 LPC_PROMOTE_THRESHOLD_F0

Name	Register Address	Access	Controller Parameter(s)
DENALI_CTL_106	0x6a	RW RW RW	LPC_SR_PHYUPD_EN LPC_SR_CTRLUPD_EN LPC_PROMOTE_THRESHOLD_F2
DENALI_CTL_107	0x6b	RW RW RW	LPC_SR_ZQ_EN RESERVED LPC_SR_PHYMSTR_EN
DENALI_CTL_108	0x6c	RW RW RW	DFS_DLL_OFF DFS_ENABLE RESERVED
DENALI_CTL_109	0x6d	RW_D RW_D RW_D	TDFI_INIT_START_F1 TDFI_INIT_COMPLETE_F0 TDFI_INIT_START_F0
DENALI_CTL_110	0x6e	RW_D RW_D	TDFI_INIT_START_F2 TDFI_INIT_COMPLETE_F1
DENALI_CTL_111	0x6f	RW RD RW_D	DFS_PHY_REG_WRITE_EN CURRENT_REG_COPY TDFI_INIT_COMPLETE_F2
DENALI_CTL_112	0x70	RW	DFS_PHY_REG_WRITE_ADDR
DENALI_CTL_113	0x71	RW	DFS_PHY_REG_WRITE_DATA_F0
DENALI_CTL_114	0x72	RW	DFS_PHY_REG_WRITE_DATA_F1
DENALI_CTL_115	0x73	RW	DFS_PHY_REG_WRITE_DATA_F2
DENALI_CTL_116	0x74	RW	DFS_PHY_REG_WRITE_MASK
DENALI_CTL_117	0x75	RW+	WRITE_MODEREG
DENALI_CTL_118	0x76	RW+	READ_MODEREG MRW_STATUS
DENALI_CTL_119	0x77	RD	PERIPHERAL_MRR_DATA [31:0]
DENALI_CTL_120	0x78	RD RD	AUTO_TEMPCHK_VAL_0 PERIPHERAL_MRR_DATA [39:32]
DENALI_CTL_121	0x79	RW RD	DISABLE_UPDATE_TVRCG AUTO_TEMPCHK_VAL_1
DENALI_CTL_122	0x7a	RW RW	TVRCG_ENABLE_F0 MRW_DFS_UPDATE_FRC
DENALI_CTL_123	0x7b	RW RW	TFC_F0 TVRCG_DISABLE_F0
DENALI_CTL_124	0x7c	RW RW RW	TVREF_LONG_F0 TCKFSPX_F0 TCKFSPE_F0
DENALI_CTL_125	0x7d	RW RW	TVRCG_DISABLE_F1 TVRCG_ENABLE_F1
DENALI_CTL_126	0x7e	RW RW RW	TCKFSPX_F1 TCKFSPE_F1 TFC_F1
DENALI_CTL_127	0x7f	RW RW	TVRCG_ENABLE_F2 TVREF_LONG_F1
DENALI_CTL_128	0x80	RW RW	TFC_F2 TVRCG_DISABLE_F2

Name	Register Address	Access	Controller Parameter(s)
DENALI_CTL_129	0x81	RW RW RW	TVREF_LONG_F2 TCKFSPX_F2 TCKFSPE_F2
DENALI_CTL_130	0x82	RW RW	MRR_PROMOTE_THRESH OLD_F1
DENALI_CTL_131	0x83	RW RW	MRW_PROMOTE_THRES HOLD_F0
DENALI_CTL_132	0x84	RW RW	MRW_PROMOTE_THRES HOLD_F2
DENALI_CTL_133	0x85	RW RW	MR1_DATA_F0_0 MR0_DATA_F0_0
DENALI_CTL_134	0x86	RW RW	MR0_DATA_F1_0 MR2_DATA_F0_0
DENALI_CTL_135	0x87	RW RW	MR2_DATA_F1_0 MR1_DATA_F1_0
DENALI_CTL_136	0x88	RW RW	MR1_DATA_F2_0 MR0_DATA_F2_0
DENALI_CTL_137	0x89	RW RW	MRSINGLE_DATA_0 MR2_DATA_F2_0
DENALI_CTL_138	0x8a	RW RW	MR3_DATA_F1_0 MR3_DATA_F0_0
DENALI_CTL_139	0x8b	RW RD RW	MR11_DATA_F0_0 MR8_DATA_0 MR3_DATA_F2_0
DENALI_CTL_140	0x8c	RW RW RW	MR12_DATA_F0_0 MR11_DATA_F2_0 MR11_DATA_F1_0
DENALI_CTL_141	0x8d	RW RW	MR12_DATA_F2_0 MR12_DATA_F1_0
DENALI_CTL_142	0x8e	RW RW	MR14_DATA_F0_0 MR13_DATA_0
DENALI_CTL_143	0x8f	RW RW	MR14_DATA_F2_0 MR14_DATA_F1_0
DENALI_CTL_144	0x90	RW RW RW RW	MR16_DATA_0 MR_FSP_DATA_VALID_F2_0 MR_FSP_DATA_VALID_F1_0 MR_FSP_DATA_VALID_F0_0
DENALI_CTL_145	0x91	RW RD RW	MR22_DATA_F0_0 MR20_DATA_0 MR17_DATA_0
DENALI_CTL_146	0x92	RW RW	MR22_DATA_F2_0 MR22_DATA_F1_0
DENALI_CTL_147	0x93	RW RW	MR1_DATA_F0_1 MR0_DATA_F0_1
DENALI_CTL_148	0x94	RW RW	MR0_DATA_F1_1 MR2_DATA_F0_1
DENALI_CTL_149	0x95	RW RW	MR2_DATA_F1_1 MR1_DATA_F1_1

Name	Register Address	Access	Controller Parameter(s)
DENALI_CTL_150	0x96	RW RW	MR1_DATA_F2_1 MR0_DATA_F2_1
DENALI_CTL_151	0x97	RW RW	MRSINGLE_DATA_1 MR2_DATA_F2_1
DENALI_CTL_152	0x98	RW RW	MR3_DATA_F1_1 MR3_DATA_F0_1
DENALI_CTL_153	0x99	RW RD RW	MR11_DATA_F0_1 MR8_DATA_1 MR3_DATA_F2_1
DENALI_CTL_154	0x9a	RW RW RW	MR12_DATA_F0_1 MR11_DATA_F2_1 MR11_DATA_F1_1
DENALI_CTL_155	0x9b	RW RW	MR12_DATA_F2_1 MR12_DATA_F1_1
DENALI_CTL_156	0x9c	RW RW	MR14_DATA_F0_1 MR13_DATA_1
DENALI_CTL_157	0x9d	RW RW	MR14_DATA_F2_1 MR14_DATA_F1_1
DENALI_CTL_158	0x9e	RW RW RW RW	MR16_DATA_1 MR_FSP_DATA_VALID_F2_1 MR_FSP_DATA_VALID_F1_1 MR_FSP_DATA_VALID_F0_1
DENALI_CTL_159	0x9f	RW RD RW	MR22_DATA_F0_1 MR20_DATA_1 MR17_DATA_1
DENALI_CTL_160	0xa0	RW RW	MR22_DATA_F2_1 MR22_DATA_F1_1
DENALI_CTL_161	0xa1	RW RD RD RD	FSP_PHY_UPDATE_MRW RESERVED RESERVED RL3_SUPPORT_EN
DENALI_CTL_162	0xa2	RW+ RW+ RW RW	FSP_WR_CURRENT FSP_OP_CURRENT FSP_STATUS DFS_ALWAYS_WRITE_FSP
DENALI_CTL_163	0xa3	RW+ RW+ RW+ RW+	FSP1_FRC FSP0_FRC FSP1_FRC_VALID FSP0_FRC_VALID
DENALI_CTL_164	0xa4	RW RW RW RW	AREF_MAX_DEFICIT AREF_HIGH_THRESHOLD AREF_NORM_THRESHOLD LONG_COUNT_MASK

Name	Register Address	Access	Controller Parameter(s)
DENALI_CTL_165	0xa5	RW RW	ZQ_CALSTART_NORM_THRESHOLD_F0 AREF_MAX_CREDIT
DENALI_CTL_166	0xa6	RW RW	ZQ_CALLATCH_HIGH_THRESHOLD_F0 ZQ_CALSTART_HIGH_THRESHOLD_F0
DENALI_CTL_167	0xa7	RW RW	ZQ_CS_HIGH_THRESHOLD_F0 ZQ_CS_NORM_THRESHOLD_F0
DENALI_CTL_168	0xa8	RW RW	ZQ_CALLATCH_TIMEOUT_F0 ZQ_CALSTART_TIMEOUT_F0
DENALI_CTL_169	0xa9	RW RW	ZQ_PROMOTE_THRESHOLD_F0 ZQ_CS_TIMEOUT_F0
DENALI_CTL_170	0xaa	RW RW	ZQ_CALSTART_HIGH_THRESHOLD_F1 ZQ_CALSTART_NORM_THRESHOLD_F1
DENALI_CTL_171	0xab	RW RW	ZQ_CS_NORM_THRESHOLD_F1 ZQ_CALLATCH_HIGH_THRESHOLD_F1
DENALI_CTL_172	0xac	RW RW	ZQ_CALSTART_TIMEOUT_F1 ZQ_CS_HIGH_THRESHOLD_F1
DENALI_CTL_173	0xad	RW RW	ZQ_CS_TIMEOUT_F1 ZQ_CALLATCH_TIMEOUT_F1
DENALI_CTL_174	0xae	RW RW	ZQ_CALSTART_NORM_THRESHOLD_F2 ZQ_PROMOTE_THRESHOLD_F1
DENALI_CTL_175	0xaf	RW RW	ZQ_CALLATCH_HIGH_THRESHOLD_F2 ZQ_CALSTART_HIGH_THRESHOLD_F2
DENALI_CTL_176	0xb0	RW RW	ZQ_CS_HIGH_THRESHOLD_F2 ZQ_CS_NORM_THRESHOLD_F2
DENALI_CTL_177	0xb1	RW RW	ZQ_CALLATCH_TIMEOUT_F2 ZQ_CALSTART_TIMEOUT_F2
DENALI_CTL_178	0xb2	RW RW	ZQ_PROMOTE_THRESHOLD_F2 ZQ_CS_TIMEOUT_F2
DENALI_CTL_179	0xb3	RW_D RW	ZQINIT_F0 RESERVED
DENALI_CTL_180	0xb4	RW RW	ZQCS_F0 ZQCL_F0
DENALI_CTL_181	0xb5	RW RW	TZQLAT_F0 TZQCAL_F0
DENALI_CTL_182	0xb6	RW RW_D	ZQCL_F1 ZQINIT_F1
DENALI_CTL_183	0xb7	RW RW	TZQCAL_F1 ZQCS_F1

Name	Register Address	Access	Controller Parameter(s)
DENALI_CTL_184	0xb8	RW_D RW	ZQINIT_F2 TZQLAT_F1
DENALI_CTL_185	0xb9	RW RW	ZQCS_F2 ZQCL_F2
DENALI_CTL_186	0xba	RW RW RW	ZQ_SW_REQ_START_LATCH_MAP TZQLAT_F2 TZQCAL_F2
DENALI_CTL_187	0xbb	RW RD WR	ZQRESET_F0 ZQ_REQ_PENDING ZQ_REQ
DENALI_CTL_188	0xbc	RW RW	ZQRESET_F2 ZQRESET_F1
DENALI_CTL_189	0xbd	RW_D RW_D RW RW	ZQ_CAL_LATCH_MAP_0 ZQ_CAL_START_MAP_0 ZQCS_ROTATE NO_ZQ_INIT
DENALI_CTL_190	0xbe	RW RW RW_D RW_D	ROW_DIFF BANK_DIFF ZQ_CAL_LATCH_MAP_1 ZQ_CAL_START_MAP_1
DENALI_CTL_191	0xbf	RW_D RW RW RW	APREBIT BANK_ADDR_INTLV_EN BANK_START_BIT COL_DIFF
DENALI_CTL_192	0xc0	RW RW RW RW	RESERVED ADDR_CMP_EN COMMAND_AGE_COUNT AGE_COUNT
DENALI_CTL_193	0xc1	RW RW RW RW	RW_SAME_EN PRIORITY_EN PLACEMENT_EN BANK_SPLIT_EN
DENALI_CTL_194	0xc2	RW RW RW RW	DISABLE_RW_GROUP_W_BNK_ CONFLICT W2R_SPLIT_EN CS_SAME_EN RW_SAME_PAGE_EN
DENALI_CTL_195	0xc3	RW RW RW RW	INHIBIT_DRAM_CMD DISABLE_RD_INTERLEAVE SWAP_EN NUM_Q_ENTRIES_ACT_DISABL E
DENALI_CTL_196	0xc4	RW RW RW	BIG_ENDIAN_EN REDUC BURST_ON_FLY_BIT

Name	Register Address	Access	Controller Parameter(s)
		RW	CS_MAP
DENALI_CTL_197	0xc5	RW RW RW RW	RESERVED RESERVED RESERVED MEMDATA_RATIO_0
DENALI_CTL_198	0xc6	RW RW RW RW	RESERVED RESERVED MEMDATA_RATIO_1 RESERVED
DENALI_CTL_199	0xc7	RW RW RW RW	IN_ORDER_ACCEPT Q_FULLNESS RESERVED RESERVED
DENALI_CTL_200	0xc8	RW RW WR RD	PREAMBLE_SUPPORT CTRLUPD_REQ_PER_AREF_EN CTRLUPD_REQ CONTROLLER_BUSY
DENALI_CTL_201	0xc9	RD RW RW RW	DFI_ERROR RD_DBI_EN WR_DBI_EN RD_PREAMBLE_TRAINING_EN
DENALI_CTL_202	0xca	RW+ RD	RESERVED DFI_ERROR_INFO
DENALI_CTL_203	0xcb	RD	INT_STATUS [31:0]
DENALI_CTL_204	0xcc	RD	INT_STATUS [33:32]
DENALI_CTL_205	0xcd	WR	INT_ACK [31:0]
DENALI_CTL_206	0xce	WR	INT_ACK [32]
DENALI_CTL_207	0xcf	RW	INT_MASK [31:0]
DENALI_CTL_208	0xd0	RW	INT_MASK [33:32]
DENALI_CTL_209	0xd1	RD	OUT_OF_RANGE_ADDR [31:0]
DENALI_CTL_210	0xd2	RD RD RD	OUT_OF_RANGE_TYPE OUT_OF_RANGE_LENGTH OUT_OF_RANGE_ADDR [33:32]
DENALI_CTL_211	0xd3	RW RW RW RD	ODT_RD_MAP_CS1 ODT_WR_MAP_CS0 ODT_RD_MAP_CS0 OUT_OF_RANGE_SOURCE_ID
DENALI_CTL_212	0xd4	RW RW RW RW	TODTL_2CMD_F2 TODTL_2CMD_F1 TODTL_2CMD_F0 ODT_WR_MAP_CS1

Name	Register Address	Access	Controller Parameter(s)
DENALI_CTL_213	0xd5	RW RW RW RW	ODT_EN_F1 ODT_EN_F0 TODTH_RD TODTH_WR
DENALI_CTL_214	0xd6	RW RW RW RW	WR_TO_ODTH_F1 WR_TO_ODTH_F0 EN_ODT_ASSERT_EXCEPT_RD ODT_EN_F2
DENALI_CTL_215	0xd7	RW RW RW RW	RD_TO_ODTH_F2 RD_TO_ODTH_F1 RD_TO_ODTH_F0 WR_TO_ODTH_F2
DENALI_CTL_216	0xd8	RW_D RW_D RW_D RW_D	R2R_DIFFCS_DLY_F0 RW2MRW_DLY_F2 RW2MRW_DLY_F1 RW2MRW_DLY_F0
DENALI_CTL_217	0xd9	RW_D RW_D RW_D RW_D	R2R_DIFFCS_DLY_F1 W2W_DIFFCS_DLY_F0 W2R_DIFFCS_DLY_F0 R2W_DIFFCS_DLY_F0
DENALI_CTL_218	0xda	RW_D RW_D RW_D RW_D	R2R_DIFFCS_DLY_F2 W2W_DIFFCS_DLY_F1 W2R_DIFFCS_DLY_F1 R2W_DIFFCS_DLY_F1
DENALI_CTL_219	0xdb	RW RW_D RW_D RW_D	R2R_SAMECS_DLY W2W_DIFFCS_DLY_F2 W2R_DIFFCS_DLY_F2 R2W_DIFFCS_DLY_F2
DENALI_CTL_220	0xdc	RW RW_D RW_D RW_D	W2R_SAMECS_DLY R2W_SAMECS_DLY_F2 R2W_SAMECS_DLY_F1 R2W_SAMECS_DLY_F0
DENALI_CTL_221	0xdd	RW RW RW RW	TDQSCK_MAX_F1 TDQSCK_MIN_F0 TDQSCK_MAX_F0 W2W_SAMECS_DLY
DENALI_CTL_222	0xde	RW RW RW RW	SW_LEVELING_MODE TDQSCK_MIN_F2 TDQSCK_MAX_F2 TDQSCK_MIN_F1
DENALI_CTL_223	0xdf	RD WR WR WR	SWLVL_OP_DONE SWLVL_EXIT SWLVL_START SWLVL_LOAD

Name	Register Address	Access	Controller Parameter(s)
DENALI_CTL_224	0xe0	RD RD RD RD	SWLVL_RESP_3 SWLVL_RESP_2 SWLVL_RESP_1 SWLVL_RESP_0
DENALI_CTL_225	0xe1	RW RW WR RW	WLDQSEN WRLVL_CS WRLVL_REQ PHYUPD_APPEND_EN
DENALI_CTL_226	0xe2	RW RW RW RW	WRLVL_PERIODIC DFI_PHY_WRLVL_MODE WRLVL_EN WLMRD
DENALI_CTL_227	0xe3	RW RW RW RW	WRLVL_ROTATE WRLVL_AREF_EN WRLVL_RESP_MASK WRLVL_ON_SREF_EXIT
DENALI_CTL_228	0xe4	RW RD RW	WRLVL_NORM_THRESHOLD_F0 WRLVL_ERROR_STATUS WRLVL_CS_MAP
DENALI_CTL_229	0xe5	RW RW	WRLVL_TIMEOUT_F0 WRLVL_HIGH_THRESHOLD_F0
DENALI_CTL_230	0xe6	RW RW	WRLVL_DFI_PROMOTE_THRESH OLD_F0 WRLVL_SW_PROMOTE_THRESH OLD_F0
DENALI_CTL_231	0xe7	RW RW	WRLVL_HIGH_THRESHOLD_F1 WRLVL_NORM_THRESHOLD_F1
DENALI_CTL_232	0xe8	RW RW	WRLVL_SW_PROMOTE_THRESHOLD_ F1 WRLVL_TIMEOUT_F1
DENALI_CTL_233	0xe9	RW RW	WRLVL_NORM_THRESHOLD_F2 WRLVL_DFI_PROMOTE_THRESHOLD_ F1
DENALI_CTL_234	0xea	RW RW	WRLVL_TIMEOUT_F2 WRLVL_HIGH_THRESHOLD_F2
DENALI_CTL_235	0xeb	RW RW	WRLVL_DFI_PROMOTE_THRESHOLD_ F2 WRLVL_SW_PROMOTE_THRESHOLD_ F2
DENALI_CTL_236	0xec	RW RW WR WR	RDLVL_SEQ_EN RDLVL_CS RDLVL_GATE_REQ RDLVL_REQ

Name	Register Address	Access	Controller Parameter(s)
DENALI_CTL_237	0xed	RW RW RW RW	RDLVL_PERIODIC DFI_PHY_RDLVL_GATE_MODE DFI_PHY_RDLVL_MODE RDLVL_GATE_SEQ_EN
DENALI_CTL_238	0xee	RW RW RW RW	RDLVL_AREF_EN RDLVL_GATE_ON_SREF_EXIT RDLVL_GATE_PERIODIC RDLVL_ON_SREF_EXIT
DENALI_CTL_239	0xef	RW RW RW RW	RDLVL_GATE_ROTATE RDLVL_ROTATE RESERVED RDLVL_GATE_AREF_EN
DENALI_CTL_240	0xf0	RW RW RW	RDLVL_NORM_THRESHOLD_F0 RDLVL_GATE_CS_MAP RDLVL_CS_MAP
DENALI_CTL_241	0xf1	RW RW	RDLVL_TIMEOUT_F0 RDLVL_HIGH_THRESHOLD_F0
DENALI_CTL_242	0xf2	RW RW	RDLVL_DFI_PROMOTE_THRESHOLD_F0 RDLVL_SW_PROMOTE_THRESHOLD_F0
DENALI_CTL_243	0xf3	RW RW	RDLVL_GATE_HIGH_THRESHOLD_F0 RDLVL_GATE_NORM_THRESHOLD_F0
DENALI_CTL_244	0xf4	RW RW	RDLVL_GATE_SW_PROMOTE_THRESHOLD_F0 RDLVL_GATE_TIMEOUT_F0
DENALI_CTL_245	0xf5	RW RW	RDLVL_NORM_THRESHOLD_F1 RDLVL_GATE_DFI_PROMOTE_THRES
DENALI_CTL_246	0xf6	RW RW	RDLVL_TIMEOUT_F1 RDLVL_HIGH_THRESHOLD_F1
DENALI_CTL_247	0xf7	RW RW	RDLVL_DFI_PROMOTE_THRESHOLD_F1
DENALI_CTL_248	0xf8	RW RW	RDLVL_GATE_HIGH_THRESHOLD_F1 RDLVL_GATE_NORM_THRESHOLD_F1
DENALI_CTL_249	0xf9	RW RW	RDLVL_GATE_SW_PROMOTE_THRESHOLD_F1 RDLVL_GATE_TIMEOUT_F1
DENALI_CTL_250	0xfa	RW RW	RDLVL_NORM_THRESHOLD_F2 RDLVL_GATE_DFI_PROMOTE_THRESHOLD_F1
DENALI_CTL_251	0xfb	RW RW	RDLVL_TIMEOUT_F2 RDLVL_HIGH_THRESHOLD_F2
DENALI_CTL_252	0xfc	RW RW	RDLVL_DFI_PROMOTE_THRESHOLD_F2 RDLVL_SW_PROMOTE_THRESHOLD_F2

Name	Register Address	Access	Controller Parameter(s)
DENALI_CTL_253	0xfd	RW RW	RDLVL_GATE_HIGH_THRESHOLD_F2 RDLVL_GATE_NORM_THRESHOLD_F2
DENALI_CTL_254	0xfe	RW RW	RDLVL_GATE_SW_PROMOTE_THRESHOLD_F2 RDLVL_GATE_TIMEOUT_F2
DENALI_CTL_255	0xff	RW WR RW	CALVL_CS CALVL_REQ RDLVL_GATE_DFI_PROMOTE_THRESHOLD_F2
DENALI_CTL_256	0x100	RW	CALVL_PAT_0
DENALI_CTL_257	0x101	RW	CALVL_BG_PAT_0
DENALI_CTL_258	0x102	RW	CALVL_PAT_1
DENALI_CTL_259	0x103	RW	CALVL_BG_PAT_1
DENALI_CTL_260	0x104	RW	CALVL_PAT_2
DENALI_CTL_261	0x105	RW	CALVL_BG_PAT_2
DENALI_CTL_262	0x106	RW	CALVL_PAT_3
DENALI_CTL_263	0x107	RW RW	RESERVED CALVL_BG_PAT_3
DENALI_CTL_264	0x108	RW RW RW RW	CALVL_PERIODIC DFI_PHY_CALVL_MODE CALVL_SEQ_EN RESERVED
DENALI_CTL_265	0x109	RW RW RW RW	CALVL_CS_MAP CALVL_ROTATE CALVL_AREF_EN CALVL_ON_SREF_EXIT
DENALI_CTL_266	0x10a	RW RW	CALVL_HIGH_THRESHOLD_F0 CALVL_NORM_THRESHOLD_F0
DENALI_CTL_267	0x10b	RW RW	CALVL_SW_PROMOTE_THRESHOLD_F0 CALVL_TIMEOUT_F0
DENALI_CTL_268	0x10c	RW RW	CALVL_NORM_THRESHOLD_F1 CALVL_DFI_PROMOTE_THRESHOL
DENALI_CTL_269	0x10d	RW RW	CALVL_TIMEOUT_F1 CALVL_HIGH_THRESHOLD_F1
DENALI_CTL_270	0x10e	RW RW	CALVL_DFI_PROMOTE_THRESHOLD_F1
DENALI_CTL_271	0x10f	RW RW	CALVL_HIGH_THRESHOLD_F2
DENALI_CTL_272	0x110	RW RW	CALVL_SW_PROMOTE_THRESHOLD_F2
DENALI_CTL_273	0x111	RD RW RW	CKE_STATUS DENALI0_ALLDATAUSED_ENABLE CALVL_DFI_PROMOTE_THRESHOLD_F2

Name	Register Address	Access	Controller Parameter(s)
DENALI_CTL_274	0x112	RW RW RD	DLL_RST_ADJ_DLY DLL_RST_DELAY MEM_RST_VALID
DENALI_CTL_275	0x113	RW_D RW_D RD RD	TDFI_PHY_RDLAT_F1 TDFI_PHY_RDLAT_F0 UPDATE_ERROR_STATUS TDFI_PHY_WRLAT
DENALI_CTL_276	0x114	RW RW RD RW_D	TDFI_CTRLUPD_MIN DRAM_CLK_DISABLE TDFI_RDDATA_EN TDFI_PHY_RDLAT_F2
DENALI_CTL_277	0x115	RW	TDFI_CTRLUPD_MAX_F0
DENALI_CTL_278	0x116	RW	TDFI_PHYUPD_TYPE0_F0
DENALI_CTL_279	0x117	RW	TDFI_PHYUPD_TYPE1_F0
DENALI_CTL_280	0x118	RW	TDFI_PHYUPD_TYPE2_F0
DENALI_CTL_281	0x119	RW	TDFI_PHYUPD_TYPE3_F0
DENALI_CTL_282	0x11a	RW	TDFI_PHYUPD_RESP_F0
DENALI_CTL_283	0x11b	RW	TDFI_CTRLUPD_INTERVAL_F0
DENALI_CTL_284	0x11c	RW RW RW	TDFI_CTRLUPD_MAX_F1 WRLAT_ADJ_F0 RDLAT_ADJ_F0
DENALI_CTL_285	0x11d	RW	TDFI_PHYUPD_TYPE0_F1
DENALI_CTL_286	0x11e	RW	TDFI_PHYUPD_TYPE1_F1
DENALI_CTL_287	0x11f	RW	TDFI_PHYUPD_TYPE2_F1
DENALI_CTL_288	0x120	RW	TDFI_PHYUPD_TYPE3_F1
DENALI_CTL_289	0x121	RW	TDFI_PHYUPD_RESP_F1
DENALI_CTL_290	0x122	RW	TDFI_CTRLUPD_INTERVAL_F1
DENALI_CTL_291	0x123	RW RW RW	TDFI_CTRLUPD_MAX_F2 WRLAT_ADJ_F1 RDLAT_ADJ_F1
DENALI_CTL_292	0x124	RW	TDFI_PHYUPD_TYPE0_F2
DENALI_CTL_293	0x125	RW	TDFI_PHYUPD_TYPE1_F2
DENALI_CTL_294	0x126	RW	TDFI_PHYUPD_TYPE2_F2
DENALI_CTL_295	0x127	RW	TDFI_PHYUPD_TYPE3_F2
DENALI_CTL_296	0x128	RW	TDFI_PHYUPD_RESP_F2
DENALI_CTL_297	0x129	RW	TDFI_CTRLUPD_INTERVAL_F2
DENALI_CTL_298	0x12a	RW_D RW_D RW RW	TDFI_CTRL_DELAY_F1 TDFI_CTRL_DELAY_F0 WRLAT_ADJ_F2 RDLAT_ADJ_F2

Name	Register Address	Access	Controller Parameter(s)
DENALI_CTL_299	0x12b	RW RW RW RW_D	TDFI_WRLVL_EN TDFI_DRAM_CLK_ENABLE TDFI_DRAM_CLK_DISABLE TDFI_CTRL_DELAY_F2
DENALI_CTL_300	0x12c	RW	TDFI_WRLVL_WW
DENALI_CTL_301	0x12d	RW	TDFI_WRLVL_RESP
DENALI_CTL_302	0x12e	RW	TDFI_WRLVL_MAX
DENALI_CTL_303	0x12f	RW RW	TDFI_RDLVL_RR TDFI_RDLVL_EN
DENALI_CTL_304	0x130	RW	TDFI_RDLVL_RESP
DENALI_CTL_305	0x131	RW RW RW	RDLVL_GATE_EN RDLVL_EN RDLVL_RESP_MASK
DENALI_CTL_306	0x132	RW	TDFI_RDLVL_MAX
DENALI_CTL_307	0x133	RW RD RD	TDFI_CALVL_EN RDLVL_GATE_ERROR_STATUS RDLVL_ERROR_STATUS
DENALI_CTL_308	0x134	RW RW	TDFI_CALVL_CAPTURE_F0 TDFI_CALVL_CC_F0
DENALI_CTL_309	0x135	RW RW	TDFI_CALVL_CAPTURE_F1 TDFI_CALVL_CC_F1
DENALI_CTL_310	0x136	RW RW	TDFI_CALVL_CAPTURE_F2 TDFI_CALVL_CC_F2
DENALI_CTL_311	0x137	RW	TDFI_CALVL_RESP
DENALI_CTL_312	0x138	RW	TDFI_CALVL_MAX
DENALI_CTL_313	0x139	RW RD RW RW	TDFI_PHY_WRDATA CALVL_ERROR_STATUS CALVL_EN CALVL_RESP_MASK
DENALI_CTL_314	0x13a	RW RW RW RW	TDFI_WRCSLAT_F1 TDFI_RDCSLAT_F1 TDFI_WRCSLAT_F0 TDFI_RDCSLAT_F0
DENALI_CTL_315	0x13b	RW RW RW	TDFI_WRDATA_DELAY TDFI_WRCSLAT_F2 TDFI_RDCSLAT_F2
DENALI_CTL_316	0x13c	RW	USER_DEF_REG_0
DENALI_CTL_317	0x13d	RD	USER_DEF_REG_RO_0
DENALI_CTL_318	0x13e	RW	USER_DEF_REG_COPIED_F0_0
DENALI_CTL_319	0x13f	RW	USER_DEF_REG_COPIED_F0_1
DENALI_CTL_320	0x140	RW	USER_DEF_REG_COPIED_F1_0
DENALI_CTL_321	0x141	RW	USER_DEF_REG_COPIED_F1_1
DENALI_CTL_322	0x142	RW	USER_DEF_REG_COPIED_F2_0
DENALI_CTL_323	0x143	RW	USER_DEF_REG_COPIED_F2_1

Name	Register Address	Access	Controller Parameter(s)
DENALI_CTL_324	0x144	RW_D RW_D RW_D RW	MULTI_CHANNEL_ZQ_CAL_MASTER BL_ON_FLY_ENABLE DISABLE_MEMORY_MASKED_WRITE EN_1T_TIMING

Name	Register Address	Type	PHY Parameter(s)
DENALI_PHY_00	PHY_BASE_ADDR + 0	RW	PHY_DQ_DM_SWIZZLE0_0
DENALI_PHY_01	PHY_BASE_ADDR + 1	RW RW	PHY_CLK_WR_BYPASS_SLAVE_DELAY _0 PHY_DQ_DM_SWIZZLE1_0
DENALI_PHY_02	PHY_BASE_ADDR + 2	RW RW RW	PHY_CLK_BYPASS_OVERRIDE_0 PHY_BYPASS_TWO_CYC_PREAMBLE_ 0 PHY_RDDQS_GATE_BYPASS_SLAVE_ DELAY_0
DENALI_PHY_03	PHY_BASE_ADDR + 3	RW RW RW	PHY_SW_WRDQ3_SHIFT_0 PHY_SW_WRDQ2_SHIFT_0 PHY_SW_WRDQ1_SHIFT_0
DENALI_PHY_04	PHY_BASE_ADDR + 4	RW RW RW	PHY_SW_WRDQ7_SHIFT_0 PHY_SW_WRDQ6_SHIFT_0 PHY_SW_WRDQ5_SHIFT_0
DENALI_PHY_05	PHY_BASE_ADDR + 5	RW RW RW	PHY_DQ_TSEL_ENABLE_0 PHY_SW_WRDQS_SHIFT_0 PHY_SW_WRDM_SHIFT_0
DENALI_PHY_06	PHY_BASE_ADDR + 6	RW RW	PHY_DQS_TSEL_ENABLE_0 PHY_DQ_TSEL_SELECT_0
DENALI_PHY_07	PHY_BASE_ADDR + 7	RW+ RW	PHY_TWO_CYC_PREAMBLE_0 PHY_DQS_TSEL_SELECT_0
DENALI_PHY_08	PHY_BASE_ADDR + 8	RW RW_D RW RW	PHY_PER_CS_TRAINING_INDEX_0 PHY_PER_CS_TRAINING_MULTICAST _EN_0 PHY_PER_RANK_CS_MAP_0 PHY_DBI_MODE_0
DENALI_PHY_09	PHY_BASE_ADDR + 9	RW RW RW	PHY_LP4_BOOT_RPTR_UPDATE_0 PHY_LP4_BOOT_RDDATA_EN_TSEL_ DLY_0

Name	Register Address	Type	PHY Parameter(s)
DENALI_PHY_10	PHY_BASE_ADDR + 10	RW RW RW	PHY_SLICE_PWR_RDC_DISABLE_0 PHY_LPBK_CONTROL_0 PHY_LP4_BOOT_RDDQS_LATENCY_ADJUST_0
DENALI_PHY_11	PHY_BASE_ADDR + 11	WR RW RW	SC_PHY_SNAP_OBS_REGS_0 PHY_GATE_ERROR_DELAY_SELECT_0 PHY_RDDQS_DQ_BYPASS_SLAVE_DELAY_0
DENALI_PHY_12	PHY_BASE_ADDR + 12	RW RW RW	PHY_GATE_SMPL1_SLAVE_DELAY_0 PHY_LPDDR_TYPE_0 PHY_LPDDR_0
DENALI_PHY_13	PHY_BASE_ADDR + 13	RW RW	ON_FLY_GATE_ADJUST_EN_0 PHY_GATE_SMPL2_SLAVE_DELAY_0
DENALI_PHY_14	PHY_BASE_ADDR + 14	RD	PHY_GATE_TRACKING_OBS_0
DENALI_PHY_15	PHY_BASE_ADDR + 15	RW RW	PHY_LP4_PST_AMBLE_0 PHY_DFI40_POLARITY_0
DENALI_PHY_16	PHY_BASE_ADDR + 16	RW	PHY_LP4_RDLVL_PATT8_0
DENALI_PHY_17	PHY_BASE_ADDR + 17	RW	PHY_LP4_RDLVL_PATT9_0
DENALI_PHY_18	PHY_BASE_ADDR + 18	RW	PHY_LP4_RDLVL_PATT10_0
DENALI_PHY_19	PHY_BASE_ADDR + 19	RW	PHY_LP4_RDLVL_PATT11_0
DENALI_PHY_20	PHY_BASE_ADDR + 20	RW RW RW	PHY_RDDQ_ENC_OBS_SELECT_0 PHY_MASTER_DLY_LOCK_OBS_SELECT_0
DENALI_PHY_21	PHY_BASE_ADDR + 21	RW RW RW	PHY_FIFO_PTR_OBS_SELECT_0 PHY_WR_SHIFT_OBS_SELECT_0 PHY_WR_ENC_OBS_SELECT_0
DENALI_PHY_22	PHY_BASE_ADDR + 22	RW RW WR	PHY_WRLVL_UPDT_WAIT_CNT_0 PHY_WRLVL_CAPTURE_CNT_0 SC_PHY_LVL_DEBUG_CONT_0
DENALI_PHY_23	PHY_BASE_ADDR + 23	RW RW RW	PHY_RDLVL_UPDT_WAIT_CNT_0 PHY_RDLVL_CAPTURE_CNT_0 PHY_GTLVL_UPDT_WAIT_CNT_0
DENALI_PHY_24	PHY_BASE_ADDR + 24	RW RW RW RW	PHY_WDQLVL_BURST_CNT_0 PHY_RDLVL_DATA_MASK_0 PHY_RDLVL_RDDQS_DQ_OBS_SELECT_0 PHY_RDLVL_OP_MODE_0

Name	Register Address	Type	PHY Parameter(s)
DENALI_PHY_25	PHY_BASE_ADDR + 25	RW RW RW	PHY_WDQLVL_UPDT_WAIT_CNT_0 PHY_WDQLVL_DQDM_SLV_DLY_JUMP_OFFSET_0 PHY_WDQLVL_PATT_0
DENALI_PHY_26	PHY_BASE_ADDR + 26	WR RW RW	SC_PHY_WDQLVL_CLR_PREV_RESULTS_0 PHY_WDQLVL_QTR_DLY_STEP_0 PHY_WDQLVL_DQDM_OBS_SELECT_0
DENALI_PHY_27	PHY_BASE_ADDR + 27	RW	PHY_WDQLVL_DATADM_MASK_0
DENALI_PHY_28	PHY_BASE_ADDR + 28	RW	PHY_USER_PATT0_0
DENALI_PHY_29	PHY_BASE_ADDR + 29	RW	PHY_USER_PATT1_0
DENALI_PHY_30	PHY_BASE_ADDR + 30	RW	PHY_USER_PATT2_0
DENALI_PHY_31	PHY_BASE_ADDR + 31	RW	PHY_USER_PATT3_0
DENALI_PHY_32	PHY_BASE_ADDR + 32	WR RW RW	SC_PHY_MANUAL_CLEAR_0 PHY_CALVL_VREF_DRIVING_SLICE_0 PHY_USER_PATT4_0
DENALI_PHY_33	PHY_BASE_ADDR + 33	RD	PHY_FIFO_PTR_OBS_0
DENALI_PHY_34	PHY_BASE_ADDR + 34	RD	PHY_LPBK_RESULT_OBS_0
DENALI_PHY_35	PHY_BASE_ADDR + 35	RD	PHY_MASTER_DLY_LOCK_OBS_0
DENALI_PHY_36	PHY_BASE_ADDR + 36	RD RD RD RD	PHY_RDDQS_DQ_FALL_ADDER_SLV_DLY_ENC_OBS_0 PHY_RDDQS_DQ_RISE_ADDER_SLV_DLY_ENC_OBS_0 PHY_RDDQS_BASE_SLV_DLY_ENC_OBS_0 PHY_RDDQ_SLV_DLY_ENC_OBS_0
DENALI_PHY_37	PHY_BASE_ADDR + 37	RD RD RD	PHY_WRDQ_BASE_SLV_DLY_ENC_OBS_0 PHY_WRDQS_BASE_SLV_DLY_ENC_OBS_0 PHY_RDDQS_GATE_SLV_DLY_ENC_OBS_0
DENALI_PHY_38	PHY_BASE_ADDR + 38	RD RD	PHY_WRLVL_HARD0_DELAY_OBS_0 PHY_WR_SHIFT_OBS_0

Name	Register Address	Type	PHY Parameter(s)
		RD	PHY_WR_ADDER_SLV_DLY_ENC_OBS_0
DENALI_PHY_39	PHY_BASE_ADDR + 39	RD	PHY_WRLVL_HARD1_DELAY_OBS_0
DENALI_PHY_40	PHY_BASE_ADDR + 40	RD	PHY_WRLVL_STATUS_OBS_0
DENALI_PHY_41	PHY_BASE_ADDR + 41	RD RD	PHY_GATE_SMPL2_SLV_DLY_ENC_OBS_0 PHY_GATE_SMPL1_SLV_DLY_ENC_OBS_0
DENALI_PHY_42	PHY_BASE_ADDR + 42	RD RD	PHY_GTLVL_HARD0_DELAY_OBS_0 PHY_WRLVL_ERROR_OBS_0
DENALI_PHY_43	PHY_BASE_ADDR + 43	RD RD	PHY_GTLVL_STATUS_OBS_0 PHY_GTLVL_HARD1_DELAY_OBS_0
DENALI_PHY_44	PHY_BASE_ADDR + 44	RD RD	PHY_RDLVL_RDDQS_DQ_TE_DLY_OBS_0 PHY_RDLVL_RDDQS_DQ_LE_DLY_OBS_0
DENALI_PHY_45	PHY_BASE_ADDR + 45	RD	PHY_RDLVL_RDDQS_DQ_NUM_WINDOWS_OBS_0
DENALI_PHY_46	PHY_BASE_ADDR + 46	RD	PHY_RDLVL_STATUS_OBS_0
DENALI_PHY_47	PHY_BASE_ADDR + 47	RD RD	PHY_WDQLVL_DQDM_TE_DLY_OBS_0
DENALI_PHY_48	PHY_BASE_ADDR + 48	RD	PHY_WDQLVL_STATUS_OBS_0
DENALI_PHY_49	PHY_BASE_ADDR + 49	RW	PHY_DDL_MODE_0
DENALI_PHY_50	PHY_BASE_ADDR + 50	RD	PHY_DDL_TEST_OBS_0
DENALI_PHY_51	PHY_BASE_ADDR + 51	RD	PHY_DDL_TEST_MSTR_DLY_OBS_0
DENALI_PHY_52	PHY_BASE_ADDR + 52	RW RW WR	PHY_RX_CAL_SAMPLE_WAIT_0 PHY_RX_CAL_OVERRIDE_0 SC_PHY_RX_CAL_START_0
DENALI_PHY_53	PHY_BASE_ADDR + 53	RW+ RW+	PHY_RX_CAL_DQ1_0 PHY_RX_CAL_DQ0_0
DENALI_PHY_54	PHY_BASE_ADDR + 54	RW+ RW+	PHY_RX_CAL_DQ3_0 PHY_RX_CAL_DQ2_0
DENALI_PHY_55	PHY_BASE_ADDR + 55	RW+ RW+	PHY_RX_CAL_DQ5_0 PHY_RX_CAL_DQ4_0
DENALI_PHY_56	PHY_BASE_ADDR + 56	RW+ RW+	PHY_RX_CAL_DQ7_0 PHY_RX_CAL_DQ6_0

Name	Register Address	Type	PHY Parameter(s)
DENALI_PHY_57	PHY_BASE_ADDR + 57	RW+ RW+	PHY_RX_CAL_DQS_0 PHY_RX_CAL_DM_0
DENALI_PHY_58	PHY_BASE_ADDR + 58	RD RW+	PHY_RX_CAL_OBS_0 PHY_RX_CAL_FDBK_0
DENALI_PHY_59	PHY_BASE_ADDR + 59	RW+ RW+	PHY_CLK_WRDQ1_SLAVE_DELAY_0 PHY_CLK_WRDQ0_SLAVE_DELAY_0
DENALI_PHY_60	PHY_BASE_ADDR + 60	RW+ RW+	PHY_CLK_WRDQ3_SLAVE_DELAY_0 PHY_CLK_WRDQ2_SLAVE_DELAY_0
DENALI_PHY_61	PHY_BASE_ADDR + 61	RW+ RW+	PHY_CLK_WRDQ5_SLAVE_DELAY_0 PHY_CLK_WRDQ4_SLAVE_DELAY_0
DENALI_PHY_62	PHY_BASE_ADDR + 62	RW+ RW+	PHY_CLK_WRDQ7_SLAVE_DELAY_0 PHY_CLK_WRDQ6_SLAVE_DELAY_0
DENALI_PHY_63	PHY_BASE_ADDR + 63	RW+ RW+	PHY_CLK_WRDQS_SLAVE_DELAY_0 PHY_CLK_WRDM_SLAVE_DELAY_0
DENALI_PHY_64	PHY_BASE_ADDR + 64	RW+ RW+	PHY_RDDQ1_SLAVE_DELAY_0 PHY_RDDQ0_SLAVE_DELAY_0
DENALI_PHY_65	PHY_BASE_ADDR + 65	RW+ RW+	PHY_RDDQ3_SLAVE_DELAY_0 PHY_RDDQ2_SLAVE_DELAY_0
DENALI_PHY_66	PHY_BASE_ADDR + 66	RW+ RW+	PHY_RDDQ5_SLAVE_DELAY_0 PHY_RDDQ4_SLAVE_DELAY_0
DENALI_PHY_67	PHY_BASE_ADDR + 67	RW+ RW+	PHY_RDDQ7_SLAVE_DELAY_0 PHY_RDDQ6_SLAVE_DELAY_0
DENALI_PHY_68	PHY_BASE_ADDR + 68	RW+ RW+	PHY_RDDQS_DQ0_RISE_SLAVE_DEL AY_0 PHY_RDDM_SLAVE_DELAY_0
DENALI_PHY_69	PHY_BASE_ADDR + 69	RW+ RW+	PHY_RDDQS_DQ1_RISE_SLAVE_DEL AY_0 PHY_RDDQS_DQ0_FALL_SLAVE_DELAY _0
DENALI_PHY_70	PHY_BASE_ADDR + 70	RW+ RW+	PHY_RDDQS_DQ2_RISE_SLAVE_DEL AY_0 PHY_RDDQS_DQ1_FALL_SLAVE_DELAY _0
DENALI_PHY_71	PHY_BASE_ADDR + 71	RW+ RW+	PHY_RDDQS_DQ3_RISE_SLAVE_DEL AY_0

Name	Register Address	Type	PHY Parameter(s)
			PHY_RDDQS_DQ2_FALL_SLAVE_DELAY_0
DENALI_PHY_72	PHY_BASE_ADDR + 72	RW+ RW+	PHY_RDDQS_DQ4_RISE_SLAVE_DELAY_0 PHY_RDDQS_DQ3_FALL_SLAVE_DELAY_0
DENALI_PHY_73	PHY_BASE_ADDR + 73	RW+ RW+	PHY_RDDQS_DQ5_RISE_SLAVE_DELAY_0 PHY_RDDQS_DQ4_FALL_SLAVE_DELAY_0
DENALI_PHY_74	PHY_BASE_ADDR + 74	RW+ RW+	PHY_RDDQS_DQ6_RISE_SLAVE_DELAY_0 PHY_RDDQS_DQ5_FALL_SLAVE_DELAY_0
DENALI_PHY_75	PHY_BASE_ADDR + 75	RW+ RW+	PHY_RDDQS_DQ7_RISE_SLAVE_DELAY_0 PHY_RDDQS_DQ6_FALL_SLAVE_DELAY_0
DENALI_PHY_76	PHY_BASE_ADDR + 76	RW+ RW+	PHY_RDDQS_DM_RISE_SLAVE_DELAY_0 PHY_RDDQS_DQ7_FALL_SLAVE_DELAY_0
DENALI_PHY_77	PHY_BASE_ADDR + 77	RW+ RW+	PHY_RDDQS_GATE_SLAVE_DELAY_0 PHY_RDDQS_DM_FALL_SLAVE_DELAY_0
DENALI_PHY_78	PHY_BASE_ADDR + 78	RW+ RW+ RW+	PHY_WRLVL_DELAY_EARLY_THRESHOLD_0 PHY_WRITE_PATH_LAT_ADD_0 PHY_RDDQS_LATENCY_ADJUST_0
DENALI_PHY_79	PHY_BASE_ADDR + 79	RW+ RW+	PHY_WRLVL_EARLY_FORCE_ZERO_0 PHY_WRLVL_DELAY_PERIOD_THRESHOLD_0
DENALI_PHY_80	PHY_BASE_ADDR + 80	RW+ RW+	PHY_GTLVL_LAT_ADJ_START_0 PHY_GTLVL_RDDQS_SLV_DLY_START_0

Name	Register Address	Type	PHY Parameter(s)
DENALI_PHY_81	PHY_BASE_ADDR + 81	RW+ RW+	PHY_RDLVL_RDDQS_DQ_SLV_DLY_START_0 PHY_WDQLVL_DQDM_SLV_DLY_START_0
DENALI_PHY_82	PHY_BASE_ADDR + 82	RW	RESERVED
DENALI_PHY_83	PHY_BASE_ADDR + 83	RW+ RW+ RW+	PHY_DQS_OE_TIMING_0 PHY_DQ_TSEL_WR_TIMING_0 PHY_DQ_TSEL_RD_TIMING_0
DENALI_PHY_84	PHY_BASE_ADDR + 84	RW+ RW+ RW+	PHY_DQ_IE_TIMING_0 PHY_PER_CS_TRAINING_EN_0 PHY_DQS_TSEL_WR_TIMING_0
DENALI_PHY_85	PHY_BASE_ADDR + 85	RW+ RW+ RW+	PHY_RDDATA_EN_DLY_0 PHY_IE_MODE_0 PHY_RDDATA_EN_IE_DLY_0
DENALI_PHY_86	PHY_BASE_ADDR + 86	RW+ RW+ RW+	PHY_MASTER_DELAY_START_0 PHY_SW_MASTER_MODE_0 PHY_RDDATA_EN_TSEL_DLY_0
DENALI_PHY_87	PHY_BASE_ADDR + 87	RW+ RW+ RW+	PHY_WRLVL_DLY_STEP_0 PHY_RPTR_UPDATE_0 PHY_MASTER_DELAY_WAIT_0
DENALI_PHY_88	PHY_BASE_ADDR + 88	RW+ RW+ RW+	PHY_GTLVL_RESP_WAIT_CNT_0 PHY_GTLVL_DLY_STEP_0 PHY_WRLVL_RESP_WAIT_CNT_0
DENALI_PHY_89	PHY_BASE_ADDR + 89	RW+ RW+	PHY_GTLVL_FINAL_STEP_0 PHY_GTLVL_BACK_STEP_0
DENALI_PHY_90	PHY_BASE_ADDR + 90	RW+ RW+	PHY_RDLVL_DLY_STEP_0 PHY_WDQLVL_DLY_STEP_0
DENALI_PHY_128	PHY_BASE_ADDR + 128	RW	PHY_DQ_DM_SWIZZLE0_1
DENALI_PHY_129	PHY_BASE_ADDR + 129	RW RW	PHY_CLK_WR_BYPASS_SLAVE_DELAY_1 PHY_DQ_DM_SWIZZLE1_1
DENALI_PHY_130	PHY_BASE_ADDR + 130	RW RW RW	PHY_CLK_BYPASS_OVERRIDE_1 PHY_BYPASS_TWO_CYC_PREAMBLE_1 PHY_RDDQS_GATE_BYPASS_SLAVE_DELAY_1

Name	Register Address	Type	PHY Parameter(s)
DENALI_PHY_131	PHY_BASE_ADDR + 131	RW RW RW	PHY_SW_WRDQ3_SHIFT_1 PHY_SW_WRDQ2_SHIFT_1 PHY_SW_WRDQ1_SHIFT_1
DENALI_PHY_132	PHY_BASE_ADDR + 132	RW RW RW	PHY_SW_WRDQ7_SHIFT_1 PHY_SW_WRDQ6_SHIFT_1 PHY_SW_WRDQ5_SHIFT_1
DENALI_PHY_133	PHY_BASE_ADDR + 133	RW RW RW	PHY_DQ_TSEL_ENABLE_1 PHY_SW_WRDQS_SHIFT_1 PHY_SW_WRDM_SHIFT_1
DENALI_PHY_134	PHY_BASE_ADDR + 134	RW RW	PHY_DQS_TSEL_ENABLE_1 PHY_DQ_TSEL_SELECT_1
DENALI_PHY_135	PHY_BASE_ADDR + 135	RW+	PHY_TWO_CYC_PREAMBLE_1
DENALI_PHY_136	PHY_BASE_ADDR + 136	RW RW_D RW	PHY_PER_CS_TRAINING_INDEX_1 PHY_PER_CS_TRAINING_MULTICAST _EN_1 PHY_PER_RANK_CS_MAP_1
DENALI_PHY_137	PHY_BASE_ADDR + 137	RW RW RW	PHY_LP4_BOOT_RPTR_UPDATE_1 PHY_LP4_BOOT_RDDATA_EN_TSEL_ DLY_1
DENALI_PHY_138	PHY_BASE_ADDR + 138	RW RW RW	PHY_SLICE_PWR_RDC_DISABLE_1 PHY_LPBK_CONTROL_1 PHY_LP4_BOOT_RDDQS_LATENCY_A DJUST_1
DENALI_PHY_139	PHY_BASE_ADDR + 139	WR RW RW	SC_PHY_SNAP_OBS_REGS_1 PHY_GATE_ERROR_DELAY_SELECT_ 1 PHY_RDDQS_DQ_BYPASS_SLAVE_DE LAY_1
DENALI_PHY_140	PHY_BASE_ADDR + 140	RW RW RW	PHY_GATE_SMPL1_SLAVE_DELAY_1 PHY_LPDDR_TYPE_1 PHY_LPDDR_1
DENALI_PHY_141	PHY_BASE_ADDR + 141	RW RW	ON_FLY_GATE_ADJUST_EN_1 PHY_GATE_SMPL2_SLAVE_DELAY_1
DENALI_PHY_142	PHY_BASE_ADDR + 142	RD	PHY_GATE_TRACKING_OBS_1
DENALI_PHY_143	PHY_BASE_ADDR + 143	RW RW	PHY_LP4_PST_AMBLE_1 PHY_RET2_RCLADJTM_1
DENALI_PHY_144	PHY_BASE_ADDR + 144	RW	PHY_LP4_RDLVL_PATT8_1
DENALI_PHY_145	PHY_BASE_ADDR + 145	RW	PHY_LP4_RDLVL_PATT9_1

Name	Register Address	Type	PHY Parameter(s)
DENALI_PHY_146	PHY_BASE_ADDR + 146	RW	PHY_LP4_RDLVL_PATT10_1
DENALI_PHY_147	PHY_BASE_ADDR + 147	RW	PHY_LP4_RDLVL_PATT11_1
DENALI_PHY_148	PHY_BASE_ADDR + 148	RW RW RW	PHY_RDDQ_ENC_OBS_SELECT_1 PHY_MASTER_DLY_LOCK_OBS_SELE CT_1
DENALI_PHY_149	PHY_BASE_ADDR + 149	RW RW RW	PHY_FIFO_PTR_OBS_SELECT_1 PHY_WR_SHIFT_OBS_SELECT_1 PHY_WR_ENC_OBS_SELECT_1
DENALI_PHY_150	PHY_BASE_ADDR + 150	RW RW WR	PHY_WRLVL_UPDT_WAIT_CNT_1 PHY_WRLVL_CAPTURE_CNT_1 SC_PHY_LVL_DEBUG_CONT_1
DENALI_PHY_151	PHY_BASE_ADDR + 151	RW RW RW	PHY_RDLVL_UPDT_WAIT_CNT_1 PHY_RDLVL_CAPTURE_CNT_1 PHY_GTLVL_UPDT_WAIT_CNT_1
DENALI_PHY_152	PHY_BASE_ADDR + 152	RW RW RW	PHY_WDQLVL_BURST_CNT_1 PHY_RDLVL_DATA_MASK_1 PHY_RDLVL_RDDQS_DQ_OBS_SELEC
DENALI_PHY_153	PHY_BASE_ADDR + 153	RW RW RW	PHY_WDQLVL_UPDT_WAIT_CNT_1 PHY_WDQLVL_DQDM_SLV_DLY_JUMP_ OFFSET_1 PHY_WDQLVL_PATT_1
DENALI_PHY_154	PHY_BASE_ADDR + 154	WR RW RW	SC_PHY_WDQLVL_CLR_PREV_RESUL TS_1 PHY_WDQLVL_QTR_DLY_STEP_1 PHY_WDQLVL_DQDM_OBS_SELECT_ 1
DENALI_PHY_155	PHY_BASE_ADDR + 155	RW	PHY_WDQLVL_DATADM_MASK_1
DENALI_PHY_156	PHY_BASE_ADDR + 156	RW	PHY_USER_PATT0_1
DENALI_PHY_157	PHY_BASE_ADDR + 157	RW	PHY_USER_PATT1_1
DENALI_PHY_158	PHY_BASE_ADDR + 158	RW	PHY_USER_PATT2_1
DENALI_PHY_159	PHY_BASE_ADDR + 159	RW	PHY_USER_PATT3_1
DENALI_PHY_160	PHY_BASE_ADDR + 160	WR RW RW	SC_PHY_MANUAL_CLEAR_1 PHY_CALVL_VREF_DRIVING_SLICE_1 PHY_USER_PATT4_1
DENALI_PHY_161	PHY_BASE_ADDR + 161	RD	PHY_FIFO_PTR_OBS_1
DENALI_PHY_162	PHY_BASE_ADDR + 162	RD	PHY_LPBK_RESULT_OBS_1
DENALI_PHY_163	PHY_BASE_ADDR + 163	RD RD	PHY_MASTER_DLY_LOCK_OBS_1 PHY_LPBK_ERROR_COUNT_OBS_1

Name	Register Address	Type	PHY Parameter(s)
DENALI_PHY_164	PHY_BASE_ADDR + 164	RD RD RD RD	PHY_RDDQS_DQ_FALL_ADDER_SLV_DLY_ENC_OBS_1 PHY_RDDQS_DQ_RISE_ADDER_SLV_DLY_ENC_OBS_1 PHY_RDDQS_BASE_SLV_DLY_ENC_OBS_1 PHY_RDDQ_SLV_DLY_ENC_OBS_1
DENALI_PHY_165	PHY_BASE_ADDR + 165	RD RD RD	PHY_WRDQ_BASE_SLV_DLY_ENC_OBS_1 PHY_WRDQS_BASE_SLV_DLY_ENC_OBS_1 PHY_RDDQS_GATE_SLV_DLY_ENC_OBS_1
DENALI_PHY_166	PHY_BASE_ADDR + 166	RD RD RD	PHY_WRLVL_HARD0_DELAY_OBS_1 PHY_WR_SHIFT_OBS_1 PHY_WR_ADDER_SLV_DLY_ENC_OBS_1
DENALI_PHY_167	PHY_BASE_ADDR + 167	RD	PHY_WRLVL_HARD1_DELAY_OBS_1
DENALI_PHY_168	PHY_BASE_ADDR + 168	RD	PHY_WRLVL_STATUS_OBS_1
DENALI_PHY_169	PHY_BASE_ADDR + 169	RD RD	PHY_GATE_SMPL2_SLV_DLY_ENC_OBS_1 PHY_GATE_SMPL1_SLV_DLY_ENC_OBS_1
DENALI_PHY_170	PHY_BASE_ADDR + 170	RD RD	PHY_GTLVL_HARD0_DELAY_OBS_1 PHY_WRLVL_ERROR_OBS_1
DENALI_PHY_171	PHY_BASE_ADDR + 171	RD RD	PHY_GTLVL_STATUS_OBS_1 PHY_GTLVL_HARD1_DELAY_OBS_1
DENALI_PHY_172	PHY_BASE_ADDR + 172	RD RD	PHY_RDLVL_RDDQS_DQ_TE_DLY_OBS_1 PHY_RDLVL_RDDQS_DQ_LE_DLY_OBS_1
DENALI_PHY_173	PHY_BASE_ADDR + 173	RD	PHY_RDLVL_RDDQS_DQ_NUM_WINDOWS_OBS_1
DENALI_PHY_174	PHY_BASE_ADDR + 174	RD	PHY_RDLVL_STATUS_OBS_1
DENALI_PHY_175	PHY_BASE_ADDR + 175	RD RD	PHY_WDQLVL_DQDM_TE_DLY_OBS_1 PHY_WDQLVL_DQDM_LE_DLY_OBS_1
DENALI_PHY_176	PHY_BASE_ADDR + 176	RD	PHY_WDQLVL_STATUS_OBS_1
DENALI_PHY_177	PHY_BASE_ADDR + 177	RW	PHY_DDL_MODE_1

Name	Register Address	Type	PHY Parameter(s)
DENALI_PHY_178	PHY_BASE_ADDR + 178	RD	PHY_DDL_TEST_OBS_1
DENALI_PHY_179	PHY_BASE_ADDR + 179	RD	PHY_DDL_TEST_MSTR_DLY_OBS_1
DENALI_PHY_180	PHY_BASE_ADDR + 180	RW RW WR	PHY_RX_CAL_SAMPLE_WAIT_1 PHY_RX_CAL_OVERRIDE_1 SC_PHY_RX_CAL_START_1
DENALI_PHY_181	PHY_BASE_ADDR + 181	RW+ RW+	PHY_RX_CAL_DQ1_1 PHY_RX_CAL_DQ0_1
DENALI_PHY_182	PHY_BASE_ADDR + 182	RW+ RW+	PHY_RX_CAL_DQ3_1 PHY_RX_CAL_DQ2_1
DENALI_PHY_183	PHY_BASE_ADDR + 183	RW+ RW+	PHY_RX_CAL_DQ5_1 PHY_RX_CAL_DQ4_1
DENALI_PHY_184	PHY_BASE_ADDR + 184	RW+ RW+	PHY_RX_CAL_DQ7_1 PHY_RX_CAL_DQ6_1
DENALI_PHY_185	PHY_BASE_ADDR + 185	RW+ RW+	PHY_RX_CAL_DQS_1 PHY_RX_CAL_DM_1
DENALI_PHY_186	PHY_BASE_ADDR + 186	RD RW+	PHY_RX_CAL_OBS_1 PHY_RX_CAL_FDBK_1
DENALI_PHY_187	PHY_BASE_ADDR + 187	RW+ RW+	PHY_CLK_WRDQ1_SLAVE_DELAY_1 PHY_CLK_WRDQ0_SLAVE_DELAY_1
DENALI_PHY_188	PHY_BASE_ADDR + 188	RW+ RW+	PHY_CLK_WRDQ3_SLAVE_DELAY_1 PHY_CLK_WRDQ2_SLAVE_DELAY_1
DENALI_PHY_189	PHY_BASE_ADDR + 189	RW+ RW+	PHY_CLK_WRDQ5_SLAVE_DELAY_1 PHY_CLK_WRDQ4_SLAVE_DELAY_1
DENALI_PHY_190	PHY_BASE_ADDR + 190	RW+ RW+	PHY_CLK_WRDQ7_SLAVE_DELAY_1 PHY_CLK_WRDQ6_SLAVE_DELAY_1
DENALI_PHY_191	PHY_BASE_ADDR + 191	RW+ RW+	PHY_CLK_WRDQS_SLAVE_DELAY_1 PHY_CLK_WRDM_SLAVE_DELAY_1
DENALI_PHY_192	PHY_BASE_ADDR + 192	RW+ RW+	PHY_RDDQ1_SLAVE_DELAY_1 PHY_RDDQ0_SLAVE_DELAY_1
DENALI_PHY_193	PHY_BASE_ADDR + 193	RW+ RW+	PHY_RDDQ3_SLAVE_DELAY_1 PHY_RDDQ2_SLAVE_DELAY_1
DENALI_PHY_194	PHY_BASE_ADDR + 194	RW+ RW+	PHY_RDDQ5_SLAVE_DELAY_1 PHY_RDDQ4_SLAVE_DELAY_1
DENALI_PHY_195	PHY_BASE_ADDR + 195	RW+ RW+	PHY_RDDQ7_SLAVE_DELAY_1 PHY_RDDQ6_SLAVE_DELAY_1

Name	Register Address	Type	PHY Parameter(s)
DENALI_PHY_196	PHY_BASE_ADDR + 196	RW+ RW+	PHY_RDDQS_DQ0_RISE_SLAVE_DELAY_1 PHY_RDDM_SLAVE_DELAY_1
DENALI_PHY_197	PHY_BASE_ADDR + 197	RW+ RW+	PHY_RDDQS_DQ1_RISE_SLAVE_DELAY_1 PHY_RDDQS_DQ0_FALL_SLAVE_DELAY_1
DENALI_PHY_198	PHY_BASE_ADDR + 198	RW+ RW+	PHY_RDDQS_DQ2_RISE_SLAVE_DELAY_1 PHY_RDDQS_DQ1_FALL_SLAVE_DELAY_1
DENALI_PHY_199	PHY_BASE_ADDR + 199	RW+ RW+	PHY_RDDQS_DQ3_RISE_SLAVE_DELAY_1 PHY_RDDQS_DQ2_FALL_SLAVE_DELAY_1
DENALI_PHY_200	PHY_BASE_ADDR + 200	RW+ RW+	PHY_RDDQS_DQ4_RISE_SLAVE_DELAY_1 PHY_RDDQS_DQ3_FALL_SLAVE_DELAY_1
DENALI_PHY_201	PHY_BASE_ADDR + 201	RW+ RW+	PHY_RDDQS_DQ5_RISE_SLAVE_DELAY_1 PHY_RDDQS_DQ4_FALL_SLAVE_DELAY_1
DENALI_PHY_202	PHY_BASE_ADDR + 202	RW+ RW+	PHY_RDDQS_DQ6_RISE_SLAVE_DELAY_1 PHY_RDDQS_DQ5_FALL_SLAVE_DELAY_1
DENALI_PHY_203	PHY_BASE_ADDR + 203	RW+ RW+	PHY_RDDQS_DQ7_RISE_SLAVE_DELAY_1 PHY_RDDQS_DQ6_FALL_SLAVE_DELAY_1
DENALI_PHY_204	PHY_BASE_ADDR + 204	RW+ RW+	PHY_RDDQS_DM_RISE_SLAVE_DELAY_ PHY_RDDQS_DQ7_FALL_SLAVE_DELAY_1
DENALI_PHY_205	PHY_BASE_ADDR + 205	RW+ RW+	PHY_RDDQS_GATE_SLAVE_DELAY_1 PHY_RDDQS_DM_FALL_SLAVE_DELAY_

Name	Register Address	Type	PHY Parameter(s)
DENALI_PHY_206	PHY_BASE_ADDR + 206	RW+ RW+ RW+	PHY_WRLVL_DELAY_EARLY_THRESHOLI _1 PHY_WRITE_PATH_LAT_ADD_1 PHY_RDDQS_LATENCY_ADJUST_1
DENALI_PHY_207	PHY_BASE_ADDR + 207	RW+ RW+	PHY_WRLVL_EARLY_FORCE_ZERO_1 PHY_WRLVL_DELAY_PERIOD_THRESHO D_1
DENALI_PHY_208	PHY_BASE_ADDR + 208	RW+ RW+	PHY_GTLVL_LAT_ADJ_START_1 PHY_GTLVL_RDDQS_SLV_DLY_START_1
DENALI_PHY_209	PHY_BASE_ADDR + 209	RW+ RW+	PHY_RDLVL_RDDQS_DQ_SLV_DLY_STA RT_1 PHY_WDQLVL_DQDM_SLV_DLY_START_ 1
DENALI_PHY_210	PHY_BASE_ADDR + 210	RW	RESERVED
DENALI_PHY_211	PHY_BASE_ADDR + 211	RW+ RW+ RW+	PHY_DQS_OE_TIMING_1 PHY_DQ_TSEL_WR_TIMING_1 PHY_DQ_TSEL_RD_TIMING_1
DENALI_PHY_212	PHY_BASE_ADDR + 212	RW+ RW+ RW+	PHY_DQ_IE_TIMING_1 PHY_PER_CS_TRAINING_EN_1 PHY_DQS_TSEL_WR_TIMING_1
DENALI_PHY_213	PHY_BASE_ADDR + 213	RW+ RW+ RW+	PHY_RDDATA_EN_DLY_1 PHY_IE_MODE_1 PHY_RDDATA_EN_IE_DLY_1
DENALI_PHY_214	PHY_BASE_ADDR + 214	RW+ RW+ RW+	PHY_MASTER_DELAY_START_1 PHY_SW_MASTER_MODE_1 PHY_RDDATA_EN_TSEL_DLY_1
DENALI_PHY_215	PHY_BASE_ADDR + 215	RW+ RW+ RW+	PHY_WRLVL_DLY_STEP_1 PHY_RPTR_UPDATE_1 PHY_MASTER_DELAY_WAIT_1
DENALI_PHY_216	PHY_BASE_ADDR + 216	RW+ RW+ RW+	PHY_GTLVL_RESP_WAIT_CNT_1 PHY_GTLVL_DLY_STEP_1 PHY_WRLVL_RESP_WAIT_CNT_1
DENALI_PHY_217	PHY_BASE_ADDR + 217	RW+ RW+	PHY_GTLVL_FINAL_STEP_1 PHY_GTLVL_BACK_STEP_1
DENALI_PHY_218	PHY_BASE_ADDR + 218	RW+ RW+	PHY_RDLVL_DLY_STEP_1 PHY_WDQLVL_DLY_STEP_1
DENALI_PHY_256	PHY_BASE_ADDR + 256	RW	PHY_DQ_DM_SWIZZLE0_2

Name	Register Address	Type	PHY Parameter(s)
DENALI_PHY_257	PHY_BASE_ADDR + 257	RW RW	PHY_CLK_WR_BYPASS_SLAVE_DELAY_ 2 PHY_DQ_DM_SWIZZLE1_2
DENALI_PHY_258	PHY_BASE_ADDR + 258	RW RW RW	PHY_CLK_BYPASS_OVERRIDE_2 PHY_BYPASS_TWO_CYC_PREAMBLE_2 PHY_RDDQS_GATE_BYPASS_SLAVE_DE LAY_2
DENALI_PHY_259	PHY_BASE_ADDR + 259	RW RW RW	PHY_SW_WRDQ3_SHIFT_2 PHY_SW_WRDQ2_SHIFT_2 PHY_SW_WRDQ1_SHIFT_2
DENALI_PHY_260	PHY_BASE_ADDR + 260	RW RW RW	PHY_SW_WRDQ7_SHIFT_2 PHY_SW_WRDQ6_SHIFT_2 PHY_SW_WRDQ5_SHIFT_2
DENALI_PHY_261	PHY_BASE_ADDR + 261	RW RW RW	PHY_DQ_TSEL_ENABLE_2 PHY_SW_WRDQS_SHIFT_2 PHY_SW_WRDM_SHIFT_2
DENALI_PHY_262	PHY_BASE_ADDR + 262	RW RW	PHY_DQS_TSEL_ENABLE_2 PHY_DQ_TSEL_SELECT_2
DENALI_PHY_263	PHY_BASE_ADDR + 263	RW+ RW	PHY_TWO_CYC_PREAMBLE_2 PHY_DQS_TSEL_SELECT_2
DENALI_PHY_264	PHY_BASE_ADDR + 264	RW RW_D RW	PHY_PER_CS_TRAINING_INDEX_2 PHY_PER_CS_TRAINING_MULTICAST_E N_2 PHY_PER_RANK_CS_MAP_2
DENALI_PHY_265	PHY_BASE_ADDR + 265	RW RW RW RW	PHY_LP4_BOOT_RPTR_UPDATE_2 PHY_LP4_BOOT_RDDATA_EN_TSEL_DL Y_2 PHY_LP4_BOOT_RDDATA_EN_DLY_2 PHY_LP4_BOOT_RDDATA_EN_IE_DLY_ 2
DENALI_PHY_266	PHY_BASE_ADDR + 266	RW RW RW	PHY_SLICE_PWR_RDC_DISABLE_2 PHY_LPBK_CONTROL_2 PHY_LP4_BOOT_RDDQS_LATENCY_ADJ UST_2
DENALI_PHY_267	PHY_BASE_ADDR + 267	WR RW RW	SC_PHY_SNAP_OBS_REGS_2 PHY_GATE_ERROR_DELAY_SELECT_2 PHY_RDDQS_DQ_BYPASS_SLAVE_DEL AY_2

Name	Register Address	Type	PHY Parameter(s)
DENALI_PHY_268	PHY_BASE_ADDR + 268	RW RW RW	PHY_GATE_SMPL1_SLAVE_DELAY_2 PHY_LPDDR_TYPE_2 PHY_LPDDR_2
DENALI_PHY_269	PHY_BASE_ADDR + 269	RW RW	ON_FLY_GATE_ADJUST_EN_2 PHY_GATE_SMPL2_SLAVE_DELAY_2
DENALI_PHY_270	PHY_BASE_ADDR + 270	RD	PHY_GATE_TRACKING_OBS_2
DENALI_PHY_271	PHY_BASE_ADDR + 271	RW RW	PHY_LP4_PST_AMBLE_2 PHY_DFI40_POLARITY_2
DENALI_PHY_272	PHY_BASE_ADDR + 272	RW	PHY_LP4_RDLVL_PATT8_2
DENALI_PHY_273	PHY_BASE_ADDR + 273	RW	PHY_LP4_RDLVL_PATT9_2
DENALI_PHY_274	PHY_BASE_ADDR + 274	RW	PHY_LP4_RDLVL_PATT10_2
DENALI_PHY_275	PHY_BASE_ADDR + 275	RW	PHY_LP4_RDLVL_PATT11_2
DENALI_PHY_276	PHY_BASE_ADDR + 276	RW RW RW	PHY_RDDQ_ENC_OBS_SELECT_2 PHY_MASTER_DLY_LOCK_OBS_SELECT _2
DENALI_PHY_277	PHY_BASE_ADDR + 277	RW RW RW	PHY_FIFO_PTR_OBS_SELECT_2 PHY_WR_SHIFT_OBS_SELECT_2 PHY_WR_ENC_OBS_SELECT_2
DENALI_PHY_278	PHY_BASE_ADDR + 278	RW RW WR	PHY_WRLVL_UPDT_WAIT_CNT_2 PHY_WRLVL_CAPTURE_CNT_2 SC_PHY_LVL_DEBUG_CONT_2
DENALI_PHY_279	PHY_BASE_ADDR + 279	RW RW RW	PHY_RDLVL_UPDT_WAIT_CNT_2 PHY_RDLVL_CAPTURE_CNT_2 PHY_GTLVL_UPDT_WAIT_CNT_2
DENALI_PHY_280	PHY_BASE_ADDR + 280	RW RW RW RW	PHY_WDQLVL_BURST_CNT_2 PHY_RDLVL_DATA_MASK_2 PHY_RDLVL_RDDQS_DQ_OBS_SELECT _2 PHY_RDLVL_OP_MODE_2
DENALI_PHY_281	PHY_BASE_ADDR + 281	RW RW RW	PHY_WDQLVL_UPDT_WAIT_CNT_2 PHY_WDQLVL_DQDM_SLV_DLY_JUMP_OF FSET_2 PHY_WDQLVL_PATT_2
DENALI_PHY_282	PHY_BASE_ADDR + 282	WR RW RW	SC_PHY_WDQLVL_CLR_PREV_RESULTS _2 PHY_WDQLVL_QTR_DLY_STEP_2 PHY_WDQLVL_DQDM_OBS_SELECT_2
DENALI_PHY_283	PHY_BASE_ADDR + 283	RW	PHY_WDQLVL_DATADM_MASK_2
DENALI_PHY_284	PHY_BASE_ADDR + 284	RW	PHY_USER_PATT0_2
DENALI_PHY_285	PHY_BASE_ADDR + 285	RW	PHY_USER_PATT1_2
DENALI_PHY_286	PHY_BASE_ADDR + 286	RW	PHY_USER_PATT2_2

Name	Register Address	Type	PHY Parameter(s)
DENALI_PHY_287	PHY_BASE_ADDR + 287	RW	PHY_USER_PATT3_2
DENALI_PHY_288	PHY_BASE_ADDR + 288	WR RW RW	SC_PHY_MANUAL_CLEAR_2 PHY_CALVL_VREF_DRIVING_SLICE_2 PHY_USER_PATT4_2
DENALI_PHY_289	PHY_BASE_ADDR + 289	RD	PHY_FIFO_PTR_OBS_2
DENALI_PHY_290	PHY_BASE_ADDR + 290	RD	PHY_LPBK_RESULT_OBS_2
DENALI_PHY_291	PHY_BASE_ADDR + 291	RD RD	PHY_MASTER_DLY_LOCK_OBS_2 PHY_LPBK_ERROR_COUNT_OBS_2
DENALI_PHY_292	PHY_BASE_ADDR + 292	RD RD RD RD	PHY_RDDQS_DQ_FALL_ADDER_SLV_DLY_ENC_OBS_2 PHY_RDDQS_DQ_RISE_ADDER_SLV_DLY_ENC_OBS_2 PHY_RDDQS_BASE_SLV_DLY_ENC_OBS_2 PHY_RDDQ_SLV_DLY_ENC_OBS_2
DENALI_PHY_293	PHY_BASE_ADDR + 293	RD RD RD	PHY_WRDQ_BASE_SLV_DLY_ENC_OBS_2 PHY_WRDQS_BASE_SLV_DLY_ENC_OBS_2 PHY_RDDQS_GATE_SLV_DLY_ENC_OBS_2
DENALI_PHY_294	PHY_BASE_ADDR + 294	RD RD RD	PHY_WRLVL_HARD0_DELAY_OBS_2 PHY_WR_SHIFT_OBS_2 PHY_WR_ADDER_SLV_DLY_ENC_OBS_2
DENALI_PHY_295	PHY_BASE_ADDR + 295	RD	PHY_WRLVL_HARD1_DELAY_OBS_2
DENALI_PHY_296	PHY_BASE_ADDR + 296	RD	PHY_WRLVL_STATUS_OBS_2
DENALI_PHY_297	PHY_BASE_ADDR + 297	RD RD	PHY_GATE_SMPL2_SLV_DLY_ENC_OBS_2 PHY_GATE_SMPL1_SLV_DLY_ENC_OBS_2
DENALI_PHY_298	PHY_BASE_ADDR + 298	RD RD	PHY_GTLVL_HARD0_DELAY_OBS_2 PHY_WRLVL_ERROR_OBS_2
DENALI_PHY_299	PHY_BASE_ADDR + 299	RD RD	PHY_GTLVL_STATUS_OBS_2 PHY_GTLVL_HARD1_DELAY_OBS_2
DENALI_PHY_300	PHY_BASE_ADDR + 300	RD RD	PHY_RDLVL_RDDQS_DQ_TE_DLY_OBS_2

Name	Register Address	Type	PHY Parameter(s)
			PHY_RDLVL_RDDQS_DQ_LE_DLY_OBS_2
DENALI_PHY_301	PHY_BASE_ADDR + 301	RD	PHY_RDLVL_RDDQS_DQ_NUM_WINDOWS_OBS_2
DENALI_PHY_302	PHY_BASE_ADDR + 302	RD	PHY_RDLVL_STATUS_OBS_2
DENALI_PHY_303	PHY_BASE_ADDR + 303	RD	PHY_WDQLVL_DQDM_TE_DLY_OBS_2
		RD	PHY_WDQLVL_DQDM_LE_DLY_OBS_2
DENALI_PHY_304	PHY_BASE_ADDR + 304	RD	PHY_WDQLVL_STATUS_OBS_2
DENALI_PHY_305	PHY_BASE_ADDR + 305	RW	PHY_DDL_MODE_2
DENALI_PHY_306	PHY_BASE_ADDR + 306	RD	PHY_DDL_TEST_OBS_2
DENALI_PHY_307	PHY_BASE_ADDR + 307	RD	PHY_DDL_TEST_MSTR_DLY_OBS_2
DENALI_PHY_308	PHY_BASE_ADDR + 308	RW	PHY_RX_CAL_SAMPLE_WAIT_2
		RW	PHY_RX_CAL_OVERRIDE_2
		WR	SC_PHY_RX_CAL_START_2
DENALI_PHY_309	PHY_BASE_ADDR + 309	RW+	PHY_RX_CAL_DQ1_2
		RW+	PHY_RX_CAL_DQ0_2
DENALI_PHY_310	PHY_BASE_ADDR + 310	RW+	PHY_RX_CAL_DQ3_2
		RW+	PHY_RX_CAL_DQ2_2
DENALI_PHY_311	PHY_BASE_ADDR + 311	RW+	PHY_RX_CAL_DQ5_2
		RW+	PHY_RX_CAL_DQ4_2
DENALI_PHY_312	PHY_BASE_ADDR + 312	RW+	PHY_RX_CAL_DQ7_2
		RW+	PHY_RX_CAL_DQ6_2
DENALI_PHY_313	PHY_BASE_ADDR + 313	RW+	PHY_RX_CAL_DQS_2
		RW+	PHY_RX_CAL_DM_2
DENALI_PHY_314	PHY_BASE_ADDR + 314	RD	PHY_RX_CAL_OBS_2
		RW+	PHY_RX_CAL_FDBK_2
DENALI_PHY_315	PHY_BASE_ADDR + 315	RW+	PHY_CLK_WRDQ1_SLAVE_DELAY_2
		RW+	PHY_CLK_WRDQ0_SLAVE_DELAY_2
DENALI_PHY_316	PHY_BASE_ADDR + 316	RW+	PHY_CLK_WRDQ3_SLAVE_DELAY_2
		RW+	PHY_CLK_WRDQ2_SLAVE_DELAY_2
DENALI_PHY_317	PHY_BASE_ADDR + 317	RW+	PHY_CLK_WRDQ5_SLAVE_DELAY_2
		RW+	PHY_CLK_WRDQ4_SLAVE_DELAY_2
DENALI_PHY_318	PHY_BASE_ADDR + 318	RW+	PHY_CLK_WRDQ7_SLAVE_DELAY_2
		RW+	PHY_CLK_WRDQ6_SLAVE_DELAY_2
DENALI_PHY_319	PHY_BASE_ADDR + 319	RW+	PHY_CLK_WRDQS_SLAVE_DELAY_2
		RW+	PHY_CLK_WRDM_SLAVE_DELAY_2

Name	Register Address	Type	PHY Parameter(s)
DENALI_PHY_320	PHY_BASE_ADDR + 320	RW+ RW+	PHY_RDDQ1_SLAVE_DELAY_2 PHY_RDDQ0_SLAVE_DELAY_2
DENALI_PHY_321	PHY_BASE_ADDR + 321	RW+ RW+	PHY_RDDQ3_SLAVE_DELAY_2 PHY_RDDQ2_SLAVE_DELAY_2
DENALI_PHY_322	PHY_BASE_ADDR + 322	RW+ RW+	PHY_RDDQ5_SLAVE_DELAY_2 PHY_RDDQ4_SLAVE_DELAY_2
DENALI_PHY_323	PHY_BASE_ADDR + 323	RW+ RW+	PHY_RDDQ7_SLAVE_DELAY_2 PHY_RDDQ6_SLAVE_DELAY_2
DENALI_PHY_324	PHY_BASE_ADDR + 324	RW+ RW+	PHY_RDDQS_DQ0_RISE_SLAVE_DELAY_2 PHY_RDDM_SLAVE_DELAY_2
DENALI_PHY_325	PHY_BASE_ADDR + 325	RW+ RW+	PHY_RDDQS_DQ1_RISE_SLAVE_DELAY_2 PHY_RDDQS_DQ0_FALL_SLAVE_DELAY_2
DENALI_PHY_326	PHY_BASE_ADDR + 326	RW+ RW+	PHY_RDDQS_DQ2_RISE_SLAVE_DELAY_2 PHY_RDDQS_DQ1_FALL_SLAVE_DELAY_2
DENALI_PHY_327	PHY_BASE_ADDR + 327	RW+ RW+	PHY_RDDQS_DQ3_RISE_SLAVE_DELAY_2 PHY_RDDQS_DQ2_FALL_SLAVE_DELAY_2
DENALI_PHY_328	PHY_BASE_ADDR + 328	RW+ RW+	PHY_RDDQS_DQ4_RISE_SLAVE_DELAY_2 PHY_RDDQS_DQ3_FALL_SLAVE_DELAY_2
DENALI_PHY_329	PHY_BASE_ADDR + 329	RW+ RW+	PHY_RDDQS_DQ5_RISE_SLAVE_DELAY_2 PHY_RDDQS_DQ4_FALL_SLAVE_DELAY_2
DENALI_PHY_330	PHY_BASE_ADDR + 330	RW+ RW+	PHY_RDDQS_DQ6_RISE_SLAVE_DELAY_2 PHY_RDDQS_DQ5_FALL_SLAVE_DELAY_2

Name	Register Address	Type	PHY Parameter(s)
DENALI_PHY_331	PHY_BASE_ADDR + 331	RW+ RW+	PHY_RDDQS_DQ7_RISE_SLAVE_DELAY_2 PHY_RDDQS_DQ6_FALL_SLAVE_DELAY_2
DENALI_PHY_332	PHY_BASE_ADDR + 332	RW+ RW+	PHY_RDDQS_DM_RISE_SLAVE_DELAY_2 PHY_RDDQS_DQ7_FALL_SLAVE_DELAY_2
DENALI_PHY_333	PHY_BASE_ADDR + 333	RW+ RW+	PHY_RDDQS_GATE_SLAVE_DELAY_2 PHY_RDDQS_DM_FALL_SLAVE_DELAY_2
DENALI_PHY_334	PHY_BASE_ADDR + 334	RW+ RW+ RW+	PHY_WRLVL_DELAY_EARLY_THRESHOLD_2 PHY_WRITE_PATH_LAT_ADD_2 PHY_RDDQS_LATENCY_ADJUST_2
DENALI_PHY_335	PHY_BASE_ADDR + 335	RW+ RW+	PHY_WRLVL_EARLY_FORCE_ZERO_2 PHY_WRLVL_DELAY_PERIOD_THRESHOLD_2
DENALI_PHY_336	PHY_BASE_ADDR + 336	RW+ RW+	PHY_GTLVL_LAT_ADJ_START_2 PHY_GTLVL_RDDQS_SLV_DLY_START_2
DENALI_PHY_337	PHY_BASE_ADDR + 337	RW+ RW+	PHY_RDLVL_RDDQS_DQ_SLV_DLY_START_2 PHY_WDQLVL_DQDM_SLV_DLY_START_2
DENALI_PHY_338	PHY_BASE_ADDR + 338	RW	RESERVED
DENALI_PHY_339	PHY_BASE_ADDR + 339	RW+ RW+ RW+	PHY_DQS_OE_TIMING_2 PHY_DQ_TSEL_WR_TIMING_2 PHY_DQ_TSEL_RD_TIMING_2
DENALI_PHY_340	PHY_BASE_ADDR + 340	RW+ RW+ RW+	PHY_DQ_IE_TIMING_2 PHY_PER_CS_TRAINING_EN_2 PHY_DQS_TSEL_WR_TIMING_2
DENALI_PHY_341	PHY_BASE_ADDR + 341	RW+ RW+ RW+	PHY_RDDATA_EN_DLY_2 PHY_IE_MODE_2 PHY_RDDATA_EN_IE_DLY_2
DENALI_PHY_342	PHY_BASE_ADDR + 342	RW+ RW+	PHY_MASTER_DELAY_START_2 PHY_SW_MASTER_MODE_2

Name	Register Address	Type	PHY Parameter(s)
		RW+	PHY_RDDATA_EN_TSEL_DLY_2
DENALI_PHY_343	PHY_BASE_ADDR + 343	RW+ RW+ RW+	PHY_WRLVL_DLY_STEP_2 PHY_RPTR_UPDATE_2 PHY_MASTER_DELAY_WAIT_2
DENALI_PHY_344	PHY_BASE_ADDR + 344	RW+ RW+ RW+	PHY_GTLVL_RESP_WAIT_CNT_2 PHY_GTLVL_DLY_STEP_2 PHY_WRLVL_RESP_WAIT_CNT_2
DENALI_PHY_345	PHY_BASE_ADDR + 345	RW+ RW+	PHY_GTLVL_FINAL_STEP_2 PHY_GTLVL_BACK_STEP_2
DENALI_PHY_346	PHY_BASE_ADDR + 346	RW+ RW+	PHY_RDLVL_DLY_STEP_2 PHY_WDQLVL_DLY_STEP_2
DENALI_PHY_384	PHY_BASE_ADDR + 384	RW	PHY_DQ_DM_SWIZZLE0_3
DENALI_PHY_385	PHY_BASE_ADDR + 385	RW RW	PHY_CLK_WR_BYPASS_SLAVE_DELAY_3 PHY_DQ_DM_SWIZZLE1_3
DENALI_PHY_386	PHY_BASE_ADDR + 386	RW RW RW	PHY_CLK_BYPASS_OVERRIDE_3 PHY_BYPASS_TWO_CYC_PREAMBLE_3 PHY_RDDQS_GATE_BYPASS_SLAVE_DELAY_3
DENALI_PHY_387	PHY_BASE_ADDR + 387	RW RW RW	PHY_SW_WRDQ3_SHIFT_3 PHY_SW_WRDQ2_SHIFT_3 PHY_SW_WRDQ1_SHIFT_3
DENALI_PHY_388	PHY_BASE_ADDR + 388	RW RW RW	PHY_SW_WRDQ7_SHIFT_3 PHY_SW_WRDQ6_SHIFT_3 PHY_SW_WRDQ5_SHIFT_3
DENALI_PHY_389	PHY_BASE_ADDR + 389	RW RW RW	PHY_DQ_TSEL_ENABLE_3 PHY_SW_WRDQS_SHIFT_3 PHY_SW_WRDM_SHIFT_3
DENALI_PHY_390	PHY_BASE_ADDR + 390	RW RW	PHY_DQS_TSEL_ENABLE_3 PHY_DQ_TSEL_SELECT_3
DENALI_PHY_391	PHY_BASE_ADDR + 391	RW+ RW	PHY_TWO_CYC_PREAMBLE_3 PHY_DQS_TSEL_SELECT_3
DENALI_PHY_392	PHY_BASE_ADDR + 392	RW RW_D RW RW	PHY_PER_CS_TRAINING_INDEX_3 PHY_PER_CS_TRAINING_MULTICAST_EN_3 PHY_PER_RANK_CS_MAP_3 PHY_DBI_MODE_3

Name	Register Address	Type	PHY Parameter(s)
DENALI_PHY_393	PHY_BASE_ADDR + 393	RW RW RW RW	PHY_LP4_BOOT_RPTR_UPDATE_3 PHY_LP4_BOOT_RDDATA_EN_TSEL_DLY_3 PHY_LP4_BOOT_RDDATA_EN_DLY_3 PHY_LP4_BOOT_RDDATA_EN_IE_DLY_3
DENALI_PHY_394	PHY_BASE_ADDR + 394	RW RW RW	PHY_SLICE_PWR_RDC_DISABLE_3 PHY_LPBK_CONTROL_3 PHY_LP4_BOOT_RDDQS_LATENCY_ADJUST_3
DENALI_PHY_395	PHY_BASE_ADDR + 395	WR RW RW	SC_PHY_SNAP_OBS_REGS_3 PHY_GATE_ERROR_DELAY_SELECT_3 PHY_RDDQS_DQ_BYPASS_SLAVE_DELAY_3
DENALI_PHY_396	PHY_BASE_ADDR + 396	RW RW RW	PHY_GATE_SMPL1_SLAVE_DELAY_3 PHY_LPDDR_TYPE_3 PHY_LPDDR_3
DENALI_PHY_397	PHY_BASE_ADDR + 397	RW RW	ON_FLY_GATE_ADJUST_EN_3 PHY_GATE_SMPL2_SLAVE_DELAY_3
DENALI_PHY_398	PHY_BASE_ADDR + 398	RD	PHY_GATE_TRACKING_OBS_3
DENALI_PHY_399	PHY_BASE_ADDR + 399	RW RW	PHY_LP4_PST_AMBLE_3 PHY_DFI40_POLARITY_3
DENALI_PHY_400	PHY_BASE_ADDR + 400	RW	PHY_LP4_RDLVL_PATT8_3
DENALI_PHY_401	PHY_BASE_ADDR + 401	RW	PHY_LP4_RDLVL_PATT9_3
DENALI_PHY_402	PHY_BASE_ADDR + 402	RW	PHY_LP4_RDLVL_PATT10_3
DENALI_PHY_403	PHY_BASE_ADDR + 403	RW	PHY_LP4_RDLVL_PATT11_3
DENALI_PHY_404	PHY_BASE_ADDR + 404	RW RW RW RW	PHY_RDDQ_ENC_OBS_SELECT_3 PHY_MASTER_DLY_LOCK_OBS_SELECT_3 PHY_SW_FIFO_PTR_RST_DISABLE_3 PHY_SLAVE_LOOP_CNT_UPDATE_3
DENALI_PHY_405	PHY_BASE_ADDR + 405	RW RW RW	PHY_FIFO_PTR_OBS_SELECT_3 PHY_WR_SHIFT_OBS_SELECT_3 PHY_WR_ENC_OBS_SELECT_3
DENALI_PHY_406	PHY_BASE_ADDR + 406	RW RW WR	PHY_WRLVL_UPDT_WAIT_CNT_3 PHY_WRLVL_CAPTURE_CNT_3 SC_PHY_LVL_DEBUG_CONT_3

Name	Register Address	Type	PHY Parameter(s)
DENALI_PHY_407	PHY_BASE_ADDR + 407	RW RW RW	PHY_RDLVL_UPDT_WAIT_CNT_3 PHY_RDLVL_CAPTURE_CNT_3 PHY_GTLVL_UPDT_WAIT_CNT_3
DENALI_PHY_408	PHY_BASE_ADDR + 408	RW RW RW	PHY_WDQLVL_BURST_CNT_3 PHY_RDLVL_DATA_MASK_3 PHY_RDLVL_RDDQS_DQ_OBS_SELECT
DENALI_PHY_409	PHY_BASE_ADDR + 409	RW RW RW	PHY_WDQLVL_UPDT_WAIT_CNT_3 PHY_WDQLVL_DQDM_SLV_DLY_JUMP_OF FSET_3 PHY_WDQLVL_PATT_3
DENALI_PHY_410	PHY_BASE_ADDR + 410	WR RW RW	SC_PHY_WDQLVL_CLR_PREV_RESULTS _3 PHY_WDQLVL_QTR_DLY_STEP_3 PHY_WDQLVL_DQDM_OBS_SELECT_3
DENALI_PHY_411	PHY_BASE_ADDR + 411	RW	PHY_WDQLVL_DATADM_MASK_3
DENALI_PHY_412	PHY_BASE_ADDR + 412	RW	PHY_USER_PATT0_3
DENALI_PHY_413	PHY_BASE_ADDR + 413	RW	PHY_USER_PATT1_3
DENALI_PHY_414	PHY_BASE_ADDR + 414	RW	PHY_USER_PATT2_3
DENALI_PHY_415	PHY_BASE_ADDR + 415	RW	PHY_USER_PATT3_3
DENALI_PHY_416	PHY_BASE_ADDR + 416	WR RW RW	SC_PHY_MANUAL_CLEAR_3 PHY_CALVL_VREF_DRIVING_SLICE_3 PHY_USER_PATT4_3
DENALI_PHY_417	PHY_BASE_ADDR + 417	RD	PHY_FIFO_PTR_OBS_3
DENALI_PHY_418	PHY_BASE_ADDR + 418	RD	PHY_LPBK_RESULT_OBS_3
DENALI_PHY_419	PHY_BASE_ADDR + 419	RD	PHY_MASTER_DLY_LOCK_OBS_3
DENALI_PHY_420	PHY_BASE_ADDR + 420	RD RD RD RD	PHY_RDDQS_DQ_FALL_ADDER_SLV_D LY_ENC_OBS_3 PHY_RDDQS_DQ_RISE_ADDER_SLV_D LY_ENC_OBS_3 PHY_RDDQS_BASE_SLV_DLY_ENC_OB S_3 PHY_RDDQ_SLV_DLY_ENC_OBS_3
DENALI_PHY_421	PHY_BASE_ADDR + 421	RD RD RD	PHY_WRDQ_BASE_SLV_DLY_ENC_OBS _3 PHY_WRDQS_BASE_SLV_DLY_ENC_OB S_3 PHY_RDDQS_GATE_SLV_DLY_ENC_OB S_3

Name	Register Address	Type	PHY Parameter(s)
DENALI_PHY_422	PHY_BASE_ADDR + 422	RD RD RD	PHY_WRLVL_HARD0_DELAY_OBS_3 PHY_WR_SHIFT_OBS_3 PHY_WR_ADDER_SLV_DLY_ENC_OBS_3
DENALI_PHY_423	PHY_BASE_ADDR + 423	RD	PHY_WRLVL_HARD1_DELAY_OBS_3
DENALI_PHY_424	PHY_BASE_ADDR + 424	RD	PHY_WRLVL_STATUS_OBS_3
DENALI_PHY_425	PHY_BASE_ADDR + 425	RD RD	PHY_GATE_SMPL2_SLV_DLY_ENC_OBS_3 PHY_GATE_SMPL1_SLV_DLY_ENC_OBS_3
DENALI_PHY_426	PHY_BASE_ADDR + 426	RD RD	PHY_GTLVL_HARD0_DELAY_OBS_3 PHY_WRLVL_ERROR_OBS_3
DENALI_PHY_427	PHY_BASE_ADDR + 427	RD	PHY_GTLVL_STATUS_OBS_3
DENALI_PHY_428	PHY_BASE_ADDR + 428	RD RD	PHY_RDLVL_RDDQS_DQ_TE_DLY_OBS_3 PHY_RDLVL_RDDQS_DQ_LE_DLY_OBS_3
DENALI_PHY_429	PHY_BASE_ADDR + 429	RD	PHY_RDLVL_RDDQS_DQ_NUM_WINDOWS_OBS_3
DENALI_PHY_430	PHY_BASE_ADDR + 430	RD	PHY_RDLVL_STATUS_OBS_3
DENALI_PHY_431	PHY_BASE_ADDR + 431	RD RD	PHY_WDQLVL_DQDM_TE_DLY_OBS_3 PHY_WDQLVL_DQDM_LE_DLY_OBS_3
DENALI_PHY_432	PHY_BASE_ADDR + 432	RD	PHY_WDQLVL_STATUS_OBS_3
DENALI_PHY_433	PHY_BASE_ADDR + 433	RW	PHY_DDL_MODE_3
DENALI_PHY_434	PHY_BASE_ADDR + 434	RD	PHY_DDL_TEST_OBS_3
DENALI_PHY_435	PHY_BASE_ADDR + 435	RD	PHY_DDL_TEST_MSTR_DLY_OBS_3
DENALI_PHY_436	PHY_BASE_ADDR + 436	RW RW WR	PHY_RX_CAL_SAMPLE_WAIT_3 PHY_RX_CAL_OVERRIDE_3 SC_PHY_RX_CAL_START_3
DENALI_PHY_437	PHY_BASE_ADDR + 437	RW+ RW+	PHY_RX_CAL_DQ1_3 PHY_RX_CAL_DQ0_3
DENALI_PHY_438	PHY_BASE_ADDR + 438	RW+ RW+	PHY_RX_CAL_DQ3_3 PHY_RX_CAL_DQ2_3
DENALI_PHY_439	PHY_BASE_ADDR + 439	RW+ RW+	PHY_RX_CAL_DQ5_3 PHY_RX_CAL_DQ4_3
DENALI_PHY_440	PHY_BASE_ADDR + 440	RW+	PHY_RX_CAL_DQ7_3

Name	Register Address	Type	PHY Parameter(s)
		RW+	PHY_RX_CAL_DQ6_3
DENALI_PHY_441	PHY_BASE_ADDR + 441	RW+ RW+	PHY_RX_CAL_DQS_3 PHY_RX_CAL_DM_3
DENALI_PHY_442	PHY_BASE_ADDR + 442	RD RW+	PHY_RX_CAL_OBS_3 PHY_RX_CAL_FDBK_3
DENALI_PHY_443	PHY_BASE_ADDR + 443	RW+ RW+	PHY_CLK_WRDQ1_SLAVE_DELAY_3 PHY_CLK_WRDQ0_SLAVE_DELAY_3
DENALI_PHY_444	PHY_BASE_ADDR + 444	RW+ RW+	PHY_CLK_WRDQ3_SLAVE_DELAY_3 PHY_CLK_WRDQ2_SLAVE_DELAY_3
DENALI_PHY_445	PHY_BASE_ADDR + 445	RW+ RW+	PHY_CLK_WRDQ5_SLAVE_DELAY_3 PHY_CLK_WRDQ4_SLAVE_DELAY_3
DENALI_PHY_446	PHY_BASE_ADDR + 446	RW+ RW+	PHY_CLK_WRDQ7_SLAVE_DELAY_3 PHY_CLK_WRDQ6_SLAVE_DELAY_3
DENALI_PHY_447	PHY_BASE_ADDR + 447	RW+ RW+	PHY_CLK_WRDQS_SLAVE_DELAY_3 PHY_CLK_WRDM_SLAVE_DELAY_3
DENALI_PHY_448	PHY_BASE_ADDR + 448	RW+ RW+	PHY_RDDQ1_SLAVE_DELAY_3 PHY_RDDQ0_SLAVE_DELAY_3
DENALI_PHY_449	PHY_BASE_ADDR + 449	RW+ RW+	PHY_RDDQ3_SLAVE_DELAY_3 PHY_RDDQ2_SLAVE_DELAY_3
DENALI_PHY_450	PHY_BASE_ADDR + 450	RW+ RW+	PHY_RDDQ5_SLAVE_DELAY_3 PHY_RDDQ4_SLAVE_DELAY_3
DENALI_PHY_451	PHY_BASE_ADDR + 451	RW+ RW+	PHY_RDDQ7_SLAVE_DELAY_3 PHY_RDDQ6_SLAVE_DELAY_3
DENALI_PHY_452	PHY_BASE_ADDR + 452	RW+ RW+	PHY_RDDQS_DQ0_RISE_SLAVE_DELAY_3 PHY_RDDM_SLAVE_DELAY_3
DENALI_PHY_453	PHY_BASE_ADDR + 453	RW+ RW+	PHY_RDDQS_DQ1_RISE_SLAVE_DELAY_3 PHY_RDDQS_DQ0_FALL_SLAVE_DELAY_3
DENALI_PHY_454	PHY_BASE_ADDR + 454	RW+ RW+	PHY_RDDQS_DQ2_RISE_SLAVE_DELAY_3 PHY_RDDQS_DQ1_FALL_SLAVE_DELAY_3

Name	Register Address	Type	PHY Parameter(s)
DENALI_PHY_455	PHY_BASE_ADDR + 455	RW+ RW+	PHY_RDDQS_DQ3_RISE_SLAVE_DELAY_3 PHY_RDDQS_DQ2_FALL_SLAVE_DELAY_3
DENALI_PHY_456	PHY_BASE_ADDR + 456	RW+ RW+	PHY_RDDQS_DQ4_RISE_SLAVE_DELAY_3 PHY_RDDQS_DQ3_FALL_SLAVE_DELAY_3
DENALI_PHY_457	PHY_BASE_ADDR + 457	RW+ RW+	PHY_RDDQS_DQ5_RISE_SLAVE_DELAY_3 PHY_RDDQS_DQ4_FALL_SLAVE_DELAY_3
DENALI_PHY_458	PHY_BASE_ADDR + 458	RW+ RW+	PHY_RDDQS_DQ6_RISE_SLAVE_DELAY_3 PHY_RDDQS_DQ5_FALL_SLAVE_DELAY_3
DENALI_PHY_459	PHY_BASE_ADDR + 459	RW+ RW+	PHY_RDDQS_DQ7_RISE_SLAVE_DELAY_3 PHY_RDDQS_DQ6_FALL_SLAVE_DELAY_3
DENALI_PHY_460	PHY_BASE_ADDR + 460	RW+ RW+	PHY_RDDQS_DM_RISE_SLAVE_DELAY_3 PHY_RDDQS_DQ7_FALL_SLAVE_DELAY_3
DENALI_PHY_461	PHY_BASE_ADDR + 461	RW+ RW+	PHY_RDDQS_GATE_SLAVE_DELAY_3 PHY_RDDQS_DM_FALL_SLAVE_DELAY_3
DENALI_PHY_462	PHY_BASE_ADDR + 462	RW+ RW+ RW+	PHY_WRLVL_DELAY_EARLY_THRESHOLD_3 PHY_WRITE_PATH_LAT_ADD_3 PHY_RDDQS_LATENCY_ADJUST_3
DENALI_PHY_463	PHY_BASE_ADDR + 463	RW+ RW+	PHY_WRLVL_EARLY_FORCE_ZERO_3 PHY_WRLVL_DELAY_PERIOD_THRESHOLD_3
DENALI_PHY_464	PHY_BASE_ADDR + 464	RW+ RW+	PHY_GTLVL_LAT_ADJ_START_3 PHY_GTLVL_RDDQS_SLV_DLY_START_3

Name	Register Address	Type	PHY Parameter(s)
DENALI_PHY_465	PHY_BASE_ADDR + 465	RW+ RW+	PHY_RDLVL_RDDQS_DQ_SLV_DLY_START_3 PHY_WDQLVL_DQDM_SLV_DLY_START_3
DENALI_PHY_466	PHY_BASE_ADDR + 466	RW	RESERVED
DENALI_PHY_467	PHY_BASE_ADDR + 467	RW+ RW+ RW+	PHY_DQS_OE_TIMING_3 PHY_DQ_TSEL_WR_TIMING_3 PHY_DQ_TSEL_RD_TIMING_3
DENALI_PHY_468	PHY_BASE_ADDR + 468	RW+ RW+ RW+	PHY_DQ_IE_TIMING_3 PHY_PER_CS_TRAINING_EN_3 PHY_DQS_TSEL_WR_TIMING_3
DENALI_PHY_469	PHY_BASE_ADDR + 469	RW+ RW+ RW+	PHY_RDDATA_EN_DLY_3 PHY_IE_MODE_3 PHY_RDDATA_EN_IE_DLY_3
DENALI_PHY_470	PHY_BASE_ADDR + 470	RW+ RW+ RW+	PHY_MASTER_DELAY_START_3 PHY_SW_MASTER_MODE_3 PHY_RDDATA_EN_TSEL_DLY_3
DENALI_PHY_471	PHY_BASE_ADDR + 471	RW+ RW+ RW+	PHY_WRLVL_DLY_STEP_3 PHY_RPTR_UPDATE_3 PHY_MASTER_DELAY_WAIT_3
DENALI_PHY_472	PHY_BASE_ADDR + 472	RW+ RW+ RW+	PHY_GTLVL_RESP_WAIT_CNT_3 PHY_GTLVL_DLY_STEP_3 PHY_WRLVL_RESP_WAIT_CNT_3
DENALI_PHY_473	PHY_BASE_ADDR + 473	RW+ RW+	PHY_GTLVL_FINAL_STEP_3 PHY_GTLVL_BACK_STEP_3
DENALI_PHY_474	PHY_BASE_ADDR + 474	RW+ RW+	PHY_RDLVL_DLY_STEP_3 PHY_WDQLVL_DLY_STEP_3
DENALI_PHY_512	PHY_BASE_ADDR + 512	RW+ RW+ RW+ RW+	PHY_ADR3_SW_WRADDR_SHIFT_0 PHY_ADR2_SW_WRADDR_SHIFT_0 PHY_ADR1_SW_WRADDR_SHIFT_0 PHY_ADR0_SW_WRADDR_SHIFT_0
DENALI_PHY_513	PHY_BASE_ADDR + 513	RW RW+ RW+	PHY_ADR_CLK_WR_BYPASS_SLAVE_DELAY_0 PHY_ADR5_SW_WRADDR_SHIFT_0 PHY_ADR4_SW_WRADDR_SHIFT_0
DENALI_PHY_514	PHY_BASE_ADDR + 514	WR RW	SC_PHY_ADR_MANUAL_CLEAR_0 PHY_ADR_CLK_BYPASS_OVERRIDE_0
DENALI_PHY_515	PHY_BASE_ADDR + 515	RD	PHY_ADR_LPBK_RESULT_OBS_0

Name	Register Address	Type	PHY Parameter(s)
DENALI_PHY_516	PHY_BASE_ADDR + 516	RW RD	PHY_ADR_MASTER_DLY_LOCK_OBS_SELECT_0 PHY_ADR_LPBK_ERROR_COUNT_OBS_0
DENALI_PHY_517	PHY_BASE_ADDR + 517	RW RW RD	PHY_ADR_SLV_DLY_ENC_OBS_SELECT_0 PHY_ADR_SLAVE_LOOP_CNT_UPDATE_0 PHY_ADR_MASTER_DLY_LOCK_OBS_0
DENALI_PHY_518	PHY_BASE_ADDR + 518	RW RW RW WR	PHY_ADR_PWR_RDC_DISABLE_0 PHY_ADR_LPBK_CONTROL_0 PHY_ADR_TSEL_ENABLE_0 SC_PHY_ADR_SNAP_OBS_REGS_0
DENALI_PHY_519	PHY_BASE_ADDR + 519	RW RD RW	PHY_ADR_IE_MODE_0 PHY_ADR_WRADDR_SHIFT_OBS_0 PHY_ADR_TYPE_0
DENALI_PHY_520	PHY_BASE_ADDR + 520	RW	PHY_ADR_DDL_MODE_0
DENALI_PHY_521	PHY_BASE_ADDR + 521	RD	PHY_ADR_DDL_TEST_OBS_0
DENALI_PHY_522	PHY_BASE_ADDR + 522	RD	PHY_ADR_DDL_TEST_MSTR_DLY_OBS
DENALI_PHY_523	PHY_BASE_ADDR + 523	RW RW	PHY_ADR_CALVL_COARSE_DLY_0 PHY_ADR_CALVL_START_0
DENALI_PHY_524	PHY_BASE_ADDR + 524	RW	PHY_ADR_CALVL_QTR_0
DENALI_PHY_525	PHY_BASE_ADDR + 525	RW	PHY_ADR_CALVL_SWIZZLE0_0_0
DENALI_PHY_526	PHY_BASE_ADDR + 526	RW	PHY_ADR_CALVL_SWIZZLE1_0_0
DENALI_PHY_527	PHY_BASE_ADDR + 527	RW	PHY_ADR_CALVL_SWIZZLE0_1_0
DENALI_PHY_528	PHY_BASE_ADDR + 528	RW RW	PHY_ADR_CALVL_DEVICE_MAP_0 PHY_ADR_CALVL_SWIZZLE1_1_0
DENALI_PHY_529	PHY_BASE_ADDR + 529	RW RW RW RW	PHY_ADR_CALVL_RESP_WAIT_CNT_0 PHY_ADR_CALVL_CAPTURE_CNT_0 PHY_ADR_CALVL_NUM_PATTERNS_0 PHY_ADR_CALVL_RANK_CTRL_0
DENALI_PHY_530	PHY_BASE_ADDR + 530	RW WR WR RW	PHY_ADR_CALVL_OBS_SELECT_0 SC_PHY_ADR_CALVL_ERROR_CLR_0 SC_PHY_ADR_CALVL_DEBUG_CONT_0 PHY_ADR_CALVL_DEBUG_MODE_0
DENALI_PHY_531	PHY_BASE_ADDR + 531	RD	PHY_ADR_CALVL_OBS0_0
DENALI_PHY_532	PHY_BASE_ADDR + 532	RD	PHY_ADR_CALVL_OBS1_0
DENALI_PHY_533	PHY_BASE_ADDR + 533	RW	PHY_ADR_CALVL_FG_0_0
DENALI_PHY_534	PHY_BASE_ADDR + 534	RW	PHY_ADR_CALVL_BG_0_0
DENALI_PHY_535	PHY_BASE_ADDR + 535	RW	PHY_ADR_CALVL_FG_1_0
DENALI_PHY_536	PHY_BASE_ADDR + 536	RW	PHY_ADR_CALVL_BG_1_0
DENALI_PHY_537	PHY_BASE_ADDR + 537	RW	PHY_ADR_CALVL_FG_2_0
DENALI_PHY_538	PHY_BASE_ADDR + 538	RW	PHY_ADR_CALVL_BG_2_0
DENALI_PHY_539	PHY_BASE_ADDR + 539	RW	PHY_ADR_CALVL_FG_3_0
DENALI_PHY_540	PHY_BASE_ADDR + 540	RW	PHY_ADR_CALVL_BG_3_0
DENALI_PHY_541	PHY_BASE_ADDR + 541	RW	PHY_ADR_ADDR_SEL_0

Name	Register Address	Type	PHY Parameter(s)
DENALI_PHY_542	PHY_BASE_ADDR + 542	RW RW RW	PHY_ADR_SEG_MASK_0 PHY_ADR_BIT_MASK_0 PHY_ADR_LP4_BOOT_SLV_DELAY_0
DENALI_PHY_543	PHY_BASE_ADDR + 543	RW RW	RESERVED PHY_ADR_CALVL_TRAIN_MASK_0
DENALI_PHY_544	PHY_BASE_ADDR + 544	RW+ RW+	PHY_ADR0_CLK_WR_SLAVE_DELAY_0 PHY_ADR_TSEL_SELECT_0
DENALI_PHY_545	PHY_BASE_ADDR + 545	RW+ RW+	PHY_ADR2_CLK_WR_SLAVE_DELAY_0 PHY_ADR1_CLK_WR_SLAVE_DELAY_0
DENALI_PHY_546	PHY_BASE_ADDR + 546	RW+ RW+	PHY_ADR4_CLK_WR_SLAVE_DELAY_0 PHY_ADR3_CLK_WR_SLAVE_DELAY_0
DENALI_PHY_547	PHY_BASE_ADDR + 547	RW+ RW+	PHY_ADR_SW_MASTER_MODE_0 PHY_ADR5_CLK_WR_SLAVE_DELAY_0
DENALI_PHY_548	PHY_BASE_ADDR + 548	RW+ RW+ RW+	PHY_ADR_MASTER_DELAY_WAIT_0 PHY_ADR_MASTER_DELAY_STEP_0 PHY_ADR_MASTER_DELAY_START_0
DENALI_PHY_549	PHY_BASE_ADDR + 549	RW+	PHY_ADR_CALVL_DLY_STEP_0
DENALI_PHY_640	PHY_BASE_ADDR + 640	RW+ RW+ RW+	PHY_ADR3_SW_WRADDR_SHIFT_1 PHY_ADR2_SW_WRADDR_SHIFT_1 PHY_ADR1_SW_WRADDR_SHIFT_1
DENALI_PHY_641	PHY_BASE_ADDR + 641	RW RW+ RW+	PHY_ADR_CLK_WR_BYPASS_SLAVE_ DELAY_1 PHY_ADR5_SW_WRADDR_SHIFT_1 PHY_ADR4_SW_WRADDR_SHIFT_1
DENALI_PHY_642	PHY_BASE_ADDR + 642	WR RW	SC_PHY_ADR_MANUAL_CLEAR_1 PHY_ADR_CLK_BYPASS_OVERRIDE_1
DENALI_PHY_643	PHY_BASE_ADDR + 643	RD	PHY_ADR_LPBK_RESULT_OBS_1
DENALI_PHY_644	PHY_BASE_ADDR + 644	RW RD	PHY_ADR_MASTER_DLY_LOCK_OBS_S ELECT_1 PHY_ADR_LPBK_ERROR_COUNT_OBS _1
DENALI_PHY_645	PHY_BASE_ADDR + 645	RW RW RD	PHY_ADR_SLV_DLY_ENC_OBS_SELEC T_1 PHY_ADR_SLAVE_LOOP_CNT_UPDATE _1 PHY_ADR_MASTER_DLY_LOCK_OBS_ 1
DENALI_PHY_646	PHY_BASE_ADDR + 646	RW RW RW	PHY_ADR_PWR_RDC_DISABLE_1 PHY_ADR_LPBK_CONTROL_1 PHY_ADR_TSEL_ENABLE_1

Name	Register Address	Type	PHY Parameter(s)
DENALI_PHY_647	PHY_BASE_ADDR + 647	RW RD RW	PHY_ADR_IE_MODE_1 PHY_ADR_WRADDR_SHIFT_OBS_1 PHY_ADR_TYPE_1
DENALI_PHY_648	PHY_BASE_ADDR + 648	RW	PHY_ADR_DDL_MODE_1
DENALI_PHY_649	PHY_BASE_ADDR + 649	RD	PHY_ADR_DDL_TEST_OBS_1
DENALI_PHY_650	PHY_BASE_ADDR + 650	RD	PHY_ADR_DDL_TEST_MSTR_DLY_OBS_1
DENALI_PHY_651	PHY_BASE_ADDR + 651	RW RW	PHY_ADR_CALVL_COARSE_DLY_1 PHY_ADR_CALVL_START_1
DENALI_PHY_652	PHY_BASE_ADDR + 652	RW	PHY_ADR_CALVL_QTR_1
DENALI_PHY_653	PHY_BASE_ADDR + 653	RW	PHY_ADR_CALVL_SWIZZLE0_0_1
DENALI_PHY_654	PHY_BASE_ADDR + 654	RW	PHY_ADR_CALVL_SWIZZLE1_0_1
DENALI_PHY_655	PHY_BASE_ADDR + 655	RW	PHY_ADR_CALVL_SWIZZLE0_1_1
DENALI_PHY_656	PHY_BASE_ADDR + 656	RW RW	PHY_ADR_CALVL_DEVICE_MAP_1 PHY_ADR_CALVL_SWIZZLE1_1_1
DENALI_PHY_657	PHY_BASE_ADDR + 657	RW RW RW	PHY_ADR_CALVL_RESP_WAIT_CNT_1 PHY_ADR_CALVL_CAPTURE_CNT_1 PHY_ADR_CALVL_NUM_PATTERNS_1
DENALI_PHY_658	PHY_BASE_ADDR + 658	RW WR WR	PHY_ADR_CALVL_OBS_SELECT_1 SC_PHY_ADR_CALVL_ERROR_CLR_1 SC_PHY_ADR_CALVL_DEBUG_CONT_1
DENALI_PHY_659	PHY_BASE_ADDR + 659	RD	PHY_ADR_CALVL_OBS0_1
DENALI_PHY_660	PHY_BASE_ADDR + 660	RD	PHY_ADR_CALVL_OBS1_1
DENALI_PHY_661	PHY_BASE_ADDR + 661	RW	PHY_ADR_CALVL_FG_0_1
DENALI_PHY_662	PHY_BASE_ADDR + 662	RW	PHY_ADR_CALVL_BG_0_1
DENALI_PHY_663	PHY_BASE_ADDR + 663	RW	PHY_ADR_CALVL_FG_1_1
DENALI_PHY_664	PHY_BASE_ADDR + 664	RW	PHY_ADR_CALVL_BG_1_1
DENALI_PHY_665	PHY_BASE_ADDR + 665	RW	PHY_ADR_CALVL_FG_2_1
DENALI_PHY_666	PHY_BASE_ADDR + 666	RW	PHY_ADR_CALVL_BG_2_1
DENALI_PHY_667	PHY_BASE_ADDR + 667	RW	PHY_ADR_CALVL_FG_3_1
DENALI_PHY_668	PHY_BASE_ADDR + 668	RW	PHY_ADR_CALVL_BG_3_1
DENALI_PHY_669	PHY_BASE_ADDR + 669	RW	PHY_ADR_ADDR_SEL_1
DENALI_PHY_670	PHY_BASE_ADDR + 670	RW RW RW	PHY_ADR_SEG_MASK_1 PHY_ADR_BIT_MASK_1 PHY_ADR_LP4_BOOT_SLV_DELAY_1
DENALI_PHY_671	PHY_BASE_ADDR + 671	RW RW	RESERVED PHY_ADR_CALVL_TRAIN_MASK_1
DENALI_PHY_672	PHY_BASE_ADDR + 672	RW+ RW+	PHY_ADR0_CLK_WR_SLAVE_DELAY_1 PHY_ADR_TSEL_SELECT_1

Name	Register Address	Type	PHY Parameter(s)
DENALI_PHY_673	PHY_BASE_ADDR + 673	RW+ RW+	PHY_ADR2_CLK_WR_SLAVE_DELAY_1 PHY_ADR1_CLK_WR_SLAVE_DELAY_1
DENALI_PHY_674	PHY_BASE_ADDR + 674	RW+ RW+	PHY_ADR4_CLK_WR_SLAVE_DELAY_1 PHY_ADR3_CLK_WR_SLAVE_DELAY_1
DENALI_PHY_675	PHY_BASE_ADDR + 675	RW+ RW+	PHY_ADR_SW_MASTER_MODE_1 PHY_ADR5_CLK_WR_SLAVE_DELAY_1
DENALI_PHY_676	PHY_BASE_ADDR + 676	RW+ RW+ RW+	PHY_ADR_MASTER_DELAY_WAIT_1 PHY_ADR_MASTER_DELAY_STEP_1 PHY_ADR_MASTER_DELAY_START_1
DENALI_PHY_677	PHY_BASE_ADDR + 677	RW+	PHY_ADR_CALVL_DLY_STEP_1
DENALI_PHY_768	PHY_BASE_ADDR + 768	RW+ RW+ RW+	PHY_ADR3_SW_WRADDR_SHIFT_2 PHY_ADR2_SW_WRADDR_SHIFT_2 PHY_ADR1_SW_WRADDR_SHIFT_2
DENALI_PHY_769	PHY_BASE_ADDR + 769	RW RW+ RW+	PHY_ADR_CLK_WR_BYPASS_SLAVE_DELAY_2 PHY_ADR5_SW_WRADDR_SHIFT_2 PHY_ADR4_SW_WRADDR_SHIFT_2
DENALI_PHY_770	PHY_BASE_ADDR + 770	WR RW	SC_PHY_ADR_MANUAL_CLEAR_2 PHY_ADR_CLK_BYPASS_OVERRIDE_2
DENALI_PHY_771	PHY_BASE_ADDR + 771	RD	PHY_ADR_LPBK_RESULT_OBS_2
DENALI_PHY_772	PHY_BASE_ADDR + 772	RW RD	PHY_ADR_MASTER_DLY_LOCK_OBS_SELECT_2 PHY_ADR_LPBK_ERROR_COUNT_OBS_2
DENALI_PHY_773	PHY_BASE_ADDR + 773	RW RW RD	PHY_ADR_SLV_DLY_ENC_OBS_SELECT_2 PHY_ADR_SLAVE_LOOP_CNT_UPDATE_2 PHY_ADR_MASTER_DLY_LOCK_OBS_2
DENALI_PHY_774	PHY_BASE_ADDR + 774	RW RW RW	PHY_ADR_PWR_RDC_DISABLE_2 PHY_ADR_LPBK_CONTROL_2 PHY_ADR_TSEL_ENABLE_2
DENALI_PHY_775	PHY_BASE_ADDR + 775	RW RD RW	PHY_ADR_IE_MODE_2 PHY_ADR_WRADDR_SHIFT_OBS_2 PHY_ADR_TYPE_2

Name	Register Address	Type	PHY Parameter(s)
DENALI_PHY_776	PHY_BASE_ADDR + 776	RW	PHY_ADR_DDL_MODE_2
DENALI_PHY_777	PHY_BASE_ADDR + 777	RD	PHY_ADR_DDL_TEST_OBS_2
DENALI_PHY_778	PHY_BASE_ADDR + 778	RD	PHY_ADR_DDL_TEST_MSTR_DLY_OBS_2
DENALI_PHY_779	PHY_BASE_ADDR + 779	RW RW	PHY_ADR_CALVL_COARSE_DLY_2 PHY_ADR_CALVL_START_2
DENALI_PHY_780	PHY_BASE_ADDR + 780	RW	PHY_ADR_CALVL_QTR_2
DENALI_PHY_781	PHY_BASE_ADDR + 781	RW	PHY_ADR_CALVL_SWIZZLE0_0_2
DENALI_PHY_782	PHY_BASE_ADDR + 782	RW	PHY_ADR_CALVL_SWIZZLE1_0_2
DENALI_PHY_783	PHY_BASE_ADDR + 783	RW	PHY_ADR_CALVL_SWIZZLE0_1_2
DENALI_PHY_784	PHY_BASE_ADDR + 784	RW RW	PHY_ADR_CALVL_DEVICE_MAP_2 PHY_ADR_CALVL_SWIZZLE1_1_2
DENALI_PHY_785	PHY_BASE_ADDR + 785	RW RW RW	PHY_ADR_CALVL_RESP_WAIT_CNT_2 PHY_ADR_CALVL_CAPTURE_CNT_2 PHY_ADR_CALVL_NUM_PATTERNS_2
DENALI_PHY_786	PHY_BASE_ADDR + 786	RW WR WR	PHY_ADR_CALVL_OBS_SELECT_2 SC_PHY_ADR_CALVL_ERROR_CLR_2 SC_PHY_ADR_CALVL_DEBUG_CONT
DENALI_PHY_787	PHY_BASE_ADDR + 787	RD	PHY_ADR_CALVL_OBS0_2
DENALI_PHY_788	PHY_BASE_ADDR + 788	RD	PHY_ADR_CALVL_OBS1_2
DENALI_PHY_789	PHY_BASE_ADDR + 789	RW	PHY_ADR_CALVL_FG_0_2
DENALI_PHY_790	PHY_BASE_ADDR + 790	RW	PHY_ADR_CALVL_BG_0_2
DENALI_PHY_791	PHY_BASE_ADDR + 791	RW	PHY_ADR_CALVL_FG_1_2
DENALI_PHY_792	PHY_BASE_ADDR + 792	RW	PHY_ADR_CALVL_BG_1_2
DENALI_PHY_793	PHY_BASE_ADDR + 793	RW	PHY_ADR_CALVL_FG_2_2
DENALI_PHY_794	PHY_BASE_ADDR + 794	RW	PHY_ADR_CALVL_BG_2_2
DENALI_PHY_795	PHY_BASE_ADDR + 795	RW	PHY_ADR_CALVL_FG_3_2
DENALI_PHY_796	PHY_BASE_ADDR + 796	RW	PHY_ADR_CALVL_BG_3_2
DENALI_PHY_797	PHY_BASE_ADDR + 797	RW	PHY_ADR_ADDR_SEL_2
DENALI_PHY_798	PHY_BASE_ADDR + 798	RW RW RW	PHY_ADR_SEG_MASK_2 PHY_ADR_BIT_MASK_2 PHY_ADR_LP4_BOOT_SLV_DELAY_2
DENALI_PHY_799	PHY_BASE_ADDR + 799	RW RW	RESERVED PHY_ADR_CALVL_TRAIN_MASK_2
DENALI_PHY_800	PHY_BASE_ADDR + 800	RW+ RW+	PHY_ADR0_CLK_WR_SLAVE_DELAY_2 PHY_ADR_TSEL_SELECT_2
DENALI_PHY_801	PHY_BASE_ADDR + 801	RW+ RW+	PHY_ADR2_CLK_WR_SLAVE_DELAY_2 PHY_ADR1_CLK_WR_SLAVE_DELAY_2
DENALI_PHY_802	PHY_BASE_ADDR + 802	RW+ RW+	PHY_ADR4_CLK_WR_SLAVE_DELAY_2 PHY_ADR3_CLK_WR_SLAVE_DELAY_2

Name	Register Address	Type	PHY Parameter(s)
DENALI_PHY_803	PHY_BASE_ADDR + 803	RW+ RW+	PHY_ADR_SW_MASTER_MODE_2 PHY_ADR5_CLK_WR_SLAVE_DELAY_2
DENALI_PHY_804	PHY_BASE_ADDR + 804	RW+ RW+ RW+	PHY_ADR_MASTER_DELAY_WAIT_2 PHY_ADR_MASTER_DELAY_STEP_2 PHY_ADR_MASTER_DELAY_START_2
DENALI_PHY_805	PHY_BASE_ADDR + 805	RW+	PHY_ADR_CALVL_DLY_STEP_2
DENALI_PHY_896	PHY_AC_BASE_ADDR +	RW+ RW+ RW+	PHY_SW_GRP_SHIFT_1 PHY_SW_GRP_SHIFT_0 PHY_FREQ_SEL_INDEX
DENALI_PHY_897	PHY_AC_BASE_ADDR + 1	RW RW+	PHY_GRP_BYPASS_SLAVE_DELAY PHY_SW_GRP_SHIFT_3
DENALI_PHY_898	PHY_AC_BASE_ADDR +	RW WR RW	PHY_LP4_BOOT_DISABLE SC_PHY_MANUAL_UPDATE PHY_GRP_BYPASS_OVERRIDE
DENALI_PHY_899	PHY_AC_BASE_ADDR + 3	RW RW	PHY_CSLVL_START PHY_CSLVL_CS_MAP
DENALI_PHY_900	PHY_AC_BASE_ADDR +	RW RW	PHY_CSLVL_CAPTURE_CNT PHY_CSLVL_OTR
DENALI_PHY_901	PHY_AC_BASE_ADDR + 5	RW RW	PHY_CSLVL_DEBUG_MODE PHY_CSLVL_COARSE_CAPTURE_CNT
DENALI_PHY_902	PHY_AC_BASE_ADDR +	WR WR	SC_PHY_CSLVL_ERROR_CLR SC_PHY_CSLVL_DEBUG_CONT
DENALI_PHY_903	PHY_AC_BASE_ADDR +	RD	PHY_CSLVL_OBS0
DENALI_PHY_904	PHY_AC_BASE_ADDR +	RD	PHY_CSLVL_OBS1
DENALI_PHY_905	PHY_AC_BASE_ADDR + 9	RW RW	PHY_GRP_SHIFT_OBS_SELECT PHY_GRP_SLV_DLY_ENC_OBS_SELE
DENALI_PHY_906	PHY_AC_BASE_ADDR + 10	RW RD	PHY_ADRCTL_SLAVE_LOOP_CNT_UP DATE PHY_GRP_SHIFT_OBS
DENALI_PHY_907	PHY_AC_BASE_ADDR + 11	RW RW RW	PHY_LP4_ACTIVE PHY_ADRCTL_LPDDR PHY_DFI_PHYUPD_TYPE
DENALI_PHY_908	PHY_AC_BASE_ADDR + 12	RW WR RW RW_D	PHY_CONTINUOUS_CLK_CAL_UPDAT E SC_PHY_UPDATE_CLK_CAL_VALUES PHY_CALVL_RESULT_MASK PHY_LPDDR3_CS
DENALI_PHY_909	PHY_AC_BASE_ADDR + 13	RW RW RW RW	RESERVED RESERVED RESERVED RESERVED

Name	Register Address	Type	PHY Parameter(s)
DENALI_PHY_910	PHY_AC_BASE_ADDR +	RW RW	PHY_PLL_WAIT RESERVED
DENALI_PHY_911	PHY_AC_BASE_ADDR +	RW+ RW+	PHY_PLL_CTRL_CA PHY_PLL_CTRL
DENALI_PHY_912	PHY_AC_BASE_ADDR +	RW+	PHY_PLL_BYPASS
DENALI_PHY_913	PHY_AC_BASE_ADDR +	RW RW+	PHY_PAD_VREF_CTRL_DQ_0 PHY_LOW_FREQ_SEL
DENALI_PHY_914	PHY_AC_BASE_ADDR +	RW RW	PHY_PAD_VREF_CTRL_DQ_2 PHY_PAD_VREF_CTRL_DQ_1
DENALI_PHY_915	PHY_AC_BASE_ADDR +	RW RW	PHY_PAD_VREF_CTRL_AC PHY_PAD_VREF_CTRL_DQ_3
DENALI_PHY_916	PHY_AC_BASE_ADDR +	RW+ RW+	PHY_GRP_SLAVE_DELAY_0 PHY_CSLVL_DLY_STEP
DENALI_PHY_917	PHY_AC_BASE_ADDR +	RW+ RW+	PHY_GRP_SLAVE_DELAY_2 PHY_GRP_SLAVE_DELAY_1
DENALI_PHY_918	PHY_AC_BASE_ADDR +	RW+	PHY_GRP_SLAVE_DELAY_3
DENALI_PHY_919	PHY_AC_BASE_ADDR +	RW RW	PHY_LP4_BOOT_PLL_CTRL_CA PHY_LP4_BOOT_PLL_CTRL
DENALI_PHY_920	PHY_AC_BASE_ADDR +	RD RW	PHY_PLL_OBS_0 PHY_PLL_CTRL_OVERRIDE
DENALI_PHY_921	PHY_AC_BASE_ADDR +	RD RD	PHY_PLL_OBS_2 PHY_PLL_OBS_1
DENALI_PHY_922	PHY_AC_BASE_ADDR + 26	RW RW RD	PHY_TCKSRE_WAIT PHY_PLL_TESTOUT_SEL PHY_PLL_OBS_3
DENALI_PHY_923	PHY_AC_BASE_ADDR +	RW RW RW	PHY_TDFI_PHY_WRDELAY PHY_LS_IDLE_EN PHY_LP_WAKEUP
DENALI_PHY_924	PHY_AC_BASE_ADDR +	RW+	PHY_PAD_FDBK_DRIVE
DENALI_PHY_925	PHY_AC_BASE_ADDR +	RW+	PHY_PAD_FDBK_DRIVE2
DENALI_PHY_926	PHY_AC_BASE_ADDR +	RW+	PHY_PAD_DATA_DRIVE
DENALI_PHY_927	PHY_AC_BASE_ADDR +	RW+	PHY_PAD_DQS_DRIVE
DENALI_PHY_928	PHY_AC_BASE_ADDR +	RW+	PHY_PAD_ADDR_DRIVE
DENALI_PHY_929	PHY_AC_BASE_ADDR +	RW+	PHY_PAD_CLK_DRIVE
DENALI_PHY_930	PHY_AC_BASE_ADDR +	RW+	PHY_PAD_FDBK_TERM
DENALI_PHY_931	PHY_AC_BASE_ADDR +	RW+	PHY_PAD_DATA_TERM
DENALI_PHY_932	PHY_AC_BASE_ADDR +	RW+	PHY_PAD_DQS_TERM
DENALI_PHY_933	PHY_AC_BASE_ADDR +	RW+	PHY_PAD_ADDR_TERM
DENALI_PHY_934	PHY_AC_BASE_ADDR +	RW+	PHY_PAD_CLK_TERM
DENALI_PHY_935	PHY_AC_BASE_ADDR +	RW+	PHY_PAD_CKE_DRIVE
DENALI_PHY_936	PHY_AC_BASE_ADDR +	RW+	PHY_PAD_CKE_TERM
DENALI_PHY_937	PHY_AC_BASE_ADDR +	RW+	PHY_PAD_RST_DRIVE
DENALI_PHY_938	PHY_AC_BASE_ADDR +	RW+	PHY_PAD_RST_TERM
DENALI_PHY_939	PHY_AC_BASE_ADDR +	RW+	PHY_PAD_CS_DRIVE
DENALI_PHY_940	PHY_AC_BASE_ADDR +	RW+	PHY_PAD_CS_TERM
DENALI_PHY_941	PHY_AC_BASE_ADDR +	RW RW	PHY_ADRCTL_LP3_RX_CAL PHY_ADRCTL_RX_CAL

Name	Register Address	Type	PHY Parameter(s)
DENALI_PHY_942	PHY_AC_BASE_ADDR +	RW	PHY_TST_CLK_PAD_CTRL
DENALI_PHY_943	PHY_AC_BASE_ADDR +	RW	PHY_TST_CLK_PAD_CTRL2
DENALI_PHY_944	PHY_AC_BASE_ADDR +	RW RW	PHY_CAL_MODE_0 PHY_TST_CLK_PAD_CTRL3
DENALI_PHY_945	PHY_AC_BASE_ADDR +	WR WR	PHY_CAL_START_0 PHY_CAL_CLEAR_0
DENALI_PHY_946	PHY_AC_BASE_ADDR +	RW	PHY_CAL_INTERVAL_COUNT_0
DENALI_PHY_947	PHY_AC_BASE_ADDR +	RW RW	PHY_CAL_CLK_SELECT_0 PHY_CAL_SAMPLE_WAIT_0
DENALI_PHY_948	PHY_AC_BASE_ADDR +	RD	PHY_CAL_RESULT_OBS_0
DENALI_PHY_949	PHY_AC_BASE_ADDR +	RD	PHY_CAL_RESULT2_OBS_0
DENALI_PHY_950	PHY_AC_BASE_ADDR + 54	WR WR RW	PHY_AC_LPBK_ERR_CLEAR PHY_ADRCTL_MANUAL_UPDATE PHY_PAD_ATB_CTRL
DENALI_PHY_951	PHY_AC_BASE_ADDR + 55	RW RW RW	PHY_AC_LPBK_CONTROL PHY_AC_LPBK_ENABLE PHY_AC_LPBK_OBS_SELECT
DENALI_PHY_952	PHY_AC_BASE_ADDR +	RD	PHY_AC_LPBK_RESULT_OBS
DENALI_PHY_953	PHY_AC_BASE_ADDR + 57	RW RW RW	PHY_AC_CLK_LPBK_CONTROL PHY_AC_CLK_LPBK_ENABLE PHY_AC_CLK_LPBK_OBS_SELECT
DENALI_PHY_954	PHY_AC_BASE_ADDR + 58	RW RW RD	PHY_DATA_BYTE_ORDER_SEL PHY_AC_PWR_RDC_DISABLE PHY_AC_CLK_LPBK_RESULT_OBS
DENALI_PHY_955	PHY_AC_BASE_ADDR + 59	RW RW RW	PHY_CS_DLY_UPT_PER_AC_SLICE PHY_ADRCTL_MSTR_DLY_ENC_SEL PHY_ADR_DISABLE
DENALI_PHY_956	PHY_AC_BASE_ADDR +	RW	PHY_DDL_AC_ENABLE
DENALI_PHY_957	PHY_AC_BASE_ADDR + 61	RW+ RW RW	PHY_DLL_RST_EN PHY_PAD_BACKGROUND_CAL PHY_DDL_AC_MODE
DENALI_PHY_958	PHY_AC_BASE_ADDR + 62	RD RD	PHY_DS_INIT_COMPLETE_OBS PHY_AC_INIT_COMPLETE_OBS

2. PI register

The channel 0 PI base address is 0xffa80800.

The channel 1 PI base address is 0xffa88800.

Name	Offset	Size	Reset Value	Description
PI_REG_0	0x0000	W	0x00000000	DDR PHY Independent Register 0
PI_REG_1	0x0004	W	0x00000000	DDR PHY Independent Register 1
PI_REG_2	0x0008	W	0x00000000	DDR PHY Independent Register 2
PI_REG_3	0x000c	W	0x00000000	DDR PHY Independent Register 3
PI_REG_4	0x0010	W	0x00000000	DDR PHY Independent Register 4
PI_REG_5	0x0014	W	0x00000000	DDR PHY Independent Register 5
PI_REG_6	0x0018	W	0x00000000	DDR PHY Independent Register 6
PI_REG_7	0x001c	W	0x00000000	DDR PHY Independent Register 7
PI_REG_8	0x0020	W	0x00000000	DDR PHY Independent Register 8
PI_REG_9	0x0024	W	0x00000000	DDR PHY Independent Register 9

Name	Offset	Size	Reset Value	Description
PI_REG_10	0x0028	W	0x00000000	DDR PHY Independent Register 10
PI_REG_11	0x002c	W	0x00000000	DDR PHY Independent Register 11
PI_REG_12	0x0030	W	0x00000000	DDR PHY Independent Register 12
PI_REG_13	0x0034	W	0x00000000	DDR PHY Independent Register 13
PI_REG_14	0x0038	W	0x00000000	DDR PHY Independent Register 14
PI_REG_15	0x003c	W	0x00000000	DDR PHY Independent Register 15
PI_REG_16	0x0040	W	0x00000000	DDR PHY Independent Register 16
PI_REG_17	0x0044	W	0x00000000	DDR PHY Independent Register 17
PI_REG_18	0x0048	W	0x00000000	DDR PHY Independent Register 18
PI_REG_19	0x004c	W	0x00000000	DDR PHY Independent Register 19
PI_REG_20	0x0050	W	0x00000000	DDR PHY Independent Register 20
PI_REG_21	0x0054	W	0x00000000	DDR PHY Independent Register 21
PI_REG_22	0x0058	W	0x00010000	DDR PHY Independent Register 22
PI_REG_23	0x005c	W	0x00000000	DDR PHY Independent Register 23
PI_REG_24	0x0060	W	0x00000100	DDR PHY Independent Register 24
PI_REG_25	0x0064	W	0x00000000	DDR PHY Independent Register 25
PI_REG_26	0x0068	W	0x00000000	DDR PHY Independent Register 26
PI_REG_27	0x006c	W	0x00000000	DDR PHY Independent Register 27
PI_REG_28	0x0070	W	0x00000000	DDR PHY Independent Register 28
PI_REG_29	0x0074	W	0x00000000	DDR PHY Independent Register 29
PI_REG_30	0x0078	W	0x00000000	DDR PHY Independent Register 30
PI_REG_31	0x007c	W	0x00000000	DDR PHY Independent Register 31
PI_REG_32	0x0080	W	0x00000000	DDR PHY Independent Register 32
PI_REG_33	0x0084	W	0x00000000	DDR PHY Independent Register 33
PI_REG_34	0x0088	W	0x00000000	DDR PHY Independent Register 34
PI_REG_35	0x008c	W	0x00000000	DDR PHY Independent Register 35
PI_REG_36	0x0090	W	0x00000000	DDR PHY Independent Register 36
PI_REG_37	0x0094	W	0x00000000	DDR PHY Independent Register 37
PI_REG_38	0x0098	W	0x00000000	DDR PHY Independent Register 38
PI_REG_39	0x009c	W	0x00000000	DDR PHY Independent Register 39
PI_REG_40	0x00a0	W	0x00000000	DDR PHY Independent Register 40
PI_REG_41	0x00a4	W	0x00000101	DDR PHY Independent Register 41
PI_REG_42	0x00a8	W	0x00000000	DDR PHY Independent Register 42
PI_REG_43	0x00ac	W	0x00000000	DDR PHY Independent Register 43
PI_REG_44	0x00b0	W	0x00000000	DDR PHY Independent Register 44
PI_REG_45	0x00b4	W	0x00000000	DDR PHY Independent Register 45
PI_REG_46	0x00b8	W	0x00000000	DDR PHY Independent Register 46
PI_REG_47	0x00bc	W	0x00000000	DDR PHY Independent Register 47
PI_REG_48	0x00c0	W	0x00000000	DDR PHY Independent Register 48
PI_REG_49	0x00c4	W	0x00000000	DDR PHY Independent Register 49
PI_REG_50	0x00c8	W	0x00000000	DDR PHY Independent Register 50
PI_REG_51	0x00cc	W	0x00000000	DDR PHY Independent Register 51
PI_REG_52	0x00d0	W	0x00000000	DDR PHY Independent Register 52
PI_REG_53	0x00d4	W	0x00000000	DDR PHY Independent Register 53

Name	Offset	Size	Reset Value	Description
PI_REG_54	0x00d8	W	0x00000000	DDR PHY Independent Register 54
PI_REG_55	0x00dc	W	0x00000000	DDR PHY Independent Register 55
PI_REG_56	0x00e0	W	0x00000000	DDR PHY Independent Register 56
PI_REG_57	0x00e4	W	0x00000000	DDR PHY Independent Register 57
PI_REG_58	0x00e8	W	0x00000100	DDR PHY Independent Register 58
PI_REG_59	0x00ec	W	0x00000000	DDR PHY Independent Register 59
PI_REG_60	0x00f0	W	0x00000000	DDR PHY Independent Register 60
PI_REG_61	0x00f4	W	0x00000000	DDR PHY Independent Register 61
PI_REG_62	0x00f8	W	0x00000000	DDR PHY Independent Register 62
PI_REG_63	0x00fc	W	0x00000000	DDR PHY Independent Register 63
PI_REG_64	0x0100	W	0x00000000	DDR PHY Independent Register 64
PI_REG_65	0x0104	W	0x00000000	DDR PHY Independent Register 65
PI_REG_66	0x0108	W	0x00000000	DDR PHY Independent Register 66
PI_REG_67	0x010c	W	0x00000000	DDR PHY Independent Register 67
PI_REG_68	0x0110	W	0x00000000	DDR PHY Independent Register 68
PI_REG_69	0x0114	W	0x00000000	DDR PHY Independent Register 69
PI_REG_70	0x0118	W	0x00000000	DDR PHY Independent Register 70
PI_REG_71	0x011c	W	0x00000000	DDR PHY Independent Register 71
PI_REG_72	0x0120	W	0x00000000	DDR PHY Independent Register 72
PI_REG_73	0x0124	W	0x00000000	DDR PHY Independent Register 73
PI_REG_74	0x0128	W	0x00000000	DDR PHY Independent Register 74
PI_REG_75	0x012c	W	0x00000000	DDR PHY Independent Register 75
PI_REG_76	0x0130	W	0x00000000	DDR PHY Independent Register 76
PI_REG_77	0x0134	W	0x00000000	DDR PHY Independent Register 77
PI_REG_78	0x0138	W	0x00000000	DDR PHY Independent Register 78
PI_REG_79	0x013c	W	0x00000000	DDR PHY Independent Register 79
PI_REG_80	0x0140	W	0x00000000	DDR PHY Independent Register 80
PI_REG_81	0x0144	W	0x00000000	DDR PHY Independent Register 81
PI_REG_82	0x0148	W	0x00000000	DDR PHY Independent Register 82
PI_REG_83	0x014c	W	0x00000000	DDR PHY Independent Register 83
PI_REG_84	0x0150	W	0x00000000	DDR PHY Independent Register 84
PI_REG_85	0x0154	W	0x00000000	DDR PHY Independent Register 85
PI_REG_86	0x0158	W	0x00000000	DDR PHY Independent Register 86
PI_REG_87	0x015c	W	0x00000000	DDR PHY Independent Register 87
PI_REG_88	0x0160	W	0x00000000	DDR PHY Independent Register 88
PI_REG_89	0x0164	W	0x00000000	DDR PHY Independent Register 89
PI_REG_90	0x0168	W	0x00000000	DDR PHY Independent Register 90
PI_REG_91	0x016c	W	0x00000000	DDR PHY Independent Register 91
PI_REG_92	0x0170	W	0x00000000	DDR PHY Independent Register 92
PI_REG_93	0x0174	W	0x00000000	DDR PHY Independent Register 93
PI_REG_94	0x0178	W	0x00000000	DDR PHY Independent Register 94
PI_REG_95	0x017c	W	0x00000000	DDR PHY Independent Register 95
PI_REG_96	0x0180	W	0x00000000	DDR PHY Independent Register 96
PI_REG_97	0x0184	W	0x00000000	DDR PHY Independent Register 97

Name	Offset	Size	Reset Value	Description
PI_REG_98	0x0188	W	0x00000000	DDR PHY Independent Register 98
PI_REG_99	0x018c	W	0x00000000	DDR PHY Independent Register 99
PI_REG_100	0x0190	W	0x00000000	DDR PHY Independent Register 100
PI_REG_101	0x0194	W	0x00000000	DDR PHY Independent Register 101
PI_REG_102	0x0198	W	0x00000000	DDR PHY Independent Register 102
PI_REG_103	0x019c	W	0x00000000	DDR PHY Independent Register 103
PI_REG_104	0x01a0	W	0x00000000	DDR PHY Independent Register 104
PI_REG_105	0x01a4	W	0x00000000	DDR PHY Independent Register 105
PI_REG_106	0x01a8	W	0x00000000	DDR PHY Independent Register 106
PI_REG_107	0x01ac	W	0x00000000	DDR PHY Independent Register 107
PI_REG_108	0x01b0	W	0x00000000	DDR PHY Independent Register 108
PI_REG_109	0x01b4	W	0x00000000	DDR PHY Independent Register 109
PI_REG_110	0x01b8	W	0x00000000	DDR PHY Independent Register 110
PI_REG_111	0x01bc	W	0x00000000	DDR PHY Independent Register 111
PI_REG_112	0x01c0	W	0x00000000	DDR PHY Independent Register 112
PI_REG_113	0x01c4	W	0x00000000	DDR PHY Independent Register 113
PI_REG_114	0x01c8	W	0x00000000	DDR PHY Independent Register 114
PI_REG_115	0x01cc	W	0x00000000	DDR PHY Independent Register 115
PI_REG_116	0x01d0	W	0x00000000	DDR PHY Independent Register 116
PI_REG_117	0x01d4	W	0x00000000	DDR PHY Independent Register 117
PI_REG_118	0x01d8	W	0x00000000	DDR PHY Independent Register 118
PI_REG_119	0x01dc	W	0x00000000	DDR PHY Independent Register 119
PI_REG_120	0x01e0	W	0x00000000	DDR PHY Independent Register 120

Name	Offset	Size	Reset Value	Description
PI_REG_121	0x01e4	W	0x00000000	DDR PHY Independent Register 121
PI_REG_122	0x01e8	W	0x00000000	DDR PHY Independent Register 122
PI_REG_123	0x01ec	W	0x00000000	DDR PHY Independent Register 123
PI_REG_124	0x01f0	W	0x00000000	DDR PHY Independent Register 124
PI_REG_125	0x01f4	W	0x00000000	DDR PHY Independent Register 125
PI_REG_126	0x01f8	W	0x00000000	DDR PHY Independent Register 126
PI_REG_127	0x01fc	W	0x00000000	DDR PHY Independent Register 127
PI_REG_128	0x0200	W	0x00000000	DDR PHY Independent Register 128
PI_REG_129	0x0204	W	0x00000000	DDR PHY Independent Register 129
PI_REG_130	0x0208	W	0x00000000	DDR PHY Independent Register 130
PI_REG_131	0x020c	W	0x00000000	DDR PHY Independent Register 131
PI_REG_132	0x0210	W	0x00000000	DDR PHY Independent Register 132
PI_REG_133	0x0214	W	0x00000000	DDR PHY Independent Register 133
PI_REG_134	0x0218	W	0x00000000	DDR PHY Independent Register 134
PI_REG_135	0x021c	W	0x00000000	DDR PHY Independent Register 135
PI_REG_136	0x0220	W	0x00000000	DDR PHY Independent Register 136
PI_REG_137	0x0224	W	0x00000000	DDR PHY Independent Register 137
PI_REG_138	0x0228	W	0x00000000	DDR PHY Independent Register 138
PI_REG_139	0x022c	W	0x00000000	DDR PHY Independent Register 139
PI_REG_140	0x0230	W	0x00000000	DDR PHY Independent Register 140
PI_REG_155	0x026c	W	0x00000000	DDR PHY Independent Register 155
PI_REG_156	0x0270	W	0x00000000	DDR PHY Independent Register 156

Name	Offset	Size	Reset Value	Description
PI_REG_157	0x0274	W	0x00000000	DDR PHY Independent Register 157
PI_REG_158	0x0278	W	0x00000000	DDR PHY Independent Register 158
PI_REG_159	0x027c	W	0x00000000	DDR PHY Independent Register 159
PI_REG_160	0x0280	W	0x00000000	DDR PHY Independent Register 160
PI_REG_161	0x0284	W	0x00000000	DDR PHY Independent Register 161
PI_REG_162	0x0288	W	0x00000000	DDR PHY Independent Register 162
PI_REG_163	0x028c	W	0x00000000	DDR PHY Independent Register 163
PI_REG_164	0x0290	W	0x00000000	DDR PHY Independent Register 164
PI_REG_165	0x0294	W	0x00000000	DDR PHY Independent Register 165
PI_REG_166	0x0298	W	0x00000000	DDR PHY Independent Register 166
PI_REG_167	0x029c	W	0x00000000	DDR PHY Independent Register 167
PI_REG_168	0x02a0	W	0x00000000	DDR PHY Independent Register 168
PI_REG_169	0x02a4	W	0x00000000	DDR PHY Independent Register 169
PI_REG_174	0x02b8	W	0x00000000	DDR PHY Independent Register 174
PI_REG_175	0x02bc	W	0x00000000	DDR PHY Independent Register 175
PI_REG_176	0x02c0	W	0x00000000	DDR PHY Independent Register 176
PI_REG_186	0x02e8	W	0x00000000	DDR PHY Independent Register 186
PI_REG_187	0x02ec	W	0x00000000	DDR PHY Independent Register 187
PI_REG_188	0x02f0	W	0x00000000	DDR PHY Independent Register 188
PI_REG_189	0x02f4	W	0x00000000	DDR PHY Independent Register 189
PI_REG_190	0x02f8	W	0x00000000	DDR PHY Independent Register 190
PI_REG_191	0x02fc	W	0x00000000	DDR PHY Independent Register 191

Name	Offset	Size	Reset Value	Description
PI_REG_192	0x0300	W	0x00000000	DDR PHY Independent Register 192
PI_REG_193	0x0304	W	0x00000000	DDR PHY Independent Register 193
PI_REG_199	0x031c	W	0x00000000	DDR PHY Independent Register 199

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

3. CIC register

The CIC base address is 0xff620000.

Name	Offset	Size	Reset Value	Description
CIC_CTRL0	0x0000	W	0x00000000	DDR Controller LP Interface Control Register 0
CIC_CTRL1	0x0004	W	0x00000000	DDR Controller LP Interface Control Register 1
CIC_IDLE_TH	0x0008	W	0x00000000	DDR Controller LP Interface Idle Threshold in standby mode
CIC_CG_WAIT_TH	0x000c	W	0x00000000	DDR Controller LP Interface CG Wait Threshold in standby mode
CIC_STATUS0	0x0010	W	0x00000000	DDR Controller LP Interface Status Register 0
CIC_STATUS1	0x0014	W	0x00000000	DDR Controller LP Interface Status Register 1
CIC_CTRL2	0x0018	W	0x00000a0a	DDR Controller LP Interface Control Register 2
CIC_CTRL3	0x001c	W	0x00000101	DDR Controller LP Interface Control Register 3
CIC_CTRL4	0x0020	W	0x00008a8a	DDR Controller LP Interface Control Register 4
CIC_STATUS2	0x0040	W	0x00000000	DDR Controller LP Interface Status Register 2

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

4. DDR monitor register

The monitor base address is 0xff630000.

Name	Offset	Size	Reset Value	Description
DDRMON_IP_VERSION	0x0000	W	0x00000000	DDR Monitor IP Version
DDRMON_CTRL	0x0004	W	0x00000008	DDR Monitor Control Register
DDRMON_INT_STATUS	0x0008	W	0x00000000	Interrupt Status
DDRMON_INT_MASK	0x000c	W	0x00000000	Interrupt mask control
DDRMON_TIMER_COUNT	0x0010	W	0x00000000	The DFI Timer Threshold
DDRMON_FLOOR_NUMBER	0x0014	W	0x00000000	The Low Threshold in the Comparison of DDR Access
DDRMON_TOP_NUMBER	0x0018	W	0x00000000	The High Threshold in the Comparison of DDR Access

Name	Offset	Size	Reset Value	Description
DDRMON_CH0_DFI_ACT_NUM	0x001c	W	0x00000000	Channel 0 DFI Active Command Number
DDRMON_CH0_DFI_WR_NUM	0x0020	W	0x00000000	Channel 0 DFI write Command Number
DDRMON_CH0_DFI_RD_NUM	0x0024	W	0x00000000	Channel 0 DFI read Command Number
DDRMON_CH0_COUNT_NUM	0x0028	W	0x00000000	Channel 0 Timer Count Number
DDRMON_CH0_DFI_ACCESS_NUM	0x002c	W	0x00000000	Channel 0 DFI Read and Write Command Number
DDRMON_CH1_DFI_ACT_NUM	0x0030	W	0x00000000	Channel 1 DFI Active Command Number
DDRMON_CH1_DFI_WR_NUM	0x0034	W	0x00000000	Channel 1 DFI write Command Number
DDRMON_CH1_DFI_RD_NUM	0x0038	W	0x00000000	Channel 1 DFI read Command Number
DDRMON_CH1_COUNT_NUM	0x003c	W	0x00000000	Channel 1 Timer Count Number
DDRMON_CH1_DFI_ACCESS_NUM	0x0040	W	0x00000000	Channel 1 DFI Read and Write Command Number
DDRMON_DDR_IF_CTRL	0x0200	W	0x00000000	DDR interface Control Register
DDRMON_CH0_WR_START_ADDR	0x020c	W	0x00000000	Channel 0 Write Start Address
DDRMON_CH0_WR_END_ADDR	0x0210	W	0x00000000	Channel 0 Write End Address
DDRMON_CH0_RD_START_ADDR	0x0214	W	0x00000000	Channel 0 Read Start Address
DDRMON_CH0_RD_END_ADDR	0x0218	W	0x00000000	Channel 0 Read End Address
DDRMON_CH1_WR_START_ADDR	0x0224	W	0x00000000	Channel 1 Write Start Address
DDRMON_CH1_WR_END_ADDR	0x0228	W	0x00000000	Channel 1 Write End Address
DDRMON_CH1_RD_START_ADDR	0x022c	W	0x00000000	Channel 1 Read Start Address
DDRMON_CH1_RD_END_ADDR	0x0230	W	0x00000000	Channel 1 Read End Address
DDRMON_CH0_DDR_FIFO0_ADDR	0x0240	W	0x00000000	DDR Channel 0 Controller Interface Address FIFO0
DDRMON_CH0_DDR_FIFO1_ADDR	0x0248	W	0x00000000	DDR Channel 0 Controller Interface Address FIFO1
DDRMON_CH0_DDR_FIFO2_ADDR	0x0250	W	0x00000000	DDR Channel 0 Controller Interface Address FIFO2
DDRMON_CH0_DDR_FIFO3_ADDR	0x0258	W	0x00000000	DDR Channel 0 Controller Interface Address FIFO3

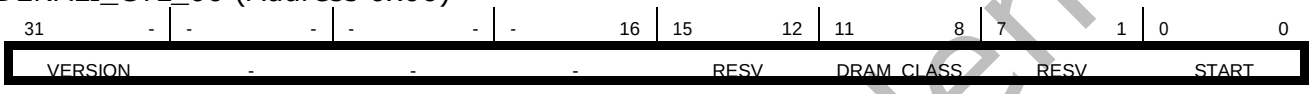
Name	Offset	Size	Reset Value	Description
DDRMON_CH1_DDR_FIFO0_ADDR	0x0260	W	0x00000000	DDR Channel 1 Controller Interface Address FIFO0
DDRMON_CH1_DDR_FIFO1_ADDR	0x0268	W	0x00000000	DDR Channel 1 Controller Interface Address FIFO1
DDRMON_CH1_DDR_FIFO2_ADDR	0x0270	W	0x00000000	DDR Channel 1 Controller Interface Address FIFO2
DDRMON_CH1_DDR_FIFO3_ADDR	0x0278	W	0x00000000	DDR Channel 1 Controller Interface Address FIFO3

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

9.4.2 Detail Register Description

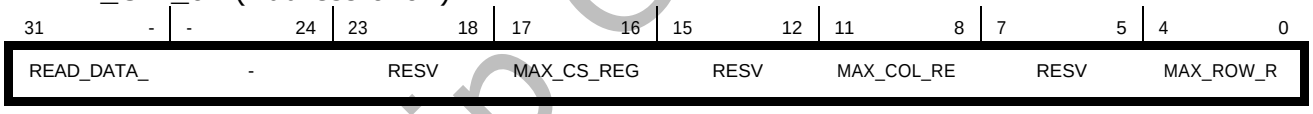
1. DDR controller/phy register

DENALI_CTL_00 (Address 0x00)



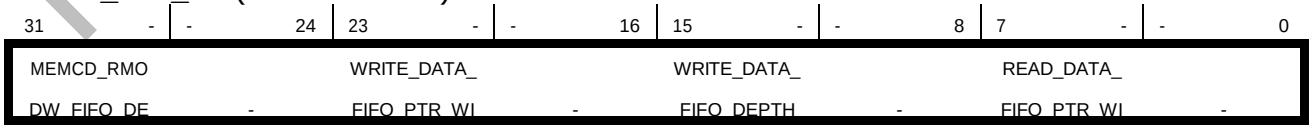
Name	Bits	Default	Range	Description
VERSION	31:16	0x2041	0x2041	Holds the controller version
DRAM_CLASS	11:8	0x0	0x0-0xf	Defines the class of DRAM memory which is connected to the
START	0	0x0	0x0-0x1	Initiate command processing in the

DENALI_CTL_01 (Address 0x01)



Name	Bits	Default	Range	Description
READ_DATA_FIFO_DEPTH	31:24	0x00	0x0-0xff	Reports the depth of the controller core read data queue. READ-
MAX_CS_REG	17:16	0x2	0x0-0x2	Holds the maximum number of chip
MAX_COL_REG	11:8	0xc	0x0-0xc	Holds the maximum width of column address in DRAMs. READ-
MAX_ROW_REG	4:0	0x10	0x0-0x10	Holds the maximum width of

DENALI_CTL_02 (Address 0x02)



Name	Bits	Default	Range	Description
MEMCD_RMODW_FIFO_DEPTH	31:24	0x00	0x0-0xff	Reports the depth of the controller core read/modify/write FIFO.
WRITE_DATA_FIFO_PTR_WIDTH	23:16	0x00	0x0-0xff	Reports the width of the controller core write data latency queue

WRITE_DATA_FIFO_DEPTH	15:8	0x00	0x0-0xff	Reports the depth of the controller core write data latency queue.
READ_DATA_FIFO_PTR_WIDTH	7:0	0x00	0x0-0xff	Reports the width of the controller core read data queue pointer.

DENALI_CTL_03 (Address 0x03)

31 - - 24	23 - - 16	15 - - 8	7 - - 0
DENALI0_WR FIFO_LOG2_D -	DENALI0_RM ODWFIFO_LO -	DENALI0_CM DFIFO_LOG2 -	MEMCD_RMO DW_FIFO_PT -

Name	Bits	Default	Range	Description
DENALI0_WRFIFO_LOG2_DEPTH	31:24	0x00	0x0-0xff	Reports the depth of the DENALI port 0 write data FIFO. Value is the
DENALI0_RMODWFIFO_LOG2_DEPTH	23:16	0x00	0x0-0xff	Reports the depth of the DENALI port 0 read/modify/write FIFO.
DENALI0_CMDFIFO_LOG2_DEPTH	15:8	0x00	0x0-0xff	Reports the depth of the DENALI port 0 command FIFO. Value is the
MEMCD_RMODW_FIFO_PTR_WIDTH	7:0	0x00	0x0-0xff	Reports the width of the controller core read/modify/write FIFO

DENALI_CTL_04 (Address 0x04)

31 - - - - - 16	15 9	8 8	7 - - 0
OBSOLETE - - -	RESV	DFS_CLOSE_	DENALI0_WR CMD_SIDE_FI -

Name	Bits	Default	Range	Description
DFS_CLOSE_BANKS	8	0x0	0x0-0x1	Close all pages before doing DFS.
DENALI0_WRCMD_SIDE_FIFO_LOG2_DE	7:0	0x00	0x0-0xff	Reports the depth of the DENALI port 0 processing FIFO. Value is

DENALI_CTL_05 (Address 0x05)

31 - - 24	23 - - 0
OBSOLETE -	TINIT_F0 -

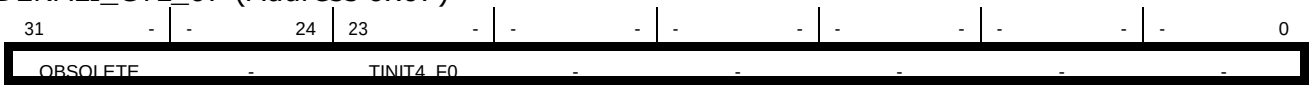
Name	Bits	Default	Range	Description
TINIT_F0	23:0	0x000000	0x0-0xffffff	DRAM TINIT value for frequency

DENALI_CTL_06 (Address 0x06)

31 - - 24	23 - - 0
OBSOLETE -	TINIT3_F0 -

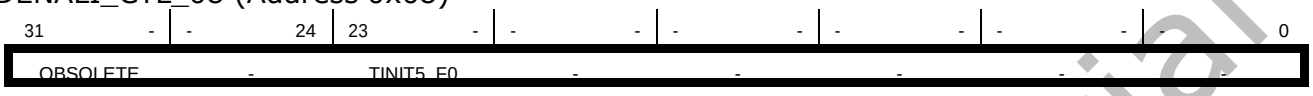
Name	Bits	Default	Range	Description
TINIT3_F0	23:0	0x000000	0x0-0xffffff	DRAM TINIT3 value for frequency

DENALI_CTL_07 (Address 0x07)



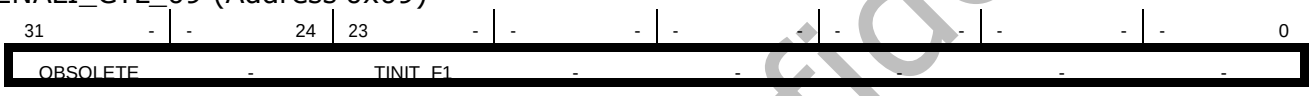
Name	Bits	Default	Range	Description
TINIT4_F0	23:0	0x000000	0x0-0xffffff	DRAM TINIT4 value for frequency

DENALI_CTL_08 (Address 0x08)



Name	Bits	Default	Range	Description
TINIT5_F0	23:0	0x000000	0x0-0xffffff	DRAM TINIT5 value for frequency

ENALI_CTL_09 (Address 0x09)

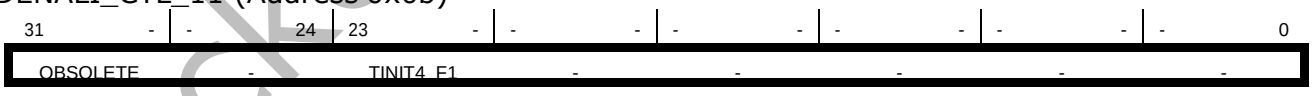


Name	Bits	Default	Range	Description
TINIT_F1	23:0	0x000000	0x0-0xffffff	DRAM TINIT value for frequency

DENALI_CTL_10 (Address 0x0a)

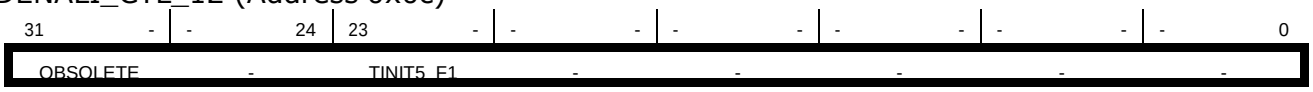
Name	Bits	Default	Range	Description
TINIT3_F1	23:0	0x000000	0x0-0xffffff	DRAM TINIT3 value for frequency

DENALI_CTL_11 (Address 0x0b)



Name	Bits	Default	Range	Description
TINIT4_F1	23:0	0x000000	0x0-0xffffff	DRAM TINIT4 value for frequency

DENALI_CTL_12 (Address 0x0c)

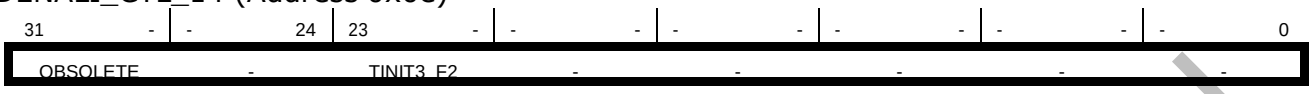


Name	Bits	Default	Range	Description
TINIT5_F1	23:0	0x000000	0x0-0xffffff	DRAM TINIT5 value for frequency

DENALI_CTL_13 (Address 0x0d)

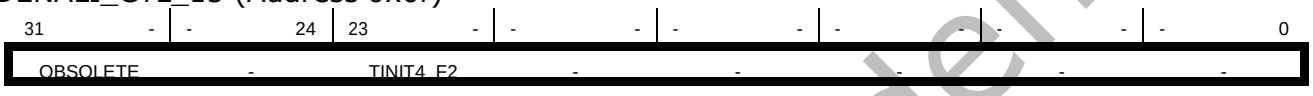
Name	Bits	Default	Range	Description
TINIT_F2	23:0	0x000000	0x0-0xffffff	DRAM TINIT value for frequency

DENALI_CTL_14 (Address 0x0e)



Name	Bits	Default	Range	Description
TINIT3_F2	23:0	0x000000	0x0-0xffffff	DRAM TINIT3 value for frequency

DENALI_CTL_15 (Address 0x0f)

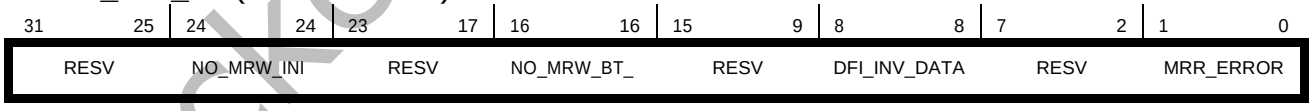


Name	Bits	Default	Range	Description
TINIT4_F2	23:0	0x000000	0x0-0xffffff	DRAM TINIT4 value for frequency

DENALI_CTL_16 (Address 0x10)

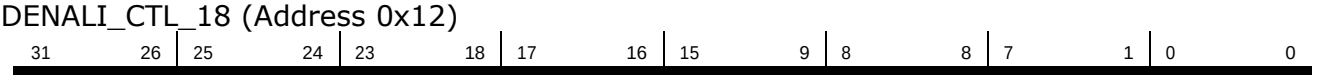
Name	Bits	Default	Range	Description
NO_AUTO_MRR_INIT	24	0x0	0x0-0x1	Disable MRR commands during
TINIT5_F2	23:0	0x000000	0x0-0xffffff	DRAM TINIT5 value for frequency

DENALI_CTL_17 (Address 0x11)



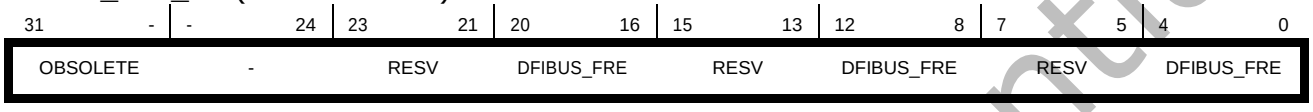
Name	Bits	Default	Range	Description
NO_MRW_INIT	24	0x0	0x0-0x1	Disable MRW commands after training during initialization. Set to 1
NO_MRW_BT_INIT	16	0x0	0x0-0x1	Disable MRW commands before training during initialization. Set to 1
DFI_INV_DATA_CS	8	0x0	0x0-0x1	Forces the inversion of the dfi_rddata_cs_n_X and
MRR_ERROR_STATUS	1:0	0x0	0x0-0x3	Identifies the source of any MRR errors. Value of 1 indicates a

DENALI_CTL_18 (Address 0x12)



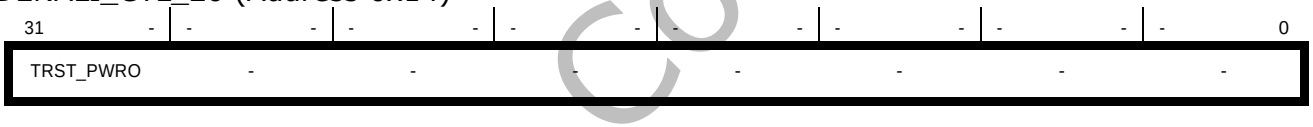
Name	Bits	Default	Range	Description
DFIBUS_BOOT_FREQ	25:24	0x0	0x0-0x3	Defines the DFI bus boot
DFIBUS_FREQ_INIT	17:16	0x0	0x0-0x3	Defines the initial DFI bus
PHY_INDEP_TRAIN_MODE	8	0x0	0x0-0x1	Enable PHY independent training mode commands during
NO_PHY_IND_TRAIN_INIT	0	0x0	0x0-0x1	Disable PHY Independent Training during initialization. Set to 1 to

DENALI_CTL_19 (Address 0x13)



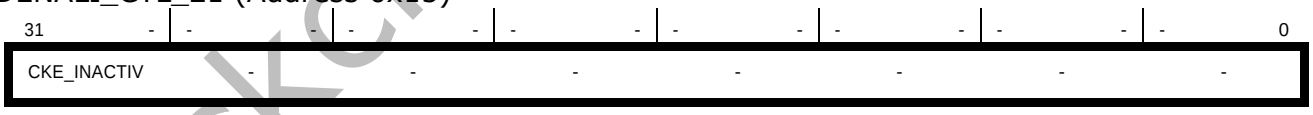
Name	Bits	Default	Range	Description
DFIBUS_FREQ_F2	20:16	0x00	0x0-0x1f	Defines the DFI bus frequency for
DFIBUS_FREQ_F1	12:8	0x00	0x0-0x1f	Defines the DFI bus frequency for
DFIBUS_FREQ_F0	4:0	0x00	0x0-0x1f	Defines the DFI bus frequency for

DENALI_CTL_20 (Address 0x14)



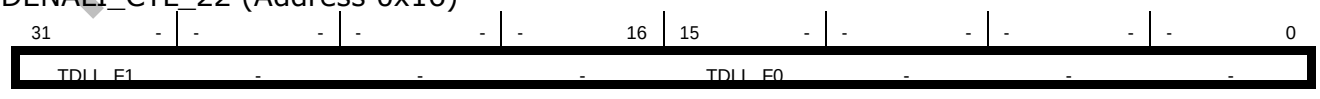
Name	Bits	Default	Range	Description
TRST_PWRON	31:0	0x00000000	0x0-0xffffffff	Duration of memory reset during

DENALI_CTL_21 (Address 0x15)



Name	Bits	Default	Range	Description
CKE_INACTIVE	31:0	0x00000000	0x0-0xffffffff	Number of cycles after reset before

DENALI_CTL_22 (Address 0x16)



Name	Bits	Default	Range	Description
TDLL_F1	31:16	0x0000	0x0-0xffff	DRAM TDLL value for frequency
TDLL_F0	15:0	0x0000	0x0-0xffff	DRAM TDLL value for frequency

DENALI_CTL_23 (Address 0x17)

31 29	28 24	23 23	22 16	15 -	- -	- -	- 0
RESV	WRLAT_F0	RESV	CASLAT_LIN_	TDLL_F2	-	-	-

Name	Bits	Default	Range	Description
WRLAT_F0	28:24	0x00	0x0-0x1f	DRAM WRLAT value for frequency
CASLAT_LIN_F0	22:16	0x00	0x0-0x7f	Sets latency from read command send to data receive from/to controller for frequency copy 0. Bit
TDLL_F2	15:0	0x0000	0x0-0xffff	DRAM TDLL value for frequency

DENALI_CTL_24 (Address 0x18)

31 30	29 24	23 21	20 16	15 15	14 8	7 6	5 0
RESV	ADDITIVE_LAT_F1	RESV	WRLAT_F1	RESV	CASLAT_LIN_	RESV	ADDITIVE_LAT_F0

Name	Bits	Default	Range	Description
ADDITIVE_LAT_F1	29:24	0x00	0x0-0x3f	DRAM additive latency value for
WRLAT_F1	20:16	0x00	0x0-0x1f	DRAM WRLAT value for frequency
CASLAT_LIN_F1	14:8	0x00	0x0-0x7f	Sets latency from read command send to data receive from/to controller for frequency copy 1. Bit
ADDITIVE_LAT_F0	5:0	0x00	0x0-0x3f	DRAM additive latency value for

DENALI_CTL_25 (Address 0x19)

31 27	26 24	23 22	21 16	15 13	12 8	7 7	6 0
RESV	TBST_INT_INT	RESV	ADDITIVE_LAT_F2	RESV	WRLAT_F2	RESV	CASLAT_LIN_

Name	Bits	Default	Range	Description
TBST_INT_INTERVAL	26:24	0x0	0x1-0x7	DRAM burst interrupt interval value
ADDITIVE_LAT_F2	21:16	0x00	0x0-0x3f	DRAM additive latency value for
WRLAT_F2	12:8	0x00	0x0-0x1f	DRAM WRLAT value for frequency
CASLAT_LIN_F2	6:0	0x00	0x0-0x7f	Sets latency from read command send to data receive from/to controller for frequency copy 2. Bit

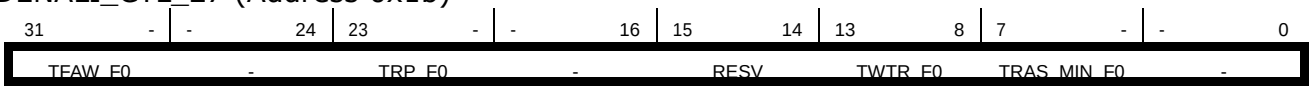
DENALI_CTL_26 (Address 0x1a)

31 -	- 24	23 -	- 16	15 14	13 8	7 5	4 0
TRC_F0	-	TRRD_F0	-	RESV	TCCDMW	RESV	TCCD

Name	Bits	Default	Range	Description
TRC_F0	31:24	0x00	0x0-0xff	DRAM TRC value for frequency

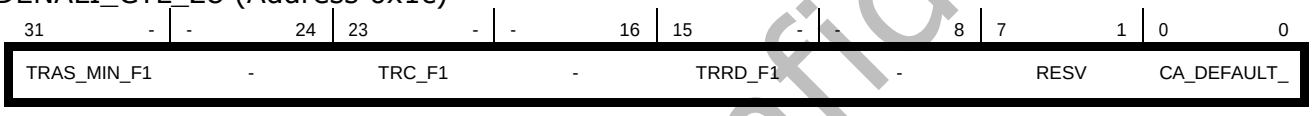
TRRD_F0	23:16	0x00	0x0-0xff	DRAM TRRD value for frequency
TCCDMW	13:8	0x00	0x1-0x3f	DRAM CAS-to-CAS masked write
TCCD	4:0	0x00	0x1-0x1f	DRAM CAS-to-CAS value in

DENALI_CTL_27 (Address 0x1b)



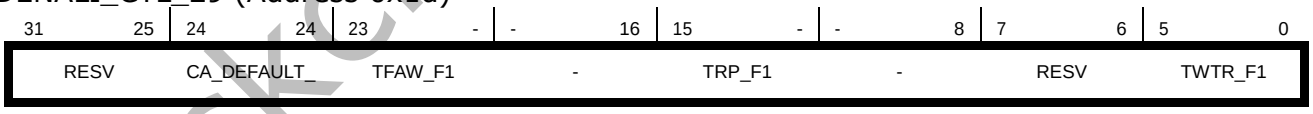
Name	Bits	Default	Range	Description
TFAW_F0	31:24	0x00	0x0-0xff	DRAM TFAW value for frequency
TRP_F0	23:16	0x00	0x0-0xff	DRAM TRP value for frequency
TWTR_F0	13:8	0x00	0x0-0x3f	DRAM TWTR value for frequency
TRAS_MIN_F0	7:0	0x00	0x0-0xff	DRAM TRAS_MIN value for

DENALI_CTL_28 (Address 0x1c)



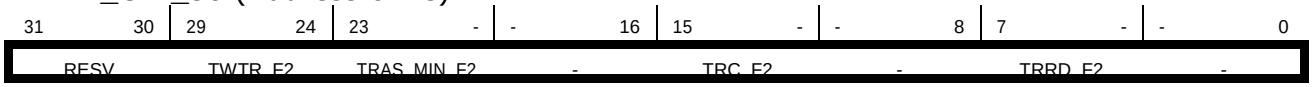
Name	Bits	Default	Range	Description
TRAS_MIN_F1	31:24	0x00	0x0-0xff	DRAM TRAS_MIN value for
TRC_F1	23:16	0x00	0x0-0xff	DRAM TRC value for frequency
TRRD_F1	15:8	0x00	0x0-0xff	DRAM TRRD value for frequency
CA_DEFAULT_VAL_F0	0	0x0	0x0-0x1	Defines how unused address/ command bits are driven for

DENALI_CTL_29 (Address 0x1d)



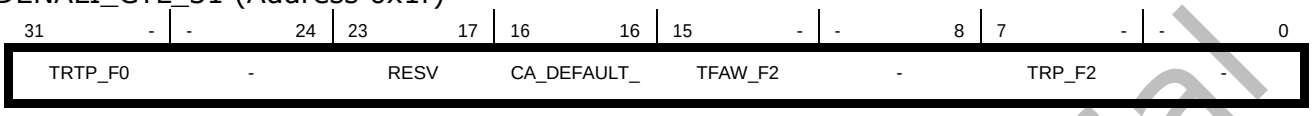
Name	Bits	Default	Range	Description
CA_DEFAULT_VAL_F1	24	0x0	0x0-0x1	Defines how unused address/ command bits are driven for
TFAW_F1	23:16	0x00	0x0-0xff	DRAM TFAW value for frequency
TRP_F1	15:8	0x00	0x0-0xff	DRAM TRP value for frequency
TWTR_F1	5:0	0x00	0x0-0x3f	DRAM TWTR value for frequency

DENALI_CTL_30 (Address 0x1e)



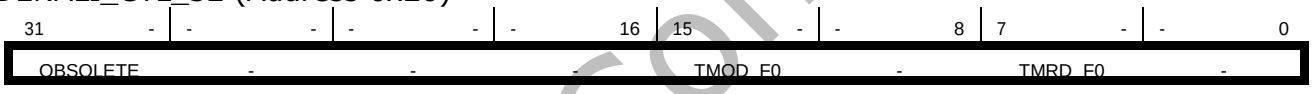
Name	Bits	Default	Range	Description
TWTR_F2	29:24	0x00	0x0-0x3f	DRAM TWTR value for frequency
TRAS_MIN_F2	23:16	0x00	0x0-0xff	DRAM TRAS_MIN value for
TRC_F2	15:8	0x00	0x0-0xff	DRAM TRC value for frequency
TRRD_F2	7:0	0x00	0x0-0xff	DRAM TRRD value for frequency

DENALI_CTL_31 (Address 0x1f)



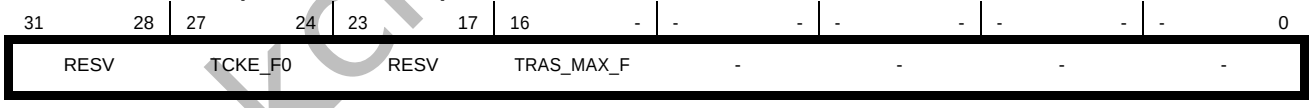
Name	Bits	Default	Range	Description
TRTP_F0	31:24	0x00	0x0-0xff	DRAM TRTP value for frequency
CA_DEFAULT_VAL_F2	16	0x0	0x0-0x1	Defines how unused address/ command bits are driven for
TFAW_F2	15:8	0x00	0x0-0xff	DRAM TFAW value for frequency
TRP_F2	7:0	0x00	0x0-0xff	DRAM TRP value for frequency

DENALI_CTL_32 (Address 0x20)



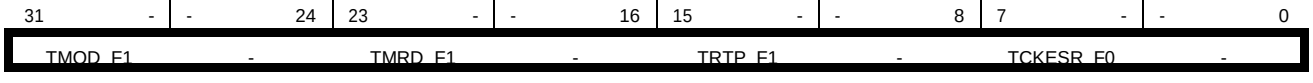
Name	Bits	Default	Range	Description
TMOD_F0	15:8	0x00	0x0-0xff	DRAM TMOD value for frequency
TMRD_F0	7:0	0x00	0x0-0xff	DRAM TMRD value for frequency

DENALI_CTL_33 (Address 0x21)



Name	Bits	Default	Range	Description
TCKE_F0	27:24	0x0	0x0-0xf	Minimum CKE pulse width for
TRAS_MAX_F0	16:0	0x00000	0x0-0x1ffff	DRAM TRAS_MAX value for

DENALI_CTL_34 (Address 0x22)



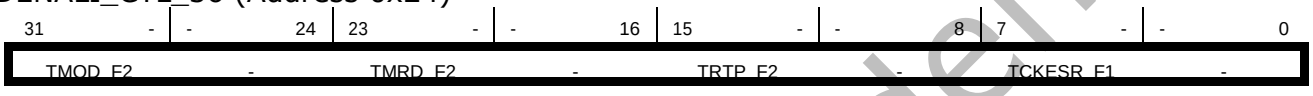
Name	Bits	Default	Range	Description
TMOD_F1	31:24	0x00	0x0-0xff	DRAM TMOD value for frequency
TMRD_F1	23:16	0x00	0x0-0xff	DRAM TMRD value for frequency

TRTP_F1	15:8	0x00	0x0-0xff	DRAM TRTP value for frequency
TCKESR_F0	7:0	0x00	0x0-0xff	Minimum CKE low pulse width during a self-refresh for frequency

DENALI_CTL_35 (Address 0x23)

Name	Bits	Default	Range	Description
TCKE_F1	27:24	0x0	0x0-0xf	Minimum CKE pulse width for
TRAS_MAX_F1	16:0	0x00000	0x0-0x1ffff	DRAM TRAS_MAX value for

DENALI_CTL_36 (Address 0x24)

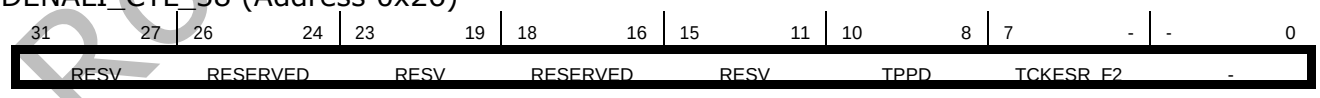


Name	Bits	Default	Range	Description
TMOD_F2	31:24	0x00	0x0-0xff	DRAM TMOD value for frequency
TMRD_F2	23:16	0x00	0x0-0xff	DRAM TMRD value for frequency
TRTP_F2	15:8	0x00	0x0-0xff	DRAM TRTP value for frequency
TCKESR_F1	7:0	0x00	0x0-0xff	Minimum CKE low pulse width during a self-refresh for frequency

DENALI_CTL_37 (Address 0x25)

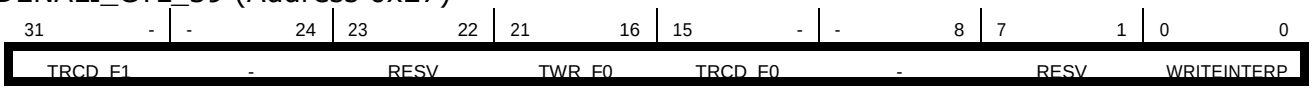
Name	Bits	Default	Range	Description
TCKE_F2	27:24	0x0	0x0-0xf	Minimum CKE pulse width for
TRAS_MAX_F2	16:0	0x00000	0x0-0x1ffff	DRAM TRAS_MAX value for

DENALI_CTL_38 (Address 0x26)



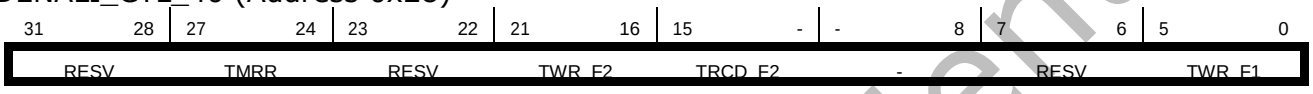
Name	Bits	Default	Range	Description
RESERVED	26:24	0x0	0x0-0x7	Reserved for future use. Refer to the regconfig files for the default
RESERVED	18:16	0x0	0x0-0x7	Reserved for future use. Refer to the regconfig files for the default
TPPD	10:8	0x4	0x0-0x7	DRAM TPPD value in cycles.
TCKESR_F2	7:0	0x00	0x0-0xff	Minimum CKE low pulse width during a self-refresh for frequency

DENALI_CTL_39 (Address 0x27)



Name	Bits	Default	Range	Description
TRCD_F1	31:24	0x00	0x0-0xff	DRAM TRCD value for frequency
TWR_F0	21:16	0x00	0x0-0x3f	DRAM TWR value for frequency
TRCD_F0	15:8	0x00	0x0-0xff	DRAM TRCD value for frequency
WRITEINTERP	0	0x0	0x0-0x1	Allow controller to interrupt a write burst to the DRAMs with a read

DENALI_CTL_40 (Address 0x28)

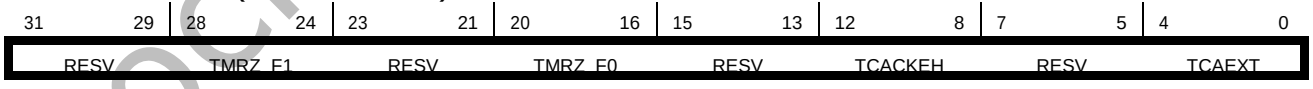


Name	Bits	Default	Range	Description
TMRR	27:24	0x0	0x0-0xf	DRAM TMRR value in cycles.
TWR_F2	21:16	0x00	0x0-0x3f	DRAM TWR value for frequency
TRCD_F2	15:8	0x00	0x0-0xff	DRAM TRCD value for frequency
TWR_F1	5:0	0x00	0x0-0x3f	DRAM TWR value for frequency

DENALI_CTL_41 (Address 0x29)

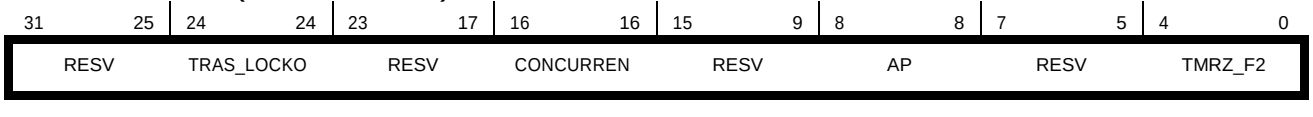
Name	Bits	Default	Range	Description
TCAMRD	29:24	0x00	0x0-0x3f	DRAM TCAMRD value in cycles.
TCAENT	17:8	0x000	0x0-0x3ff	DRAM TCAENT value in cycles.
TCACKEL	4:0	0x00	0x0-0x1f	DRAM TCACKEL value in cycles.

DENALI_CTL_42 (Address 0x2a)



Name	Bits	Default	Range	Description
TMRZ_F1	28:24	0x00	0x0-0x1f	DRAM TMRZ value for frequency
TMRZ_F0	20:16	0x00	0x0-0x1f	DRAM TMRZ value for frequency
TCACKEH	12:8	0x00	0x0-0x1f	DRAM TCACKEH value in cycles.
TCAEXT	4:0	0x00	0x0-0x1f	DRAM TCAEXT value in cycles.

DENALI_CTL_43 (Address 0x2b)



Name	Bits	Default	Range	Description
TRAS_LOCKOUT	24	0x0	0x0-0x1	IF the DRAM supports it, this allows the controller to execute auto pre-charge commands before the
CONCURRENTAP	16	0x0	0x0-0x1	IF the DRAM supports it, this allows the controller to issue commands to
AP	8	0x0	0x0-0x1	Enable auto pre-charge mode of
TMRZ_F2	4:0	0x00	0x0-0x1f	DRAM TMRZ value for frequency

DENALI_CTL_44 (Address 0x2c)

31 29	28 24	23 -	- 16	15 -	- 8	7 -	- 0
RESV	BSTLEN	TDAL_F2	-	TDAL_F1	-	TDAL_F0	-

Name	Bits	Default	Range	Description
BSTLEN	28:24	0x02	0x0-0x1f	Encoded burst length sent to DRAMs during initialization.
TDAL_F2	23:16	0x00	0x0-0xff	DRAM TDAL value for frequency
TDAL_F1	15:8	0x00	0x0-0xff	DRAM TDAL value for frequency
TDAL_F0	7:0	0x00	0x0-0xff	DRAM TDAL value for frequency

DENALI_CTL_45 (Address 0x2d)

31 25	24 24	23 -	- 16	15 -	- 8	7 -	- 0
RESV	REG_DIMM_E	TRP_AB_F2	-	TRP_AB_F1	-	TRP_AB_F0	-

Name	Bits	Default	Range	Description
REG_DIMM_ENABLE	24	0x0	0x0-0x1	Enable registered DIMM operation
TRP_AB_F2	23:16	0x00	0x0-0xff	DRAM TRP all bank value for
TRP_AB_F1	15:8	0x00	0x0-0xff	DRAM TRP all bank value for
TRP_AB_F0	7:0	0x00	0x0-0xff	DRAM TRP all bank value for

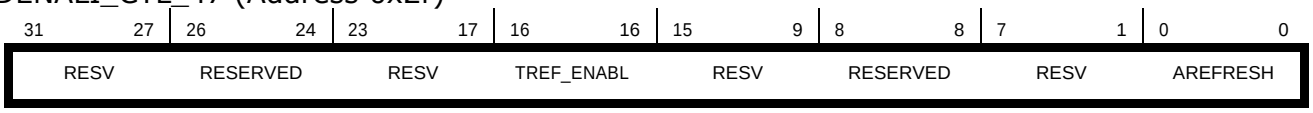
DENALI_CTL_46 (Address 0x2e)

31 25	24 24	23 17	16 16	15 9	8 8	7 2	1 0
RESV	NO_MEMORY	RESV	RESERVED	RESV	RESERVED	RESV	ADDRESS_MI

Name	Bits	Default	Range	Description
NO_MEMORY_DM	24	0x0	0x0-0x1	Indicates that the external DRAM does not support DM masking. Set
RESERVED	16	0x0	0x0-0x1	Reserved for future use. Refer to the regconfig files for the default
RESERVED	8	0x0	0x0-0x1	Reserved for future use. Refer to the regconfig files for the default

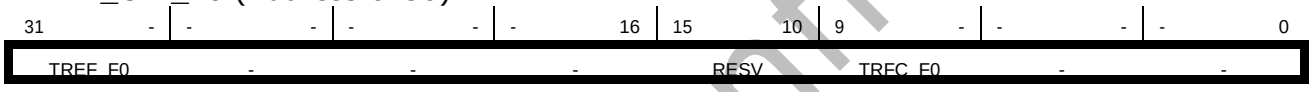
ADDRESS_MIRRORING	1:0	0x0	0x0-0x3	Indicates which chip selects support address mirroring. Bit (0)

DENALI_CTL_47 (Address 0x2f)



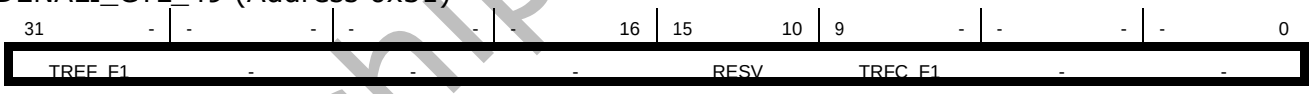
Name	Bits	Default	Range	Description
RESERVED	26:24	0x0	0x0-0x7	Reserved for future use. Refer to the regconfig files for the default
TREF_ENABLE	16	0x0	0x0-0x1	Issue auto-refresh commands to the DRAMs at the interval defined
RESERVED	8	0x0	0x0-0x1	Reserved for future use. Refer to the regconfig files for the default
AREFRESH	0	0x0	0x0-0x1	Initiate auto-refresh at the end of the current burst boundary. Set to 1

DENALI_CTL_48 (Address 0x30)



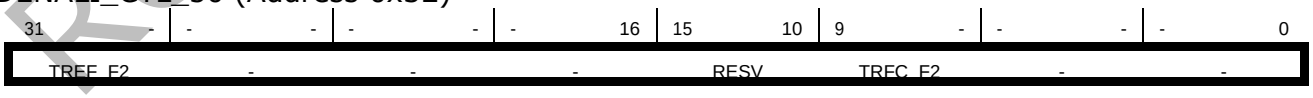
Name	Bits	Default	Range	Description
TREF_F0	31:16	0x0000	0x0-0xffff	DRAM TREF value for frequency
TRFC_F0	9:0	0x000	0x0-0x3ff	DRAM TRFC value for frequency

DENALI_CTL_49 (Address 0x31)



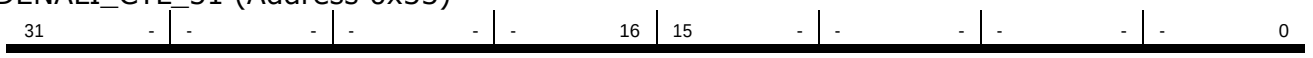
Name	Bits	Default	Range	Description
TREF_F1	31:16	0x0000	0x0-0xffff	DRAM TREF value for frequency
TRFC_F1	9:0	0x000	0x0-0x3ff	DRAM TRFC value for frequency

DENALI_CTL_50 (Address 0x32)



Name	Bits	Default	Range	Description
TREF_F2	31:16	0x0000	0x0-0xffff	DRAM TREF value for frequency
TRFC_F2	9:0	0x000	0x0-0x3ff	DRAM TRFC value for frequency

DENALI_CTL_51 (Address 0x33)



OBSOLETE	-	-	-	TREF_INTERV	-	-	-

Name	Bits	Default	Range	Description
TREF_INTERVAL	15:0	0x0000	0x0-0xffff	Defines the cycles between

DENALI_CTL_52 (Address 0x34)

31	-	-	-	-	-	16	15	-	-	-	-	-	0
TPDEX_F1							TPDEX_F0						

Name	Bits	Default	Range	Description
TPDEX_F1	31:16	0x0000	0x0-0xffff	DRAM TPDEX value for frequency
TPDEX_F0	15:0	0x0000	0x0-0xffff	DRAM TPDEX value for frequency

DENALI_CTL_53 (Address 0x35)

31	-	-	-	-	-	16	15	-	-	-	-	-	0
TXPDLL_F0							TPDEX_F2						

Name	Bits	Default	Range	Description
TXPDLL_F0	31:16	0x0000	0x0-0xffff	DRAM TXPDLL value for
TPDEX_F2	15:0	0x0000	0x0-0xffff	DRAM TPDEX value for frequency

DENALI_CTL_54 (Address 0x36)

31	-	-	-	-	-	16	15	-	-	-	-	-	0
TXPDLL_F2							TXPDLL_F1						

Name	Bits	Default	Range	Description
TXPDLL_F2	31:16	0x0000	0x0-0xffff	DRAM TXPDLL value for
TXPDLL_F1	15:0	0x0000	0x0-0xffff	DRAM TXPDLL value for

DENALI_CTL_55 (Address 0x37)

31	28	27	24	23	-	-	16	15	-	-	8	7	-	-	0
RESV		TCSCKE_F0		TMRRI_F2		-		TMRRI_F1		-		TMRRI_F0		-	

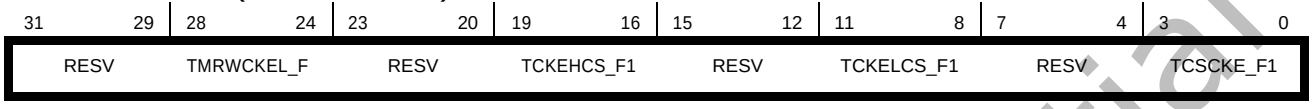
Name	Bits	Default	Range	Description
TCSCKE_F0	27:24	0x0	0x0-0xf	DRAM TCSCKE value for
TMRRI_F2	23:16	0x00	0x0-0xff	DRAM TMRRI value for frequency
TMRRI_F1	15:8	0x00	0x0-0xff	DRAM TMRRI value for frequency
TMRRI_F0	7:0	0x00	0x0-0xff	DRAM TMRRI value for frequency

DENALI_CTL_56 (Address 0x38)

31	28	27	24	23	21	20	16	15	12	11	8	7	4	3	0
RESV		TZQCKE_F0		RESV		TMRWCKEL_F		RESV		TCKEHCS_F0		RESV		TCKELCS_F0	

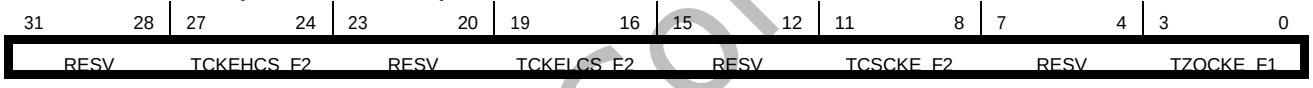
Name	Bits	Default	Range	Description
TZQCKE_F0	27:24	0x0	0x0-0xf	DRAM TZQCKE value for
TMRWCKEL_F0	20:16	0x00	0x0-0x1f	DRAM TMRWCKEL value for
TCKEHCS_F0	11:8	0x0	0x0-0xf	DRAM TCKEHCS value for
TCKELCS_F0	3:0	0x0	0x0-0xf	DRAM TCKELCS value for

DENALI_CTL_57 (Address 0x39)



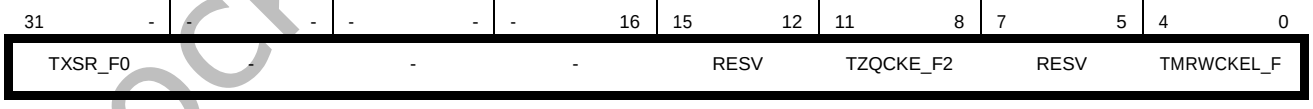
Name	Bits	Default	Range	Description
TMRWCKEL_F1	28:24	0x00	0x0-0x1f	DRAM TMRWCKEL value for
TCKEHCS_F1	19:16	0x0	0x0-0xf	DRAM TCKEHCS value for
TCKELCS_F1	11:8	0x0	0x0-0xf	DRAM TCKELCS value for
TCSCKE_F1	3:0	0x0	0x0-0xf	DRAM TCSCKE value for

DENALI_CTL_58 (Address 0x3a)



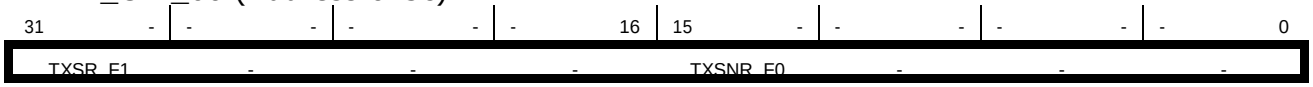
Name	Bits	Default	Range	Description
TCKEHCS_F2	27:24	0x0	0x0-0xf	DRAM TCKEHCS value for
TCKELCS_F2	19:16	0x0	0x0-0xf	DRAM TCKELCS value for
TCSCKE_F2	11:8	0x0	0x0-0xf	DRAM TCSCKE value for
TZQCKE_F1	3:0	0x0	0x0-0xf	DRAM TZQCKE value for

DENALI_CTL_59 (Address 0x3b)



Name	Bits	Default	Range	Description
TXSR_F0	31:16	0x0000	0x0-0xffff	DRAM TXSR value for frequency
TZQCKE_F2	11:8	0x0	0x0-0xf	DRAM TZQCKE value for
TMRWCKEL_F2	4:0	0x00	0x0-0x1f	DRAM TMRWCKEL value for

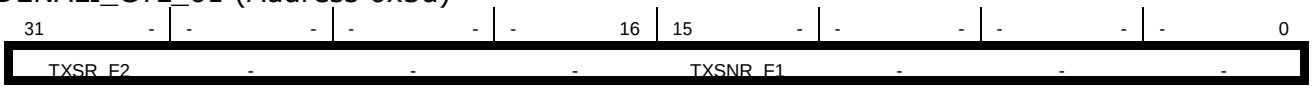
DENALI_CTL_60 (Address 0x3c)



Name	Bits	Default	Range	Description

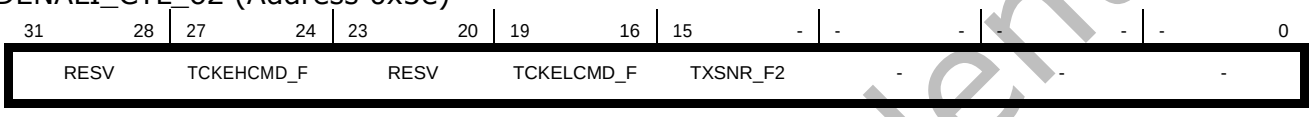
TXSR_F1	31:16	0x0000	0x0-0xffff	DRAM TXSR value for frequency
TXSNR_F0	15:0	0x0000	0x0-0xffff	DRAM TXSNR value for frequency

DENALI_CTL_61 (Address 0x3d)



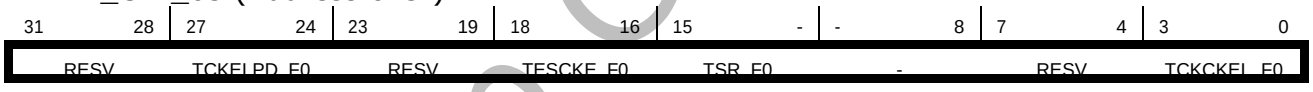
Name	Bits	Default	Range	Description
TXSR_F2	31:16	0x0000	0x0-0xffff	DRAM TXSR value for frequency
TXSNR_F1	15:0	0x0000	0x0-0xffff	DRAM TXSNR value for frequency

DENALI_CTL_62 (Address 0x3e)



Name	Bits	Default	Range	Description
TCKEHCMD_F0	27:24	0x0	0x0-0xf	DRAM TCKEHCMD value for
TCKELCMD_F0	19:16	0x0	0x0-0xf	DRAM TCKELCMD value for
TXSNR_F2	15:0	0x0000	0x0-0xffff	DRAM TXSNR value for frequency

DENALI_CTL_63 (Address 0x3f)

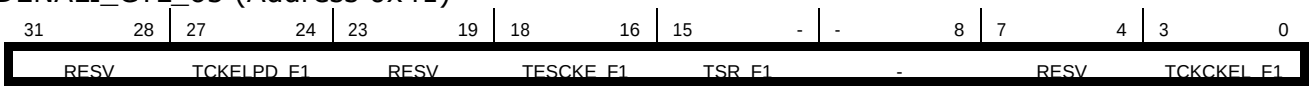


Name	Bits	Default	Range	Description
TCKELPD_F0	27:24	0x0	0x0-0xf	DRAM TCKELPD value for
TESCKE_F0	18:16	0x0	0x0-0x7	DRAM TESCKE value for
TSR_F0	15:8	0x00	0x0-0xff	DRAM TSR value for frequency
TCKCKEL_F0	3:0	0x0	0x0-0xf	DRAM TCKCKEL value for

DENALI_CTL_64 (Address 0x40)

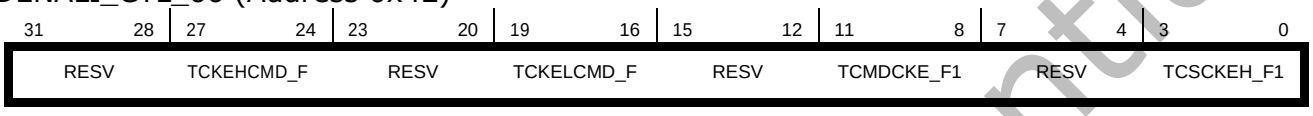
Name	Bits	Default	Range	Description
TCKEHCMD_F1	27:24	0x0	0x0-0xf	DRAM TCKEHCMD value for
TCKELCMD_F1	19:16	0x0	0x0-0xf	DRAM TCKELCMD value for
TCMDCKE_F0	11:8	0x0	0x0-0xf	DRAM TCMDCKE value for
TCSCKEH_F0	3:0	0x0	0x0-0xf	DRAM TCSCKEH value for

DENALI_CTL_65 (Address 0x41)



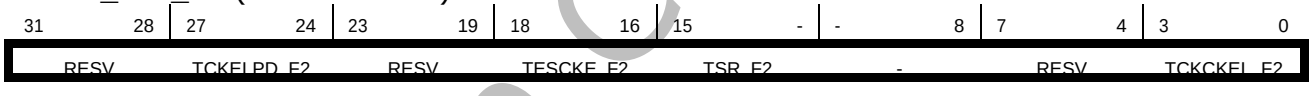
Name	Bits	Default	Range	Description
TCKELPD_F1	27:24	0x0	0x0-0xf	DRAM TCKELPD value for
TESCKE_F1	18:16	0x0	0x0-0x7	DRAM TESCKE value for
TSR_F1	15:8	0x00	0x0-0xff	DRAM TSR value for frequency
TCKCKEL_F1	3:0	0x0	0x0-0xf	DRAM TCKCKEL value for

DENALI_CTL_66 (Address 0x42)



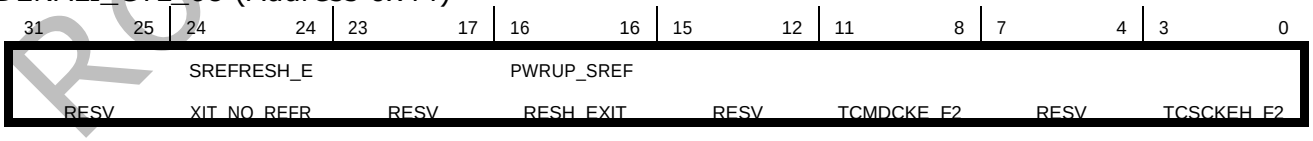
Name	Bits	Default	Range	Description
TCKEHCMD_F2	27:24	0x0	0x0-0xf	DRAM TCKEHCMD value for
TCKELCMD_F2	19:16	0x0	0x0-0xf	DRAM TCKELCMD value for
TCMDCKE_F1	11:8	0x0	0x0-0xf	DRAM TCMDCKE value for
TCSCKEH_F1	3:0	0x0	0x0-0xf	DRAM TCSCKEH value for

DENALI_CTL_67 (Address 0x43)



Name	Bits	Default	Range	Description
TCKELPD_F2	27:24	0x0	0x0-0xf	DRAM TCKELPD value for
TESCKE_F2	18:16	0x0	0x0-0x7	DRAM TESCKE value for
TSR_F2	15:8	0x00	0x0-0xff	DRAM TSR value for frequency
TCKCKEL_F2	3:0	0x0	0x0-0xf	DRAM TCKCKEL value for

DENALI_CTL_68 (Address 0x44)



Name	Bits	Default	Range	Description
SREFRESH_EXIT_NO_REFRESH	24	0x0	0x0-0x1	Disables the automatic refresh request associated with self-refresh
PWRUP_SREFRESH_EXIT	16	0x0	0x0-0x1	Allow powerup via self-refresh instead of full memoryinitialization.
TCMDCKE_F2	11:8	0x0	0x0-0xf	DRAM TCMDCKE value for
TCSCKEH_F2	3:0	0x0	0x0-0xf	DRAM TCSCKEH value for

DENALI_CTL_69 (Address 0x45)

31 26	25 24	23 -	- 16	15 11	10 8	7 1	0 0
RESV	DFS_STATUS	RESERVED	-	RESV	CKE_DELAY	RESV	ENABLE_QUICK_SREFRES

Name	Bits	Default	Range	Description
DFS_STATUS	25:24	0x0	0x0-0x3	Holds the error associated with the DFS interrupt. Bit (0) set indicates an illegal command and bit (1) set
RESERVED	23:16	0x00	0x0-0xff	Reserved for future use. Refer to the regconfig files for the default
CKE_DELAY	10:8	0x0	0x0-0x7	Additional cycles to delay CKE for
ENABLE_QUICK_SREFRESH	0	0x0	0x0-0x1	Allow user to interrupt memory initialization to enter self-refresh

DENALI_CTL_70 (Address 0x46)

31 25	24 24	23 17	16 16	15 9	8 8	7 1	0 0
RESV	DFS_RDLVL_E	RESV	DFS_WRLVL_	RESV	DFS_CALVL_E	RESV	DFS_ZQ_EN

Name	Bits	Default	Range	Description
DFS_RDLVL_EN	24	0x0	0x0-0x1	Enables read data eye training during a DFS exit. Set to 1 to
DFS_WRLVL_EN	16	0x0	0x0-0x1	Enables write leveling during a
DFS_CALVL_EN	8	0x0	0x0-0x1	Enables CA training during a DFS
DFS_ZQ_EN	0	0x0	0x0-0x1	Enables ZQ calibration during a

DENALI_CTL_71 (Address 0x47)

31 -	- 24	23 -	- -	- -	- 8	7 1	0 0
OBSOLETE	-	DFS_PROMOTE_THRESHOL	-	-	-	RESV	DFS_RDLVL_GATE_EN

Name	Bits	Default	Range	Description
DFS_PROMOTE_THRESHOLD_F0	23:8	0x0000	0x0-0xffff	DFS promotion number of long counts until the high priority request is asserted for frequency copy 0.
DFS_RDLVL_GATE_EN	0	0x0	0x0-0x1	Enables read gate training during a

DENALI_CTL_72 (Address 0x48)

31 -	- -	- -	- 16	15 -	- -	- -	- 0
DFS_PROMOTE_THRESHOL	-	-	-	DFS_PROMOTE_THRESHOL	-	-	-

Name	Bits	Default	Range	Description

DFS_PROMOTE_THRESHOLD_F2	31:16	0x0000	0x0-0xffff	DFS promotion number of long counts until the high priority request is asserted for frequency copy 2.
DFS_PROMOTE_THRESHOLD_F1	15:0	0x0000	0x0-0xffff	DFS promotion number of long counts until the high priority request is asserted for frequency copy 1.

DENALI_CTL_73 (Address 0x49)

31 27	26 24	23 18	17 16	15 10	9 8	7 2	1 0
RESV	RESERVED	RESV	ZQ_CALINIT_CS_CL_STATU	RESV	ZQ_CALLATCH_STATUS	RESV	ZQ_CALSTART_STATUS

Name	Bits	Default	Range	Description
RESERVED	26:24	0x0	0x0-0x7	Reserved for future use. Refer to the regconfig files for the default
ZQ_CALINIT_CS_CL_STATUS	17:16	0x0	0x0-0x3	Holds the status associated with the ZQ calibration interrupt. Bit (0) indicates that the ZQCS timer was exceeded and bit (1) indicates a
ZQ_CALLATCH_STATUS	9:8	0x0	0x0-0x3	Holds the status associated with the ZQ calibration interrupt. Bit (0) indicates that the ZQ cal latch timer was exceeded and bit (1) indicates
ZQ_CALSTART_STATUS	1:0	0x0	0x0-0x3	Holds the status associated with the ZQ calibration interrupt. Bit (0) indicates that the ZQ cal start timer was exceeded and bit (1) indicates

DENALI_CTL_74 (Address 0x4a)

31 -	- 24	23 -	- 16	15 -	- 8	7 3	2 0
RESERVED	-	RESERVED	-	RESERVED	-	RESV	RESERVED

Name	Bits	Default	Range	Description
RESERVED	31:24	0x00	0x0-0xff	Reserved for future use. Refer to the regconfig files for the default
RESERVED	23:16	0x00	0x0-0xff	Reserved for future use. Refer to the regconfig files for the default
RESERVED	15:8	0x00	0x0-0xff	Reserved for future use. Refer to the regconfig files for the default
RESERVED	2:0	0x0	0x0-0x7	Reserved for future use. Refer to the regconfig files for the default

DENALI_CTL_75 (Address 0x4b)

31 -	- -	- -	- 16	15 -	- -	- -	- 0
UPD_CTRLUPD_HIGH_THR	-	-	-	UPD_CTRLUPD_NORM_THR	-	-	-

Name	Bits	Default	Range	Description
UPD_CTRLUPD_HIGH_THRESHOLD_F0	31:16	0x0000	0x0-0xffff	DFI control update number of long counts until the high priority request
UPD_CTRLUPD_NORM_THRESHOLD_F0	15:0	0x0000	0x0-0xffff	DFI control update number of long counts until the normal priority

DENALI_CTL_76 (Address 0x4c)

31	-	-	-	-	-	16	15	-	-	-	-	-	0
UPD_CTRLUPD_SW_PROM	-	-	-				UPD_CTRLUPD_TIMEOUT_F	-	-	-			

Name	Bits	Default	Range	Description
UPD_CTRLUPD_SW_PROMOTE_THRESH	31:16	0x0000	0x0-0xffff	DFI control update SW promotion number of long counts until the high
UPD_CTRLUPD_TIMEOUT_F0	15:0	0x0000	0x0-0xffff	DFI control update number of long counts until the timeout is asserted

DENALI_CTL_77 (Address 0x4d)

31	-	-	-	-	-	16	15	-	-	-	-	-	0
UPD_CTRLUPD_NORM_THR	-	-	-				UPD_PHYUPD_DFI_PROMOTE_THRESHO	-	-	-			

Name	Bits	Default	Range	Description
UPD_CTRLUPD_NORM_THRESHOLD_F1	31:16	0x0000	0x0-0xffff	DFI control update number of long counts until the normal priority
UPD_PHYUPD_DFI_PROMOTE_THRESH	15:0	0x0000	0x0-0xffff	DFI PHY update DFI promotion number of long counts until the high

DENALI_CTL_78 (Address 0x4e)

31	-	-	-	-	-	16	15	-	-	-	-	-	0
UPD_CTRLUPD_TIMEOUT_F	-	-	-				UPD_CTRLUPD_HIGH_THR	-	-	-			

Name	Bits	Default	Range	Description
UPD_CTRLUPD_TIMEOUT_F1	31:16	0x0000	0x0-0xffff	DFI control update number of long counts until the timeout is asserted
UPD_CTRLUPD_HIGH_THRESHOLD_F1	15:0	0x0000	0x0-0xffff	DFI control update number of long counts until the high priority request

DENALI_CTL_79 (Address 0x4f)

31	-	-	-	-	-	16	15	-	-	-	-	-	0
UPD_PHYUPD_DFI_PROMOTE_THRESHO	-	-	-				UPD_CTRLUPD_SW_PROM	-	-	-			

Name	Bits	Default	Range	Description
UPD_PHYUPD_DFI_PROMOTE_THRESH	31:16	0x0000	0x0-0xffff	DFI PHY update DFI promotion number of long counts until the high
UPD_CTRLUPD_SW_PROMOTE_THRESH	15:0	0x0000	0x0-0xffff	DFI control update SW promotion number of long counts until the high

DENALI_CTL_80 (Address 0x50)

31 - - - - - - - - - - - - - - - 16	15 - - - - - - - - - - - - - - - 0
UPD_CTRLUPD_HIGH_THR - - -	UPD_CTRLUPD_NORM_THR - - -

Name	Bits	Default	Range	Description
UPD_CTRLUPD_HIGH_THRESHOLD_F2	31:16	0x0000	0x0-0xffff	DFI control update number of long counts until the high priority request
UPD_CTRLUPD_NORM_THRESHOLD_F2	15:0	0x0000	0x0-0xffff	DFI control update number of long counts until the normal priority

DENALI_CTL_81 (Address 0x51)

31 - - - - - - - - - - - - - - - 16	15 - - - - - - - - - - - - - - - 0
UPD_CTRLUPD_SW_PROM - - -	UPD_CTRLUPD_TIMEOUT_F - - -

Name	Bits	Default	Range	Description
UPD_CTRLUPD_SW_PROMOTE_THRESH	31:16	0x0000	0x0-0xffff	DFI control update SW promotion number of long counts until the high
UPD_CTRLUPD_TIMEOUT_F2	15:0	0x0000	0x0-0xffff	DFI control update number of long counts until the timeout is asserted

DENALI_CTL_82 (Address 0x52)

31 - - - - - - - - - - - - - - - 16	15 - - - - - - - - - - - - - - - 0
TDFI_PHYMST - - -	UPD_PHYUPD_DFI_PROMOTE_THRESHO - - -

Name	Bits	Default	Range	Description
TDFI_PHYMSTR_MAX_F0	31:16	0x0000	0x0-0xffff	Defines the DFI tPHYMSTR_MAX timing parameter (in DFI clocks), the maximum cycles that dfi_phymstr_req following the assertion of dfi_phymstr_ack can be asserted, for frequency copy 0.
UPD_PHYUPD_DFI_PROMOTE_THRESH	15:0	0x0000	0x0-0xffff	DFI PHY update DFI promotion number of long counts until the high

DENALI_CTL_83 (Address 0x53)

31 - - - - - - 16	15 - - - - - - 0
PHYMSTR_DF I_PROMOTE_ - - -	TDFI_PHYMST - - -

Name	Bits	Default	Range	Description
PHYMSTR_DFI_PROMOTE_THRESHOLD_	31:16	0x0000	0x0-0xffff	DFI PHY master request promotion number of long counts until the high
TDFI_PHYMSTR_RESP_F0	15:0	0x0000	0x0-0xffff	Defines the DFI tPHYMSTR_RESP timing parameter (in DFI clocks), the maximum cycles between a dfi_phymstr_req assertion and a dfi_phymstr_ack assertion, for

DENALI_CTL_84 (Address 0x54)

31 - - - - - - 16	15 - - - - - - 0
TDFI_PHYMST - - -	TDFI_PHYMST - - -

Name	Bits	Default	Range	Description
TDFI_PHYMSTR_RESP_F1	31:16	0x0000	0x0-0xffff	Defines the DFI tPHYMSTR_RESP timing parameter (in DFI clocks), the maximum cycles between a dfi_phymstr_req assertion and a dfi_phymstr_ack assertion, for
TDFI_PHYMSTR_MAX_F1	15:0	0x0000	0x0-0xffff	Defines the DFI tPHYMSTR_MAX timing parameter (in DFI clocks), the maximum cycles that dfi_phymstr_req following the assertion of dfi_phymstr_ack can be asserted, for frequency copy 1.

DENALI_CTL_85 (Address 0x55)

31 - - - - - - 16	15 - - - - - - 0
TDFI_PHYMST - - -	PHYMSTR_DF I_PROMOTE_ - - -

Name	Bits	Default	Range	Description
TDFI_PHYMSTR_MAX_F2	31:16	0x0000	0x0-0xffff	Defines the DFI tPHYMSTR_MAX timing parameter (in DFI clocks), the maximum cycles that dfi_phymstr_req following the assertion of dfi_phymstr_ack can be asserted, for frequency copy 2.

PHYMSTR_DFI_PROMOTE_THRESHOLD_	15:0	0x0000	0x0-0xffff	DFI PHY master request promotion number of long counts until the high

DENALI_CTL_86 (Address 0x56)

31 -	-	-	-	-	-	16	15 -	-	-	-	-	0
PHYMSTR_DFI_PROMOTE_	-	-	-				TDFI_PHYMST	-	-	-		

Name	Bits	Default	Range	Description
PHYMSTR_DFI_PROMOTE_THRESHOLD_	31:16	0x0000	0x0-0xffff	DFI PHY master request promotion number of long counts until the high
TDFI_PHYMSTR_RESP_F2	15:0	0x0000	0x0-0xffff	Defines the DFI tPHYMSTR_RESP timing parameter (in DFI clocks), the maximum cycles between a dfi_phymstr_req assertion and a dfi_phymstr_ack assertion, for

DENALI_CTL_87 (Address 0x57)

31 -	-	-	-	-	-	16	15	10	9	8	7	1	0	0
MRR_TEMPCHK_NORM_TH	-	-	-				RESV		PHYMSTR_ERROR_STATUS		RESV			PHYMSTR_NO_AREF

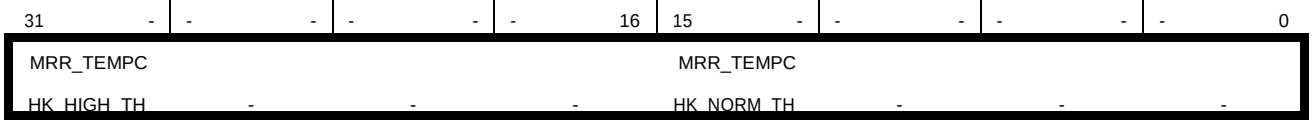
Name	Bits	Default	Range	Description
MRR_TEMPCHK_NORM_THRESHOLD_F0	31:16	0x0000	0x0-0xffff	MRR temp check number of long counts until the normal priority
PHYMSTR_ERROR_STATUS	9:8	0x0	0x0-0x3	Identifies the source of any DFI PHY Master Interface errors. Value of 1 indicates a timing violation of
PHYMSTR_NO_AREF	0	0x0	0x0-0x1	Disables refreshes during the PHY master interface sequence. Set to 1 to disable. Refreshes during reset are only supported for DFI 4.0 and

DENALI_CTL_88 (Address 0x58)

31 -	-	-	-	-	-	16	15 -	-	-	-	-	0
MRR_TEMPCHK_TIMEOUT	-	-	-				MRR_TEMPCHK_HIGH_TH	-	-	-		

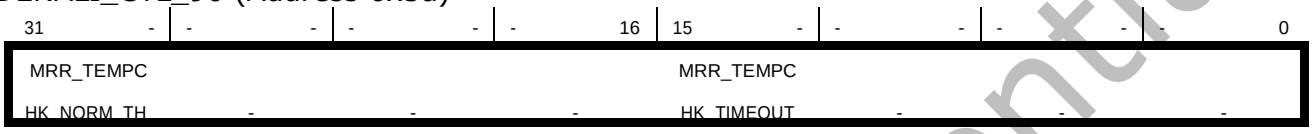
Name	Bits	Default	Range	Description
MRR_TEMPCHK_TIMEOUT_F0	31:16	0x0000	0x0-0xffff	MRR temp check number of long counts until the timeout is asserted
MRR_TEMPCHK_HIGH_THRESHOLD_F0	15:0	0x0000	0x0-0xffff	MRR temp check number of long counts until the high priority request

DENALI_CTL_89 (Address 0x59)



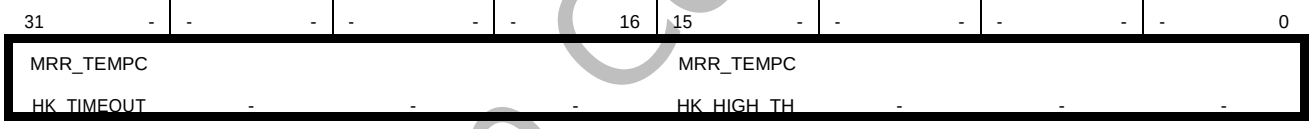
Name	Bits	Default	Range	Description
MRR_TEMPCHK_HIGH_THRESHOLD_F1	31:16	0x0000	0x0-0xffff	MRR temp check number of long counts until the high priority request
MRR_TEMPCHK_NORM_THRESHOLD_F1	15:0	0x0000	0x0-0xffff	MRR temp check number of long counts until the normal priority

DENALI_CTL_90 (Address 0x5a)



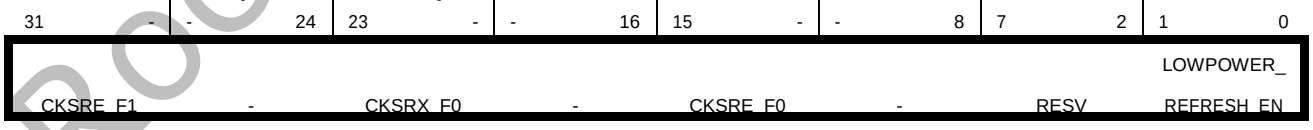
Name	Bits	Default	Range	Description
MRR_TEMPCHK_NORM_THRESHOLD_F2	31:16	0x0000	0x0-0xffff	MRR temp check number of long counts until the normal priority
MRR_TEMPCHK_TIMEOUT_F1	15:0	0x0000	0x0-0xffff	MRR temp check number of long counts until the timeout is asserted

DENALI_CTL_91 (Address 0x5b)



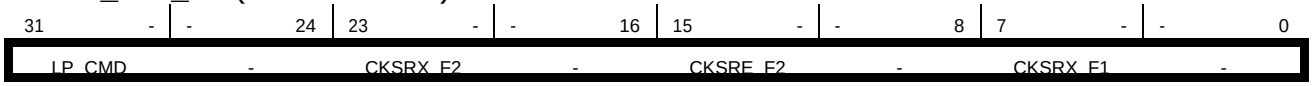
Name	Bits	Default	Range	Description
MRR_TEMPCHK_TIMEOUT_F2	31:16	0x0000	0x0-0xffff	MRR temp check number of long counts until the timeout is asserted
MRR_TEMPCHK_HIGH_THRESHOLD_F2	15:0	0x0000	0x0-0xffff	MRR temp check number of long counts until the high priority request

DENALI_CTL_92 (Address 0x5c)



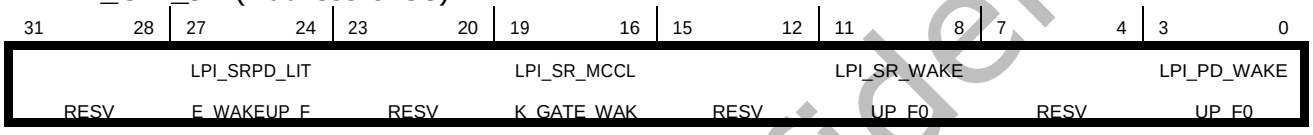
Name	Bits	Default	Range	Description
CKSRE_F1	31:24	0x00	0x0-0xff	Clock hold delay on self-refresh
CKSRX_F0	23:16	0x00	0x0-0xff	Clock stable delay on self-refresh
CKSRE_F0	15:8	0x00	0x0-0xff	Clock hold delay on self-refresh
LOWPOWER_REFRESH_ENABLE	1:0	0x0	0x0-0x3	Enable refreshes while in low power mode. Bit (0) controls cs0,

DENALI_CTL_93 (Address 0x5d)



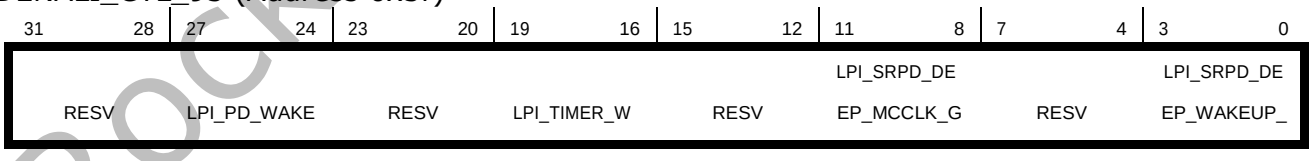
Name	Bits	Default	Range	Description
LP_CMD	31:24	0x00	0x0-0xff	Low power software command request interface. Bit (0) controls exit, bit (1) controls entry, bits (4:2) define the low power state, bit (5)
CKSRX_F2	23:16	0x00	0x0-0xff	Clock stable delay on self-refresh
CKSRE_F2	15:8	0x00	0x0-0xff	Clock hold delay on self-refresh
CKSRX_F1	7:0	0x00	0x0-0xff	Clock stable delay on self-refresh

DENALI_CTL_94 (Address 0x5e)



Name	Bits	Default	Range	Description
LPI_SRPD_LITE_WAKEUP_F0	27:24	0x0	0x0-0xf	Defines the DFI tLP_WAKEUP timing parameter (in DFI clocks) to be driven when memory is in self-
LPI_SR_MCCLK_GATE_WAKEUP_F0	19:16	0x0	0x0-0xf	Defines the DFI tLP_WAKEUP timing parameter (in DFI clocks) to be driven when memory is in self-
LPI_SR_WAKEUP_F0	11:8	0x0	0x0-0xf	Defines the DFI tLP_WAKEUP timing parameter (in DFI clocks) to
LPI_PD_WAKEUP_F0	3:0	0x0	0x0-0xf	Defines the DFI tLP_WAKEUP timing parameter (in DFI clocks) to

DENALI_CTL_95 (Address 0x5f)



Name	Bits	Default	Range	Description
LPI_PD_WAKEUP_F1	27:24	0x0	0x0-0xf	Defines the DFI tLP_WAKEUP timing parameter (in DFI clocks) to
LPI_TIMER_WAKEUP_F0	19:16	0x0	0x0-0xf	Defines the DFI tLP_WAKEUP timing parameter (in DFI clocks) to
LPI_SRPD_DEEP_MCCLK_GATE_WAKEU	11:8	0x0	0x0-0xf	Defines the DFI tLP_WAKEUP timing parameter (in DFI clocks) to be driven when memory is in self-

LPI_SRPD_DEEP_WAKEUP_F0	3:0	0x0	0x0-0xf	Defines the DFI tLP_WAKEUP timing parameter (in DFI clocks) to be driven when memory is in self-

DENALI_CTL_96 (Address 0x60)

31 28	27 24	23 20	19 16	15 12	11 8	7 4	3 0
RESV	LPI_SRPD_DEEP_WAKEUP_F1	RESV	LPI_SRPD_LITE_WAKEUP_F	RESV	LPI_SR_MCCLK_GATE_WAKEUP_F1	RESV	LPI_SR_WAKEUP_F1

Name	Bits	Default	Range	Description
LPI_SRPD_DEEP_WAKEUP_F1	27:24	0x0	0x0-0xf	Defines the DFI tLP_WAKEUP timing parameter (in DFI clocks) to be driven when memory is in self-
LPI_SRPD_LITE_WAKEUP_F1	19:16	0x0	0x0-0xf	Defines the DFI tLP_WAKEUP timing parameter (in DFI clocks) to be driven when memory is in self-
LPI_SR_MCCLK_GATE_WAKEUP_F1	11:8	0x0	0x0-0xf	Defines the DFI tLP_WAKEUP timing parameter (in DFI clocks) to be driven when memory is in self-
LPI_SR_WAKEUP_F1	3:0	0x0	0x0-0xf	Defines the DFI tLP_WAKEUP timing parameter (in DFI clocks) to

DENALI_CTL_97 (Address 0x61)

31 28	27 24	23 20	19 16	15 12	11 8	7 4	3 0
RESV	LPI_SR_WAKEUP_F2	RESV	LPI_PD_WAKEUP_F2	RESV	LPI_TIMER_WAKEUP_F1	RESV	LPI_SRPD_DEEP_MCCLK_GATE_WAKEU

Name	Bits	Default	Range	Description
LPI_SR_WAKEUP_F2	27:24	0x0	0x0-0xf	Defines the DFI tLP_WAKEUP timing parameter (in DFI clocks) to
LPI_PD_WAKEUP_F2	19:16	0x0	0x0-0xf	Defines the DFI tLP_WAKEUP timing parameter (in DFI clocks) to
LPI_TIMER_WAKEUP_F1	11:8	0x0	0x0-0xf	Defines the DFI tLP_WAKEUP timing parameter (in DFI clocks) to
LPI_SRPD_DEEP_MCCLK_GATE_WAKEU	3:0	0x0	0x0-0xf	Defines the DFI tLP_WAKEUP timing parameter (in DFI clocks) to be driven when memory is in self-

DENALI_CTL_98 (Address 0x62)

31 28	27 24	23 20	19 16	15 12	11 8	7 4	3 0
RESV	LPI_SRPD_DEEP_MCCLK_GATE_WAKEUP_F2	RESV	LPI_SRPD_DEEP_WAKEUP_F2	RESV	LPI_SRPD_LITE_WAKEUP_F2	RESV	LPI_SR_MCCLK_GATE_WAK

Name	Bits	Default	Range	Description

LPI_SRPD_DEEP_MCCLK_GATE_WAKEU	27:24	0x0	0x0-0xf	Defines the DFI tLP_WAKEUP timing parameter (in DFI clocks) to be driven when memory is in self-
LPI_SRPD_DEEP_WAKEUP_F2	19:16	0x0	0x0-0xf	Defines the DFI tLP_WAKEUP timing parameter (in DFI clocks) to be driven when memory is in self-
LPI_SRPD_LITE_WAKEUP_F2	11:8	0x0	0x0-0xf	Defines the DFI tLP_WAKEUP timing parameter (in DFI clocks) to be driven when memory is in self-
LPI_SR_MCCLK_GATE_WAKEUP_F2	3:0	0x0	0x0-0xf	Defines the DFI tLP_WAKEUP timing parameter (in DFI clocks) to be driven when memory is in self-

DENALI_CTL_99 (Address 0x63)

31 28	27 -	- -	- 16	15 13	12 8	7 4	3 0
RESV	LPI_TIMER_C	-	-	RESV	LPI_WAKEUP_	RESV	LPI_TIMER_W

Name	Bits	Default	Range	Description
LPI_TIMER_COUNT	27:16	0x000	0x0-0xfff	Defines the LPI timer count.
LPI_WAKEUP_EN	12:8	0x00	0x0-0x1f	Enables the various low power wakeup parameters. Bit (0) enables power-down wakeup, bit (1) enables self-refresh wakeup, bit (2) enables self-refresh with memory
LPI_TIMER_WAKEUP_F2	3:0	0x0	0x0-0xf	Defines the DFI tLP_WAKEUP timing parameter (in DFI clocks) to

DENALI_CTL_100 (Address 0x64)

31 31	30 24	23 19	18 16	15 12	11 -	- -	- 0
RESV	LP_STATE	RESV	TDFI_LP_RES	RESV	LPI_WAKEUP_	-	-

Name	Bits	Default	Range	Description
LP_STATE	30:24	0x20	0x0-0x7f	Low power state status parameter. Bits (4:0) indicate the current low power state and bit (5) set indicates
TDFI_LP_RESP	18:16	0x0	0x0-0x7	Defines the DFI tLP_RESP timing parameter (in DFI clocks), the maximum cycles between a
LPI_WAKEUP_TIMEOUT	11:0	0x000	0x0-0xfff	Defines the LPI timeout time, the maximum cycles between a dfi_lp_req de-assertion and a

DENALI_CTL_101 (Address 0x65)

31 -	- 24	23 19	18 16	15 12	11 8	7 4	3 0
OBSOLETE	-	RESV	LP_AUTO_ME	RESV	LP_AUTO_EXI	RESV	LP_AUTO_EN

Name	Bits	Default	Range	Description
LP_AUTO_MEM_GATE_EN	18:16	0x0	0x0-0x7	Enable memory clock gating when entering a low power state via the auto low power counters. Bit (0)
LP_AUTO_EXIT_EN	11:8	0x0	0x0-0xf	Enable auto exit from each of the low power states when a read or write command enters the command queue. Bit (0) controls
LP_AUTO_ENTRY_EN	3:0	0x0	0x0-0xf	Enable auto entry into each of the low power states when the associated idle timer expires. Bit (0) controls power-down, bit (1) controls self-refresh, bit (2) controls

DENALI_CTL_102 (Address 0x66)

31 28	27 - 16	15 12	11 - 0
RESV	LP_AUTO_SR - -	RESV	LP_AUTO_PD _IDLE - -

Name	Bits	Default	Range	Description
LP_AUTO_SRPD_LITE_IDLE	27:16	0x000	0x0-0xfff	Defines the idle time until the controller will place memory in self-
LP_AUTO_PD_IDLE	11:0	0x000	0x0-0xfff	Defines the idle time until the controller will place memory in

DENALI_CTL_103 (Address 0x67)

31 - 16	15 - 8	7 - 0
HW_PROMOT E_THRESHOL - - -	LP_AUTO_SR _MC_GATE_ID -	LP_AUTO_SR _IDLE -

Name	Bits	Default	Range	Description
HW_PROMOTE_THRESHOLD_F0	31:16	0x0000	0x0-0xffff	HW interface promotion number of long counts until the high priority
LP_AUTO_SR_MC_GATE_IDLE	15:8	0x00	0x0-0xff	Number of long count sequences until the controller will place memory in self-refresh with
LP_AUTO_SR_IDLE	7:0	0x00	0x0-0xff	Number of long count sequences until the controller will place

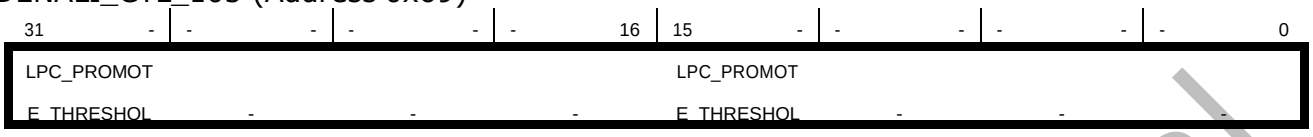
DENALI_CTL_104 (Address 0x68)

31 - 16	15 - 0
HW_PROMOT E_THRESHOL - - -	HW_PROMOT E_THRESHOL - - -

Name	Bits	Default	Range	Description

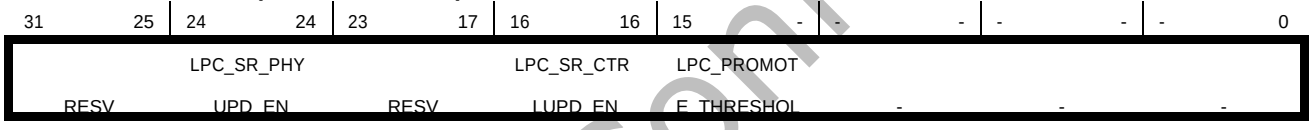
HW_PROMOTE_THRESHOLD_F2	31:16	0x0000	0x0-0xffff	HW interface promotion number of long counts until the high priority
HW_PROMOTE_THRESHOLD_F1	15:0	0x0000	0x0-0xffff	HW interface promotion number of long counts until the high priority

DENALI_CTL_105 (Address 0x69)



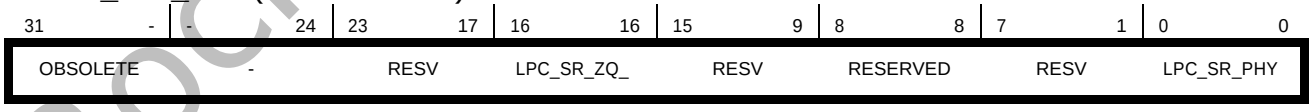
Name	Bits	Default	Range	Description
LPC_PROMOTE_THRESHOLD_F1	31:16	0x0000	0x0-0xffff	LPC promotion number of long counts until the high priority request is asserted for frequency copy 1.
LPC_PROMOTE_THRESHOLD_F0	15:0	0x0000	0x0-0xffff	LPC promotion number of long counts until the high priority request is asserted for frequency copy 0.

DENALI_CTL_106 (Address 0x6a)



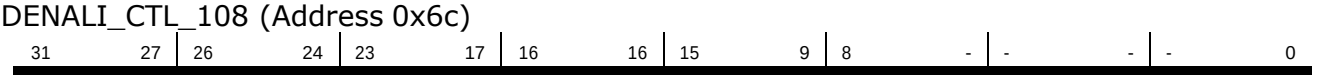
Name	Bits	Default	Range	Description
LPC_SR_PHYUPD_EN	24	0x0	0x0-0x1	Enable LPC to execute a DFI PHY update on a self-refresh exit
LPC_SR_CTRLUPD_EN	16	0x0	0x0-0x1	Enable LPC to execute a DFI control update on a self-refresh exit
LPC_PROMOTE_THRESHOLD_F2	15:0	0x0000	0x0-0xffff	LPC promotion number of long counts until the high priority request is asserted for frequency copy 2.

DENALI_CTL_107 (Address 0x6b)



Name	Bits	Default	Range	Description
LPC_SR_ZQ_EN	16	0x0	0x0-0x1	Enable LPC to execute a ZQ calibration on a self-refresh exit
RESERVED	8	0x0	0x0-0x1	Reserved for future use. Refer to the regconfig files for the default
LPC_SR_PHYMSTR_EN	0	0x0	0x0-0x1	Enable LPC to execute a DFI PHY Master request on a self-refresh

DENALI_CTL_108 (Address 0x6c)



RESV	DFS_DLL_OFF	RESV	DFS_ENABLE	RESV	RESERVED	-	-

Name	Bits	Default	Range	Description
DFS_DLL_OFF	26:24	0x0	0x0-0x7	Defines if the memory DLL must be off for the associated frequency set. Bit (0) corresponds to
DFS_ENABLE	16	0x0	0x0-0x1	Enable hardware dynamic frequency scaling. Set to 1 to
RESERVED	8:0	0x000	0x0-0x1ff	Reserved for future use. Refer to the regconfig files for the default

DENALI_CTL_109 (Address 0x6d)

31 - 24	23 - 8	7 - 0
TDFI_INIT_ST -	TDFI_INIT_CO - - -	TDFI_INIT_ST -

Name	Bits	Default	Range	Description
TDFI_INIT_START_F1	31:24	0x00	0x0-0xff	Defines the DFI tINIT_START timing parameter (in DFI clocks) for frequency copy 1, the maximum number of cycles between a
TDFI_INIT_COMPLETE_F0	23:8	0x0000	0x0-0xffff	Defines the DFI tINIT_COMPLETE timing parameter (in DFI clocks) for frequency copy 0, the maximum
TDFI_INIT_START_F0	7:0	0x00	0x0-0xff	Defines the DFI tINIT_START timing parameter (in DFI clocks) for frequency copy 0, the maximum number of cycles between a

DENALI_CTL_110 (Address 0x6e)

31 - 24	23 - 16	15 - 0
OBSOLETE -	TDFI_INIT_ST -	TDFI_INIT_CO - - -

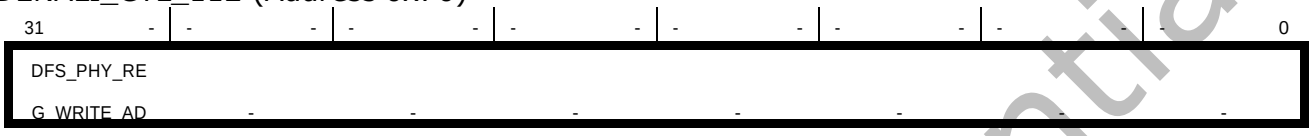
Name	Bits	Default	Range	Description
TDFI_INIT_START_F2	23:16	0x00	0x0-0xff	Defines the DFI tINIT_START timing parameter (in DFI clocks) for frequency copy 2, the maximum number of cycles between a
TDFI_INIT_COMPLETE_F1	15:0	0x0000	0x0-0xffff	Defines the DFI tINIT_COMPLETE timing parameter (in DFI clocks) for frequency copy 1, the maximum

DENALI_CTL_111 (Address 0x6f)

31 25	24 24	23 18	17 16	15 - 0
RESV	DFS_PHY_RE	RESV	CURRENT_RE	TDFI_INIT_CO - - -

Name	Bits	Default	Range	Description
DFS_PHY_REG_WRITE_EN	24	0x0	0x0-0x1	Enable a register write to the PHY during a frequency change. Set to
CURRENT_REG_COPY	17:16	0x0	0x0-0x3	Indicates the current copy of timing parameters that is in use by the
TDFI_INIT_COMPLETE_F2	15:0	0x0000	0x0-0xffff	Defines the DFI tINIT_COMPLETE timing parameter (in DFI clocks) for frequency copy 2, the maximum

DENALI_CTL_112 (Address 0x70)

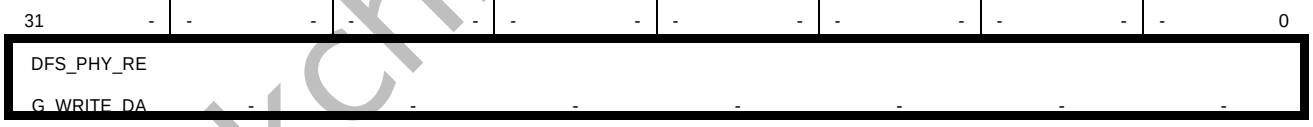


Name	Bits	Default	Range	Description
DFS_PHY_REG_WRITE_ADDR	31:0	0x00000000	0x0-0xffffffff	Register address which will be written during a frequency change.

DENALI_CTL_113 (Address 0x71)

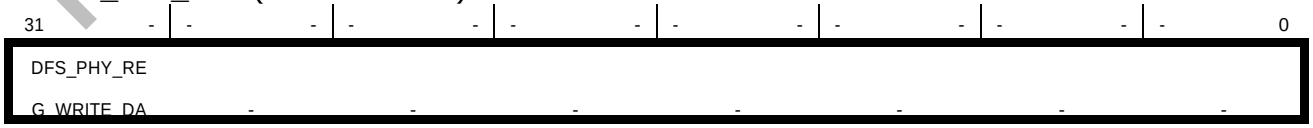
Name	Bits	Default	Range	Description
DFS_PHY_REG_WRITE_DATA_F0	31:0	0x00000000	0x0-0xffffffff	Register data which will be written during a frequency change for

DENALI_CTL_114 (Address 0x72)



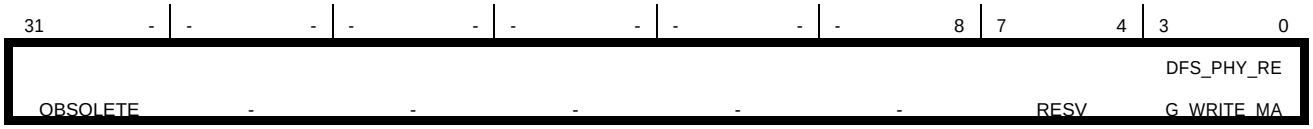
Name	Bits	Default	Range	Description
DFS_PHY_REG_WRITE_DATA_F1	31:0	0x00000000	0x0-0xffffffff	Register data which will be written during a frequency change for

DENALI_CTL_115 (Address 0x73)



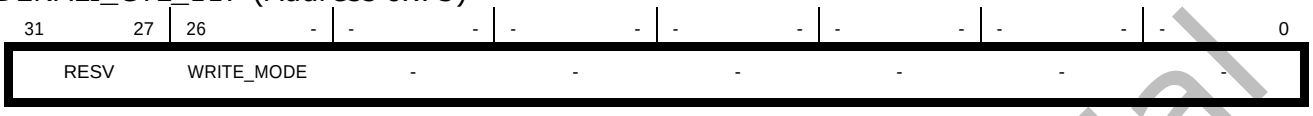
Name	Bits	Default	Range	Description
DFS_PHY_REG_WRITE_DATA_F2	31:0	0x00000000	0x0-0xffffffff	Register data which will be written during a frequency change for

DENALI_CTL_116 (Address 0x74)



Name	Bits	Default	Range	Description
DFS_PHY_REG_WRITE_MASK	3:0	0x0	0x0-0xf	Register mask which will be written

DENALI_CTL_117 (Address 0x75)

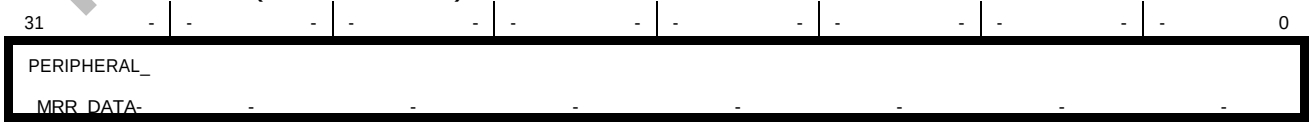


Name	Bits	Default	Range	Description
WRITE_MODEREG	26:0	0x0000000	0x0-0x7fffffff	Write memory mode register data to the DRAMs. Bits (7:0) define the memory mode register number if bit (23) is set, bits (15:8) define the chip select if bit (24) is clear, bits register/s to write, bit (24) defines whether all chip selects will be written, and bit (25) triggers the write.

DENALI_CTL_118 (Address 0x76)

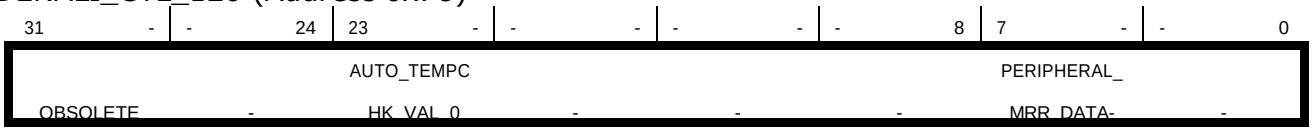
Name	Bits	Default	Range	Description
READ_MODEREG	24:8	0x00000	0x0-0x1ffff	Read the specified memory mode register from specified chip when start bit set. Bits (7:0) define the
MRW_STATUS	7:0	0x00	0x0-0xff	Write memory mode register status. Bit (0) set indicates a WRITE_MODEREG parameter programming error. Bit (1) set indicates a PASR error. Bit (2) is Reserved. Bit (3) set indicates a self refresh or deep power down error. Bit (4) set indicates that a

DENALI_CTL_119 (Address 0x77)



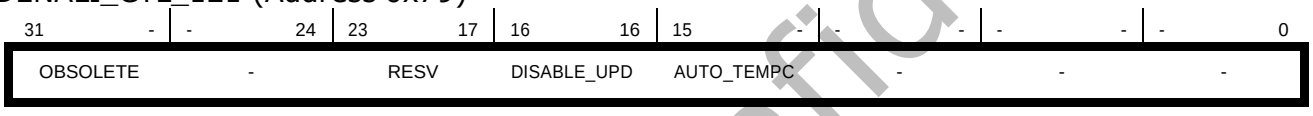
Name	Bits	Default	Range	Description
PERIPHERAL_MRR_DATA[31:0]	31:0	0x0000000	0x0-0xffffffff	Data and chip returned from memory mode register read requested by the READ_MODEREG parameter. Bits (15:8) indicate the chip. READ-ONLY

DENALI_CTL_120 (Address 0x78)



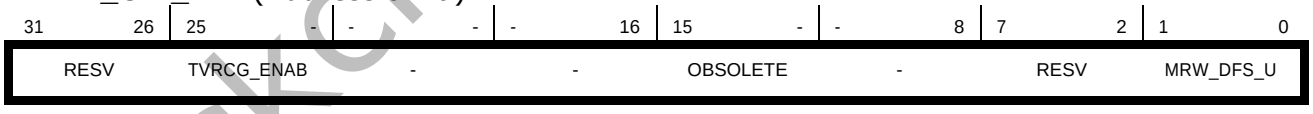
Name	Bits	Default	Range	Description
AUTO_TEMPCHK_VAL_0	23:8	0x0000	0x0-0xffff	MR4 data for all devices on chip 0 accessed by automatic MRR commands. Bits (3:0) correlate to the device on the lower byte, bits
PERIPHERAL_MRR_DATA [39:32]	7:0	0x00	0x0-0xff	Data and chip returned from memory mode register read requested by the READ_MODEREG parameter.Bits

DENALI_CTL_121 (Address 0x79)



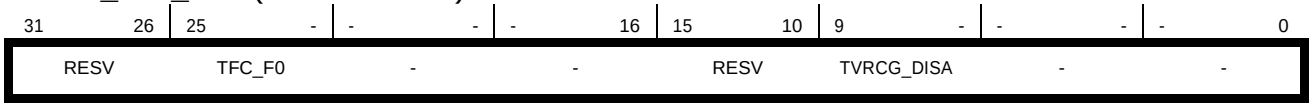
Name	Bits	Default	Range	Description
DISABLE_UPDATE_TVRCG	16	0x0	0x0-0x1	Bypass changing for TVRCG during a DFS operation. Set to 1to
AUTO_TEMPCHK_VAL_1	15:0	0x0000	0x0-0xffff	MR4 data for all devices on chip 1 accessed by automatic MRR commands. Bits (3:0) correlate to the device on the lower byte, bits

DENALI_CTL_122 (Address 0x7a)



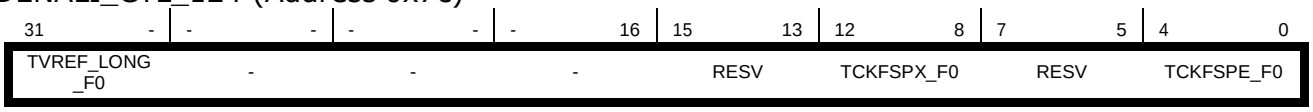
Name	Bits	Default	Range	Description
TVRCG_ENABLE_F0	25:16	0x000	0x0-0x3ff	JEDEC TVRCG_ENABLE time.
MRW_DFS_UPDATE_FRC	1:0	0x0	0x0-0x3	Defines the frequency register set to use when doing a software MRW

DENALI_CTL_123 (Address 0x7b)



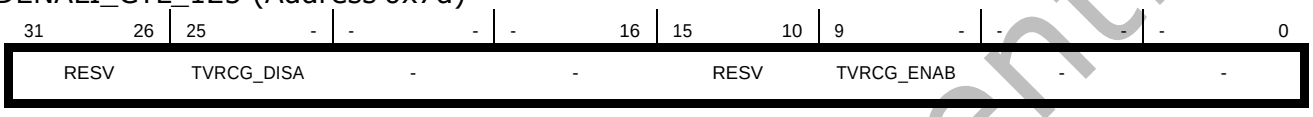
Name	Bits	Default	Range	Description
TFC_F0	25:16	0x000	0x0-0x3ff	JEDEC TFC, the frequency set
TVRCG_DISABLE_F0	9:0	0x000	0x0-0x3ff	JEDEC TVRCG_DISABLE time.

DENALI_CTL_124 (Address 0x7c)



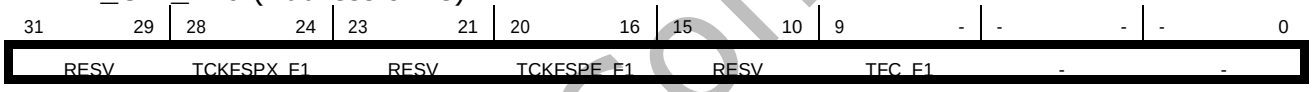
Name	Bits	Default	Range	Description
TVREF_LONG_F0	31:16	0x0000	0x0-0xffff	JEDEC TVREF, design will always
TCKFSPX_F0	12:8	0x00	0x0-0x1f	JEDEC TCKFSPX, the valid clock requirement before 1st valid
TCKFSPE_F0	4:0	0x00	0x0-0x1f	JEDEC TCKFSPE, the valid clock requirement after entering SDP

DENALI_CTL_125 (Address 0x7d)



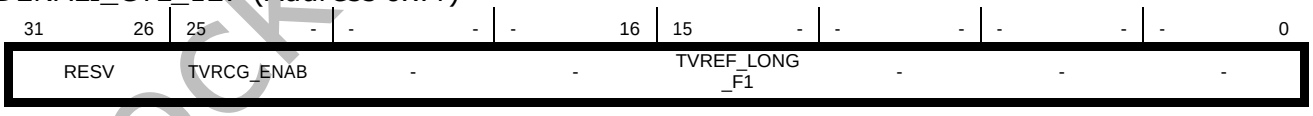
Name	Bits	Default	Range	Description
TVRCG_DISABLE_F1	25:16	0x000	0x0-0x3ff	JEDEC TVRCG_DISABLE time.
TVRCG_ENABLE_F1	9:0	0x000	0x0-0x3ff	JEDEC TVRCG_ENABLE time.

DENALI_CTL_126 (Address 0x7e)



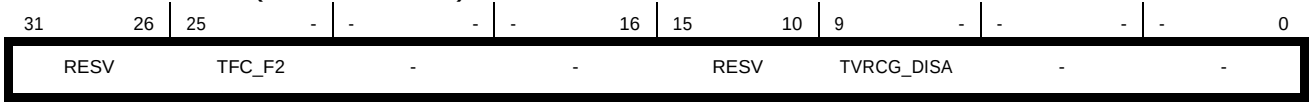
Name	Bits	Default	Range	Description
TCKFSPX_F1	28:24	0x00	0x0-0x1f	JEDEC TCKFSPX, the valid clock requirement before 1st valid
TCKFSPE_F1	20:16	0x00	0x0-0x1f	JEDEC TCKFSPE, the valid clock requirement after entering SDP
TFC_F1	9:0	0x000	0x0-0x3ff	JEDEC TFC, the frequency set

DENALI_CTL_127 (Address 0x7f)



Name	Bits	Default	Range	Description
TVRCG_ENABLE_F2	25:16	0x000	0x0-0x3ff	JEDEC TVRCG_ENABLE time.
TVREF_LONG_F1	15:0	0x0000	0x0-0xffff	JEDEC TVREF, design will always

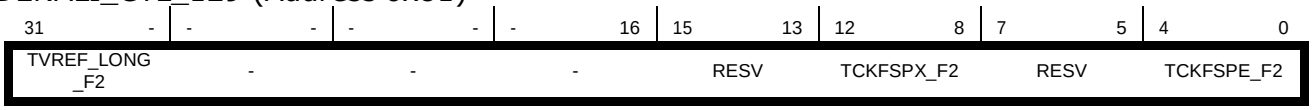
DENALI_CTL_128 (Address 0x80)



Name	Bits	Default	Range	Description
TFC_F2	25:16	0x000	0x0-0x3ff	JEDEC TFC, the frequency set

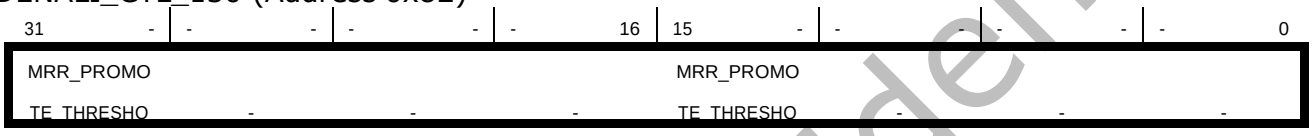
TVRCG_DISABLE_F2	9:0	0x000	0x0-0x3ff	JEDEC TVRCG_DISABLE time.

DENALI_CTL_129 (Address 0x81)



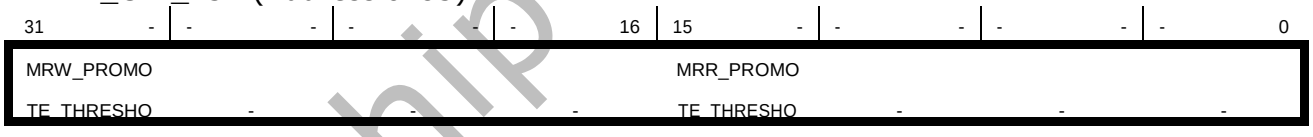
Name	Bits	Default	Range	Description
TVREF_LONG_F2	31:16	0x0000	0x0-0xffff	JEDEC TVREF, design will always
TCKFSPX_F2	12:8	0x00	0x0-0x1f	JEDEC TCKFSPX, the valid clock requirement before 1st valid
TCKFSPE_F2	4:0	0x00	0x0-0x1f	JEDEC TCKFSPE, the valid clock requirement after entering SDP

DENALI_CTL_130 (Address 0x82)



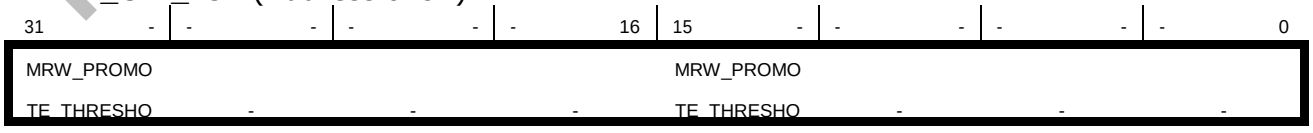
Name	Bits	Default	Range	Description
MRR_PROMOTE_THRESHOLD_F1	31:16	0x0000	0x0-0xffff	MRR promotion number of long counts until the high priority request
MRR_PROMOTE_THRESHOLD_F0	15:0	0x0000	0x0-0xffff	MRR promotion number of long counts until the high priority request

DENALI_CTL_131 (Address 0x83)



Name	Bits	Default	Range	Description
MRW_PROMOTE_THRESHOLD_F0	31:16	0x0000	0x0-0xffff	MRW promotion number of long counts until the high priority request
MRR_PROMOTE_THRESHOLD_F2	15:0	0x0000	0x0-0xffff	MRR promotion number of long counts until the high priority request

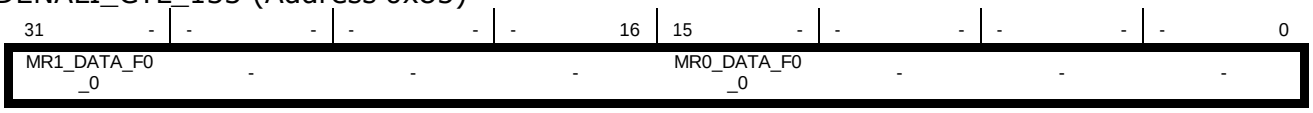
DENALI_CTL_132 (Address 0x84)



Name	Bits	Default	Range	Description
MRW_PROMOTE_THRESHOLD_F2	31:16	0x0000	0x0-0xffff	MRW promotion number of long counts until the high priority request

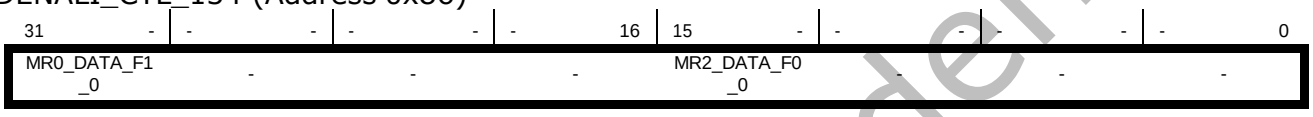
MRW_PROMOTE_THRESHOLD_F1	15:0	0x0000	0x0-0xffff	MRW promotion number of long counts until the high priority request

DENALI_CTL_133 (Address 0x85)



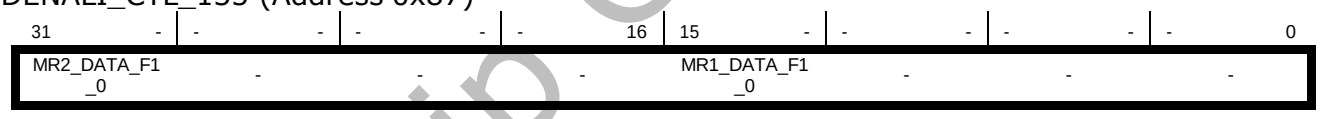
Name	Bits	Default	Range	Description
MR1_DATA_F0_0	31:16	0x0000	0x0-0xffff	Data to program into memory mode register 1 for chip select 0 for
MR0_DATA_F0_0	15:0	0x0000	0x0-0xffff	Data to program into memory mode register 0 for chip select 0 for

DENALI_CTL_134 (Address 0x86)



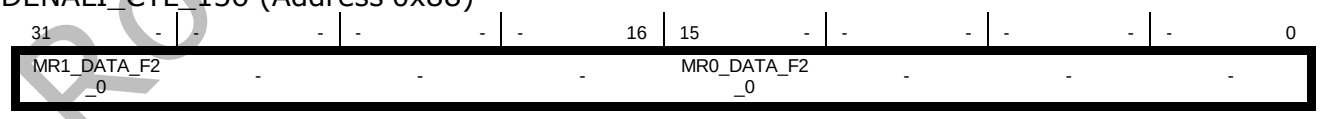
Name	Bits	Default	Range	Description
MR0_DATA_F1_0	31:16	0x0000	0x0-0xffff	Data to program into memory mode register 0 for chip select 0 for
MR2_DATA_F0_0	15:0	0x0000	0x0-0xffff	Data to program into memory mode register 2 for chip select 0 for

DENALI_CTL_135 (Address 0x87)



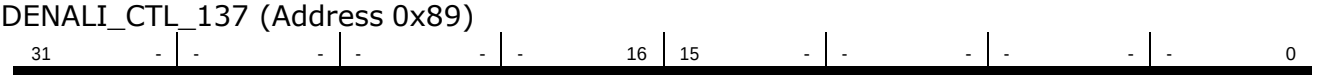
Name	Bits	Default	Range	Description
MR2_DATA_F1_0	31:16	0x0000	0x0-0xffff	Data to program into memory mode register 2 for chip select 0 for
MR1_DATA_F1_0	15:0	0x0000	0x0-0xffff	Data to program into memory mode register 1 for chip select 0 for

DENALI_CTL_136 (Address 0x88)



Name	Bits	Default	Range	Description
MR1_DATA_F2_0	31:16	0x0000	0x0-0xffff	Data to program into memory mode register 1 for chip select 0 for
MR0_DATA_F2_0	15:0	0x0000	0x0-0xffff	Data to program into memory mode register 0 for chip select 0 for

DENALI_CTL_137 (Address 0x89)



MRSINGLE_D	-	-	-	MR2_DATA_F2_0	-	-	-

Name	Bits	Default	Range	Description
MRSINGLE_DATA_0	31:16	0x0000	0x0-0xffff	Data to program into memory mode register single write to chip select
MR2_DATA_F2_0	15:0	0x0000	0x0-0xffff	Data to program into memory mode register 2 for chip select 0 for

DENALI_CTL_138 (Address 0x8a)

31	-	-	-	-	-	16	15	-	-	-	-	-	0
MR3_DATA_F1_0	-	-	-	MR3_DATA_F0_0	-	-	-						

Name	Bits	Default	Range	Description
MR3_DATA_F1_0	31:16	0x0000	0x0-0xffff	Data to program into memory mode register 3 for chip select 0 for
MR3_DATA_F0_0	15:0	0x0000	0x0-0xffff	Data to program into memory mode register 3 for chip select 0 for

DENALI_CTL_139 (Address 0x8b)

31	-	-	24	23	-	-	16	15	-	-	-	-	-	0
MR11_DATA_F0_0	-	MR8_DATA_0		-	MR3_DATA_F2_0			-	-	-				

Name	Bits	Default	Range	Description
MR11_DATA_F0_0	31:24	0x00	0x0-0xff	Data to program into memory mode register 11 for chip select 0 for
MR8_DATA_0	23:16	0x00	0x0-0xff	Data read from MR8 for chip select 0. READ-ONLY
MR3_DATA_F2_0	15:0	0x0000	0x0-0xffff	Data to program into memory mode register 3 for chip select 0 for

DENALI_CTL_140 (Address 0x8c)

31	-	-	-	-	-	16	15	-	-	8	7	-	-	0
MR12_DATA_F0_0	-	-	-	MR11_DATA_F2_0	-	MR11_DATA_F1_0	-							

Name	Bits	Default	Range	Description
MR12_DATA_F0_0	31:16	0x0000	0x0-0xffff	Data to program into memory mode
MR11_DATA_F2_0	15:8	0x00	0x0-0xff	Data to program into memory mode register 11 for chip select 0 for
MR11_DATA_F1_0	7:0	0x00	0x0-0xff	Data to program into memory mode register 11 for chip select 0 for

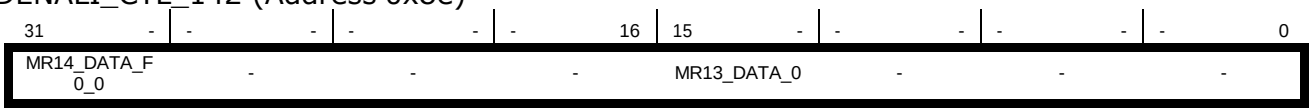
DENALI_CTL_141 (Address 0x8d)

31	-	-	-	-	-	16	15	-	-	-	-	-	0
MR12_DATA_F2_0	-	-	-	MR12_DATA_F1_0	-	-	-						

Name	Bits	Default	Range	Description

MR12_DATA_F2_0	31:16	0x0000	0x0-0xffff	Data to program into memory mode
MR12_DATA_F1_0	15:0	0x0000	0x0-0xffff	Data to program into memory mode

DENALI_CTL_142 (Address 0x8e)

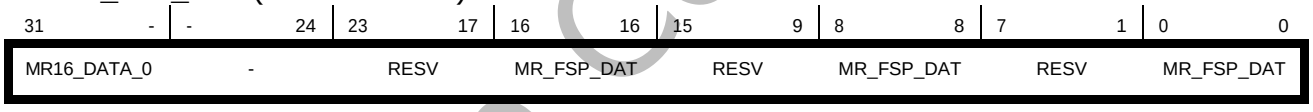


Name	Bits	Default	Range	Description
MR14_DATA_F0_0	31:16	0x0000	0x0-0xffff	Data to program into memory mode
MR13_DATA_0	15:0	0x0000	0x0-0xffff	Data to program into memory mode

DENALI_CTL_143 (Address 0x8f)

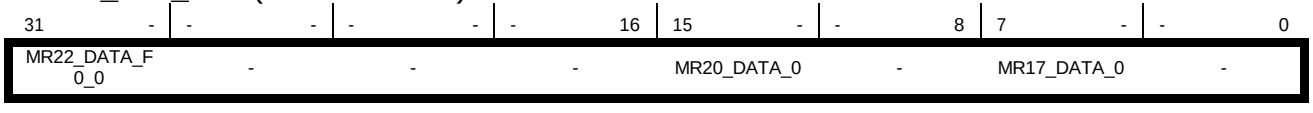
Name	Bits	Default	Range	Description
MR14_DATA_F2_0	31:16	0x0000	0x0-0xffff	Data to program into memory mode
MR14_DATA_F1_0	15:0	0x0000	0x0-0xffff	Data to program into memory mode

DENALI_CTL_144 (Address 0x90)



Name	Bits	Default	Range	Description
MR16_DATA_0	31:24	0x00	0x0-0xff	Data to program into memory mode
MR_FSP_DATA_VALID_F2_0	16	0x0	0x0-0x1	Indicates that, at this frequency, memory was trained and the associated data has been loaded
MR_FSP_DATA_VALID_F1_0	8	0x0	0x0-0x1	Indicates that, at this frequency, memory was trained and the associated data has been loaded
MR_FSP_DATA_VALID_F0_0	0	0x0	0x0-0x1	Indicates that, at this frequency, memory was trained and the associated data has been loaded

DENALI_CTL_145 (Address 0x91)



Name	Bits	Default	Range	Description

MR22_DATA_F0_0	31:16	0x0000	0x0-0xffff	Data to program into memory mode
MR20_DATA_0	15:8	0x00	0x0-0xff	Data read from MR20 for chip
MR17_DATA_0	7:0	0x00	0x0-0xff	Data to program into memory mode

DENALI_CTL_146 (Address 0x92)

Name	Bits	Default	Range	Description
MR22_DATA_F2_0	31:16	0x0000	0x0-0xffff	Data to program into memory mode
MR22_DATA_F1_0	15:0	0x0000	0x0-0xffff	Data to program into memory mode

DENALI_CTL_147 (Address 0x93)

Name	Bits	Default	Range	Description
MR1_DATA_F0_1	31:16	0x0000	0x0-0xffff	Data to program into memory mode register 1 for chip select 1 for
MR0_DATA_F0_1	15:0	0x0000	0x0-0xffff	Data to program into memory mode register 0 for chip select 1 for

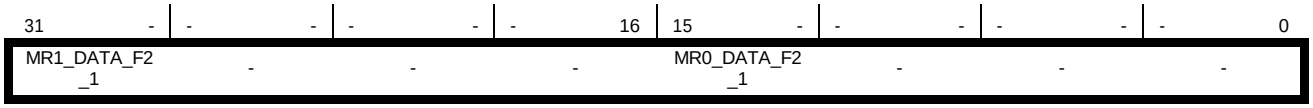
DENALI_CTL_148 (Address 0x94)

Name	Bits	Default	Range	Description
MR0_DATA_F1_1	31:16	0x0000	0x0-0xffff	Data to program into memory mode register 0 for chip select 1 for
MR2_DATA_F0_1	15:0	0x0000	0x0-0xffff	Data to program into memory mode register 2 for chip select 1 for

DENALI_CTL_149 (Address 0x95)

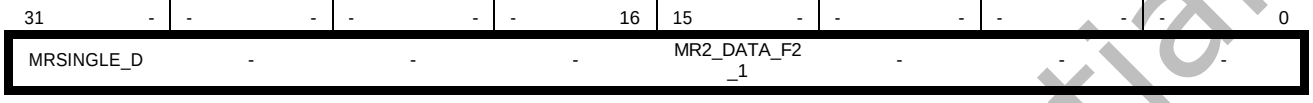
Name	Bits	Default	Range	Description
MR2_DATA_F1_1	31:16	0x0000	0x0-0xffff	Data to program into memory mode register 2 for chip select 1 for
MR1_DATA_F1_1	15:0	0x0000	0x0-0xffff	Data to program into memory mode register 1 for chip select 1 for

DENALI_CTL_150 (Address 0x96)



Name	Bits	Default	Range	Description
MR1_DATA_F2_1	31:16	0x0000	0x0-0xffff	Data to program into memory mode register 1 for chip select 1 for
MR0_DATA_F2_1	15:0	0x0000	0x0-0xffff	Data to program into memory mode register 0 for chip select 1 for

DENALI_CTL_151 (Address 0x97)



Name	Bits	Default	Range	Description
MRSINGLE_DATA_1	31:16	0x0000	0x0-0xffff	Data to program into memory mode register single write to chip select
MR2_DATA_F2_1	15:0	0x0000	0x0-0xffff	Data to program into memory mode register 2 for chip select 1 for

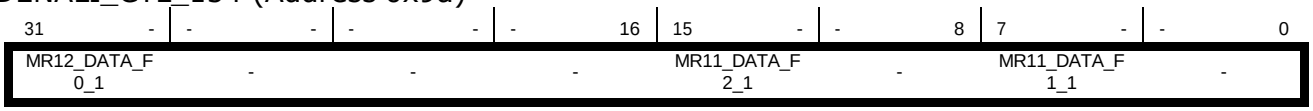
DENALI_CTL_152 (Address 0x98)

Name	Bits	Default	Range	Description
MR3_DATA_F1_1	31:16	0x0000	0x0-0xffff	Data to program into memory mode register 3 for chip select 1 for
MR3_DATA_F0_1	15:0	0x0000	0x0-0xffff	Data to program into memory mode register 3 for chip select 1 for

DENALI_CTL_153 (Address 0x99)

Name	Bits	Default	Range	Description
MR11_DATA_F0_1	31:24	0x00	0x0-0xff	Data to program into memory mode register 11 for chip select 1 for
MR8_DATA_1	23:16	0x00	0x0-0xff	Data read from MR8 for chip select 1. READ-ONLY
MR3_DATA_F2_1	15:0	0x0000	0x0-0xffff	Data to program into memory mode register 3 for chip select 1 for

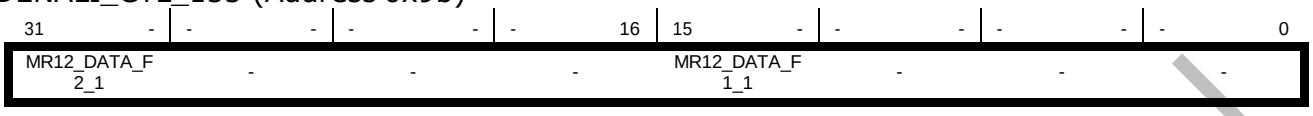
DENALI_CTL_154 (Address 0x9a)



Name	Bits	Default	Range	Description

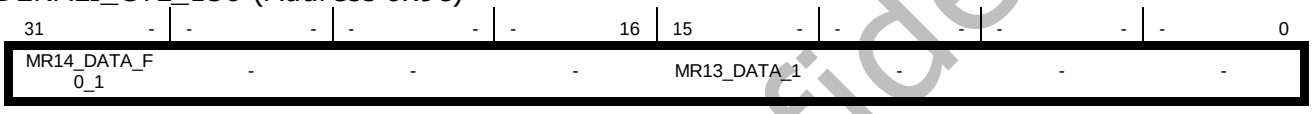
MR12_DATA_F0_1	31:16	0x0000	0x0-0xffff	Data to program into memory mode
MR11_DATA_F2_1	15:8	0x00	0x0-0xff	Data to program into memory mode register 11 for chip select 1 for
MR11_DATA_F1_1	7:0	0x00	0x0-0xff	Data to program into memory mode register 11 for chip select 1 for

DENALI_CTL_155 (Address 0x9b)



Name	Bits	Default	Range	Description
MR12_DATA_F2_1	31:16	0x0000	0x0-0xffff	Data to program into memory mode
MR12_DATA_F1_1	15:0	0x0000	0x0-0xffff	Data to program into memory mode

DENALI_CTL_156 (Address 0x9c)

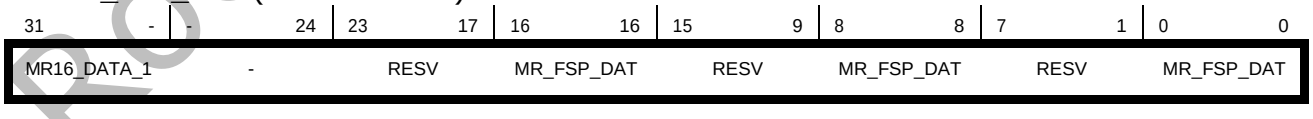


Name	Bits	Default	Range	Description
MR14_DATA_F0_1	31:16	0x0000	0x0-0xffff	Data to program into memory mode
MR13_DATA_1	15:0	0x0000	0x0-0xffff	Data to program into memory mode

DENALI_CTL_157 (Address 0x9d)

Name	Bits	Default	Range	Description
MR14_DATA_F2_1	31:16	0x0000	0x0-0xffff	Data to program into memory mode
MR14_DATA_F1_1	15:0	0x0000	0x0-0xffff	Data to program into memory mode

DENALI_CTL_158 (Address 0x9e)



Name	Bits	Default	Range	Description
MR16_DATA_1	31:24	0x00	0x0-0xff	Data to program into memory mode
MR_FSP_DATA_VALID_F2_1	16	0x0	0x0-0x1	Indicates that, at this frequency, memory was trained and the associated data has been loaded

MR_FSP_DATA_VALID_F1_1	8	0x0	0x0-0x1	Indicates that, at this frequency, memory was trained and the associated data has been loaded
MR_FSP_DATA_VALID_F0_1	0	0x0	0x0-0x1	Indicates that, at this frequency, memory was trained and the associated data has been loaded

DENALI_CTL_159 (Address 0x9f)

31 - 16	15 - 8	7 - 0
MR22_DATA_F0_1	MR20_DATA_1	MR17_DATA_1

Name	Bits	Default	Range	Description
MR22_DATA_F0_1	31:16	0x0000	0x0-0xffff	Data to program into memory mode
MR20_DATA_1	15:8	0x00	0x0-0xff	Data read from MR20 for chip
MR17_DATA_1	7:0	0x00	0x0-0xff	Data to program into memory mode

DENALI_CTL_160 (Address 0xa0)

31 - 16	15 - 0
MR22_DATA_F	MR22_DATA_F

Name	Bits	Default	Range	Description
MR22_DATA_F2_1	31:16	0x0000	0x0-0xffff	Data to program into memory mode
MR22_DATA_F1_1	15:0	0x0000	0x0-0xffff	Data to program into memory mode

DENALI_CTL_161 (Address 0xa1)

31 - 25	24 - 24	23 - 17	16 - 16	15 - 9	8 - 8	7 - 2	1 - 0
RESV	FSP_PHY_UP	RESV	RESERVED	RESV	RESERVED	RESV	RL3_SUPPOR

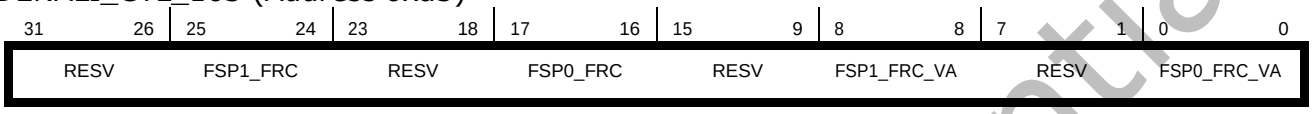
Name	Bits	Default	Range	Description
FSP_PHY_UPDATE_MRW	24	0x0	0x0-0x1	Identifies the logic responsible for updating MR12 and MR14 in memory. Clear to 0 for the
RESERVED	16	0x0	0x0-0x1	Reserved for future use. Refer to the regconfig files for the default
RESERVED	8	0x0	0x0-0x1	Reserved for future use. Refer to the regconfig files for the default
RL3_SUPPORT_EN	1:0	0x0	0x0-0x3	Indicates if RL3 is supported by a connected LPDDR3 memory. Data

DENALI_CTL_162 (Address 0xa2)

31 - 25	24 - 24	23 - 17	16 - 16	15 - 9	8 - 8	7 - 1	0 - 0
RESV	FSP_WR_CUR	RESV	FSP_OP_CUR	RESV	FSP_STATUS	RESV	DFS_ALWAYS_WRITE_FSP

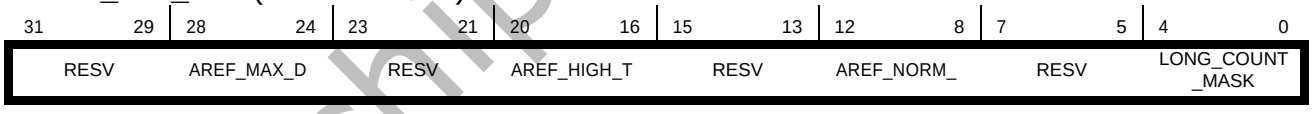
Name	Bits	Default	Range	Description
FSP_WR_CURRENT	24	0x0	0x0-0x1	Reports which FSP set the memory
FSP_OP_CURRENT	16	0x0	0x0-0x1	Reports which FSP set the memory
FSP_STATUS	8	0x0	0x0-0x1	Indicates that a DFS event caused the FSP mode registers to be
DFS_ALWAYS_WRITE_FSP	0	0x0	0x0-0x1	Forces all FSP mode registers to be written by the controller during a

DENALI_CTL_163 (Address 0xa3)



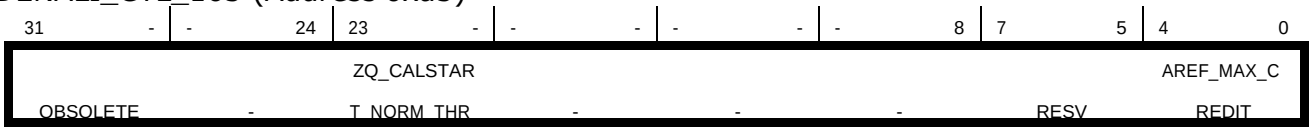
Name	Bits	Default	Range	Description
FSP1_FRC	25:24	0x0	0x0-0x3	Identifies which of the controllersfrequencycopyisassociat
FSP0_FRC	17:16	0x0	0x0-0x3	Identifies which of the controllersfrequencycopyisassociat
FSP1_FRC_VALID	8	0x0	0x0-0x1	Specifies whether the FSP set defined in the FSP1_FRC parameter reflects the frequency
FSP0_FRC_VALID	0	0x0	0x0-0x1	Specifies whether the FSP set defined in the FSP0_FRC parameter reflects the frequency

DENALI_CTL_164 (Address 0xa4)



Name	Bits	Default	Range	Description
AREF_MAX_DEFICIT	28:24	0x00	0x0-0x1f	AREF number of pending refreshes until the maximum number of
AREF_HIGH_THRESHOLD	20:16	0x00	0x0-0x1f	AREF number of pending refreshes until the high priority request is
AREF_NORM_THRESHOLD	12:8	0x00	0x0-0x1f	AREF number of pending refreshes until the normal priority request is
LONG_COUNT_MASK	4:0	0x00	0x0-0x1f	Reduces the length of the long counter from 1024 cycles. The only supported values are 0x00 (1024 cycles), 0x10 (512 clocks), 0x18

DENALI_CTL_165 (Address 0xa5)



Name	Bits	Default	Range	Description
ZQ_CALSTART_NORM_THRESHOLD_F0	23:8	0x0000	0x0-0xffff	ZQ START number of long counts until the normal priority request is asserted for frequency copy 0. This value should be scaled based on the number of ranks (chip selects)
AREF_MAX_CREDIT	4:0	0x00	0x0-0x1f	AREF number of posted refreshes until the maximum number of

DENALI_CTL_166 (Address 0xa6)

31 - 16	15 - 0
ZQ_CALLATCH_HIGH_THR -	ZQ_CALSTART_HIGH_THRE -

Name	Bits	Default	Range	Description
ZQ_CALLATCH_HIGH_THRESHOLD_F0	31:16	0x0000	0x0-0xffff	ZQ LATCH number of long counts until the high priority request is
ZQ_CALSTART_HIGH_THRESHOLD_F0	15:0	0x0000	0x0-0xffff	ZQ START number of long counts until the high priority request is

DENALI_CTL_167 (Address 0xa7)

31 - 16	15 - 0
ZQ_CS_HIGH_THRESHOLD -	ZQ_CS_NORM_THRESHOLD -

Name	Bits	Default	Range	Description
ZQ_CS_HIGH_THRESHOLD_F0	31:16	0x0000	0x0-0xffff	ZQ CS number of long counts until the high priority request is asserted
ZQ_CS_NORM_THRESHOLD_F0	15:0	0x0000	0x0-0xffff	ZQ CS number of long counts until the normal priority request is

DENALI_CTL_168 (Address 0xa8)

31 - 16	15 - 0
ZQ_CALLATCH_TIMEOUT_F -	ZQ_CALSTART_TIMEOUT_F -

Name	Bits	Default	Range	Description
ZQ_CALLATCH_TIMEOUT_F0	31:16	0x0000	0x0-0xffff	ZQ LATCH number of long counts until the timeout is asserted for
ZQ_CALSTART_TIMEOUT_F0	15:0	0x0000	0x0-0xffff	ZQ START number of long counts until the timeout is asserted for

DENALI_CTL_169 (Address 0xa9)

31 - 16	15 - 0
ZQ_PROMOTE_THRESHOL -	ZQ_CS_TIMEOUT_F0 -

Name	Bits	Default	Range	Description
ZQ_PROMOTE_THRESHOLD_F0	31:16	0x0000	0x0-0xffff	ZQ SW promotion number of long counts until the high priority request
ZQ_CS_TIMEOUT_F0	15:0	0x0000	0x0-0xffff	ZQ CS number of long counts until the timeout is asserted for

DENALI_CTL_170 (Address 0xaa)

31 - 16	15 - 0
ZQ_CALSTART_HIGH_THRE -	ZQ_CALSTART_NORM_THR -

Name	Bits	Default	Range	Description
ZQ_CALSTART_HIGH_THRESHOLD_F1	31:16	0x0000	0x0-0xffff	ZQ START number of long counts until the high priority request is
ZQ_CALSTART_NORM_THRESHOLD_F1	15:0	0x0000	0x0-0xffff	ZQ START number of long counts until the normal priority request is asserted for frequency copy 1. This value should be scaled based on the number of ranks (chip selects)

DENALI_CTL_171 (Address 0xab)

31 - 16	15 - 0
ZQ_CS_NORM_THRESHOLD_F1 -	ZQ_CALLATCH_HIGH_THR -

Name	Bits	Default	Range	Description
ZQ_CS_NORM_THRESHOLD_F1	31:16	0x0000	0x0-0xffff	ZQ CS number of long counts until the normal priority request is
ZQ_CALLATCH_HIGH_THRESHOLD_F1	15:0	0x0000	0x0-0xffff	ZQ LATCH number of long counts until the high priority request is

DENALI_CTL_172 (Address 0xac)

31 - 16	15 - 0
ZQ_CALSTART_TIMEOUT_F -	ZQ_CS_HIGH_THRESHOLD -

Name	Bits	Default	Range	Description
ZQ_CALSTART_TIMEOUT_F1	31:16	0x0000	0x0-0xffff	ZQ START number of long counts until the timeout is asserted for
ZQ_CS_HIGH_THRESHOLD_F1	15:0	0x0000	0x0-0xffff	ZQ CS number of long counts until the high priority request is asserted

DENALI_CTL_173 (Address 0xad)

31 - 16	15 - 0
ZQ_CS_TIMEOUT_F1 -	ZQ_CALLATCH_TIMEOUT_F -

Name	Bits	Default	Range	Description
ZQ_CS_TIMEOUT_F1	31:16	0x0000	0x0-0xffff	ZQ CS number of long counts until the timeout is asserted for
ZQ_CALLATCH_TIMEOUT_F1	15:0	0x0000	0x0-0xffff	ZQ LATCH number of long counts until the timeout is asserted for

DENALI_CTL_174 (Address 0xae)

31 - 16	15 - 0
ZQ_CALSTART_NORM_THR	ZQ_PROMOTE_THRESHOL

Name	Bits	Default	Range	Description
ZQ_CALSTART_NORM_THRESHOLD_F2	31:16	0x0000	0x0-0xffff	ZQ START number of long counts until the normal priority request is asserted for frequency copy 2. This value should be scaled based on the number of ranks (chip selects)
ZQ_PROMOTE_THRESHOLD_F1	15:0	0x0000	0x0-0xffff	ZQ SW promotion number of long counts until the high priority request

DENALI_CTL_175 (Address 0xaf)

31 - 16	15 - 0
ZQ_CALLATCH_HIGH_THR	ZQ_CALSTART_HIGH_THRE

Name	Bits	Default	Range	Description
ZQ_CALLATCH_HIGH_THRESHOLD_F2	31:16	0x0000	0x0-0xffff	ZQ LATCH number of long counts until the high priority request is
ZQ_CALSTART_HIGH_THRESHOLD_F2	15:0	0x0000	0x0-0xffff	ZQ START number of long counts until the high priority request is

DENALI_CTL_176 (Address 0xb0)

31 - 16	15 - 0
ZQ_CS_HIGH_THRESHOLD	ZQ_CS_NORM_THRESHOLD

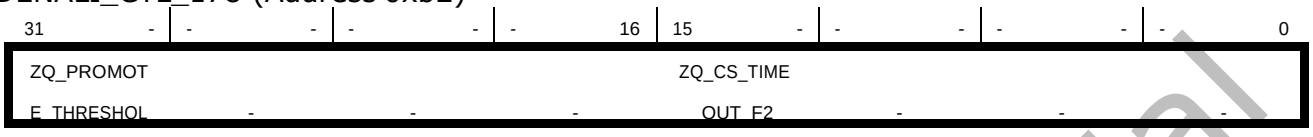
Name	Bits	Default	Range	Description
ZQ_CS_HIGH_THRESHOLD_F2	31:16	0x0000	0x0-0xffff	ZQ CS number of long counts until the high priority request is asserted
ZQ_CS_NORM_THRESHOLD_F2	15:0	0x0000	0x0-0xffff	ZQ CS number of long counts until the normal priority request is

DENALI_CTL_177 (Address 0xb1)

31 - 16	15 - 0
ZQ_CALLATCH_TIMEOUT_F	ZQ_CALSTART_TIMEOUT_F

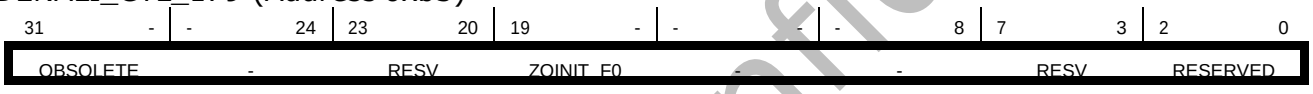
Name	Bits	Default	Range	Description
ZQ_CALLATCH_TIMEOUT_F2	31:16	0x0000	0x0-0xffff	ZQ LATCH number of long counts until the timeout is asserted for
ZQ_CALSTART_TIMEOUT_F2	15:0	0x0000	0x0-0xffff	ZQ START number of long counts until the timeout is asserted for

DENALI_CTL_178 (Address 0xb2)



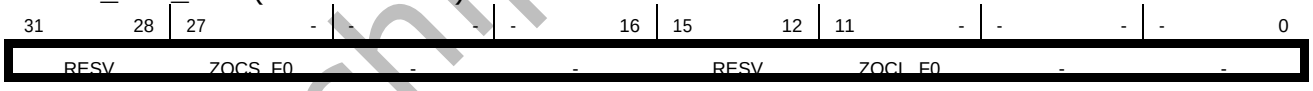
Name	Bits	Default	Range	Description
ZQ_PROMOTE_THRESHOLD_F2	31:16	0x0000	0x0-0xffff	ZQ SW promotion number of long counts until the high priority request
ZQ_CS_TIMEOUT_F2	15:0	0x0000	0x0-0xffff	ZQ CS number of long counts until the timeout is asserted for

DENALI_CTL_179 (Address 0xb3)



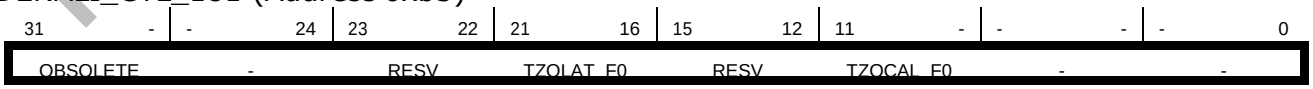
Name	Bits	Default	Range	Description
ZQINIT_F0	19:8	0x000	0x0-0xfff	Number of cycles needed for a ZQINIT command for frequency
RESERVED	2:0	0x0	0x0-0x7	Reserved for future use. Refer to the regconfig files for the default

DENALI_CTL_180 (Address 0xb4)



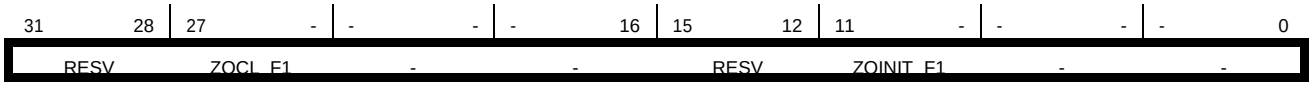
Name	Bits	Default	Range	Description
ZQCS_F0	27:16	0x000	0x0-0xfff	Number of cycles needed for a ZQCS command for frequency
ZQCL_F0	11:0	0x000	0x0-0xfff	Number of cycles needed for a ZQCL command for frequency

DENALI_CTL_181 (Address 0xb5)



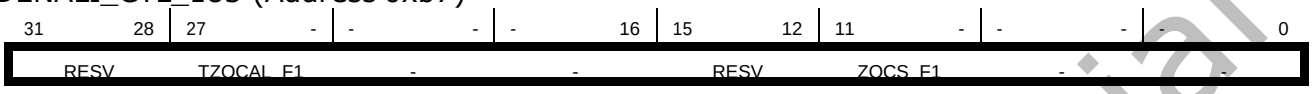
Name	Bits	Default	Range	Description
TZQLAT_F0	21:16	0x00	0x0-0x3f	Holds the DRAM ZQLAT value for
TZQCAL_F0	11:0	0x000	0x0-0xfff	Holds the DRAM ZQCAL value for

DENALI_CTL_182 (Address 0xb6)



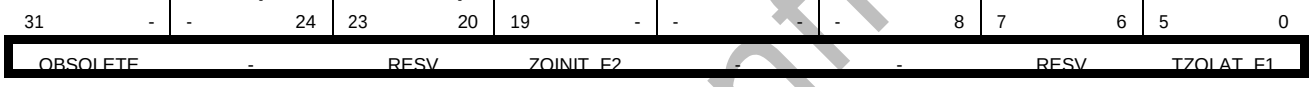
Name	Bits	Default	Range	Description
ZQCL_F1	27:16	0x000	0x0-0xfff	Number of cycles needed for a ZQCL command for frequency
ZQINIT_F1	11:0	0x000	0x0-0xfff	Number of cycles needed for a ZQINIT command for frequency

DENALI_CTL_183 (Address 0xb7)



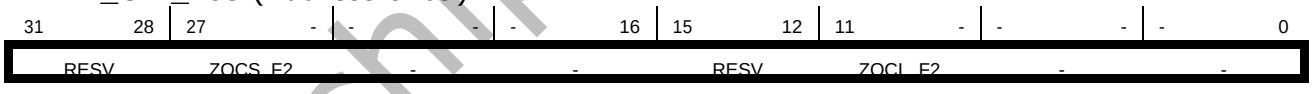
Name	Bits	Default	Range	Description
TZQCAL_F1	27:16	0x000	0x0-0xfff	Holds the DRAM ZQCAL value for
ZQCS_F1	11:0	0x000	0x0-0xfff	Number of cycles needed for a ZQCS command for frequency

DENALI_CTL_184 (Address 0xb8)



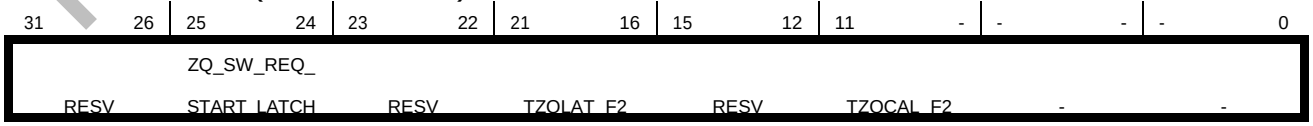
Name	Bits	Default	Range	Description
ZQINIT_F2	19:8	0x000	0x0-0xfff	Number of cycles needed for a ZQINIT command for frequency
TZQLAT_F1	5:0	0x00	0x0-0x3f	Holds the DRAM ZQLAT value for

DENALI_CTL_185 (Address 0xb9)



Name	Bits	Default	Range	Description
ZQCS_F2	27:16	0x000	0x0-0xfff	Number of cycles needed for a ZQCS command for frequency
ZQCL_F2	11:0	0x000	0x0-0xfff	Number of cycles needed for a ZQCL command for frequency

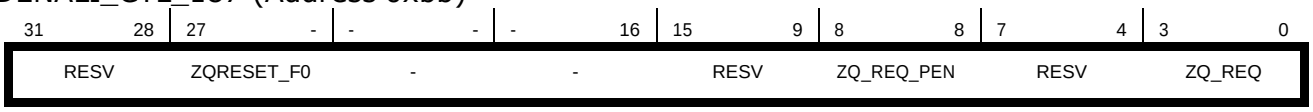
DENALI_CTL_186 (Address 0xba)



Name	Bits	Default	Range	Description
ZQ_SW_REQ_START_LATCH_MAP	25:24	0x0	0x0-0x3	Specifies which chip selects will simultaneously receive a ZQ start or latch command once the
TZQLAT_F2	21:16	0x00	0x0-0x3f	Holds the DRAM ZQLAT value for

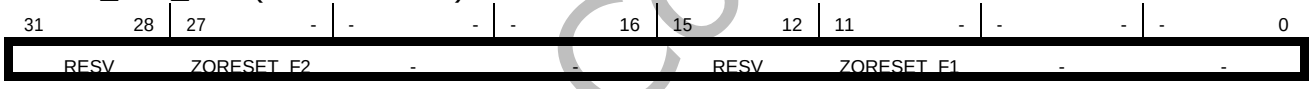
TZQCAL_F2	11:0	0x000	0x0-0xfff	Holds the DRAM ZQCAL value for

DENALI_CTL_187 (Address 0xbb)



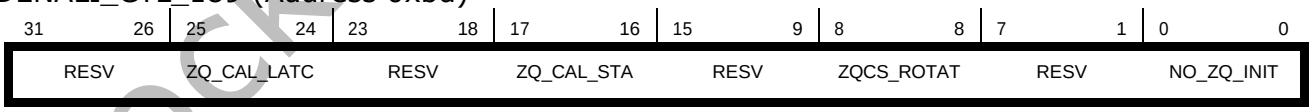
Name	Bits	Default	Range	Description
ZQRESET_F0	27:16	0x000	0x0-0xfff	Number of cycles needed for a ZQRESET command forfrequency
ZQ_REQ_PENDING	8	0x0	0x0-0x1	Indicates that a ZQ command is currently in progress or waiting to run. Value of 1 indicates command in progress or waiting to run. When
ZQ_REQ	3:0	0x0	0x0-0xf	User request to initiate a ZQ calibration. Program to 0x1 for ZQ Short (ZQCS), program to 0x2 for ZQ Long (ZQCL), program to 0x3 for ZQ Start, program to 0x4 for ZQ Initialization (ZQINIT), program to 0x5 for ZQ Latch, or program to

DENALI_CTL_188 (Address 0xbc)



Name	Bits	Default	Range	Description
ZQRESET_F2	27:16	0x000	0x0-0xfff	Number of cycles needed for a ZQRESET command forfrequency
ZQRESET_F1	11:0	0x000	0x0-0xfff	Number of cycles needed for a ZQRESET command forfrequency

DENALI_CTL_189 (Address 0xbd)



Name	Bits	Default	Range	Description
ZQ_CAL_LATCH_MAP_0	25:24	0x1	0x0-0x3	Defines which chip select(s) will receive ZQ calibration latch commands simultaneously on iteration 0 of the ZQ LATCH
ZQ_CAL_START_MAP_0	17:16	0x1	0x0-0x3	Defines which chip select(s) will receive ZQ calibration start commands simultaneously on iteration 0 of the ZQ START

ZQCS_ROTATE	8	0x0	0x0-0x1	For non-LPDDR4 memories, selects whether a ZQCS command will calibrate just one chip select or all chip selects. When rotation is off, all chip selects will be calibrated, requiring a longer time
NO_ZQ_INIT	0	0x0	0x0-0x1	Disable ZQ operations during

DENALI_CTL_190 (Address 0xbe)

31 27	26 24	23 18	17 16	15 10	9 8	7 2	1 0
RESV	ROW_DIFF	RESV	BANK_DIFF	RESV	ZQ_CAL_LATC	RESV	ZQ_CAL_STA

Name	Bits	Default	Range	Description
ROW_DIFF	26:24	0x0	0x0-0x7	Difference between number of address pins available and number
BANK_DIFF	17:16	0x0	0x0-0x3	Encoded number of banks on the
ZQ_CAL_LATCH_MAP_1	9:8	0x2	0x0-0x3	Defines which chip select(s) will receive ZQ calibration latch commands simultaneously on iteration 1 of the ZQ LATCH
ZQ_CAL_START_MAP_1	1:0	0x2	0x0-0x3	Defines which chip select(s) will receive ZQ calibration start commands simultaneously on iteration 1 of the ZQ START

DENALI_CTL_191 (Address 0xbf)

31 28	27 24	23 17	16 16	15 13	12 8	7 4	3 0
RESV	APREBIT	RESV	BANK_ADDR_I	RESV	BANK_START_BIT	RESV	COL_DIFF

Name	Bits	Default	Range	Description
APREBIT	27:24	0xa	0x0-0xf	Location of the auto pre-charge bit
BANK_ADDR_INTLV_EN	16	0x0	0x0-0x1	Enables the capability to interleave the bank address within the row
BANK_START_BIT	12:8	0x00	0x0-0x1f	Defines the LSbit of the bank address within the page of the user address when the
COL_DIFF	3:0	0x0	0x0-0xf	Difference between number of column pins available and number

DENALI_CTL_192 (Address 0xc0)

31 25	24 24	23 17	16 16	15 12	11 8	7 4	3 0
RESV	RESERVED	RESV	ADDR_CMP_E	RESV	COMMAND_A	RESV	AGE_COUNT

Name	Bits	Default	Range	Description

RESERVED	24	0x0	0x0-0x1	Reserved for future use. Refer to the regconfig files for the default
ADDR_CMP_EN	16	0x0	0x0-0x1	Enable address collision detection as a rule for command queue
COMMAND_AGE_COUNT	11:8	0x0	0x0-0xf	Initial value of individual command
AGE_COUNT	3:0	0x0	0x0-0xf	Initial value of master aging-rate

DENALI_CTL_193 (Address 0xc1)

31 25	24 24	23 17	16 16	15 9	8 8	7 1	0 0
RESV	RW_SAME_E	RESV	PRIORITY_EN	RESV	PLACEMENT_	RESV	BANK_SPLIT_

Name	Bits	Default	Range	Description
RW_SAME_EN	24	0x0	0x0-0x1	Enable read/write grouping as a rule for command queue
PRIORITY_EN	16	0x0	0x0-0x1	Enable priority as a rule for command queue placement. Set to
PLACEMENT_EN	8	0x0	0x0-0x1	Enable placement logic for command queue. Set to 1 to
BANK_SPLIT_EN	0	0x0	0x0-0x1	Enable bank splitting as a rule for command queue placement. Set to

DENALI_CTL_194 (Address 0xc2)

31 26	25 24	23 17	16 16	15 9	8 8	7 1	0 0
RESV	DISABLE_RW_GROUP_W_B	RESV	W2R_SPLIT_E N	RESV	CS_SAME_EN	RESV	RW_SAME_PA GE_EN

Name	Bits	Default	Range	Description
DISABLE_RW_GROUP_W_BNK_CONFLIC	25:24	0x0	0x0-0x3	Disables placement to read/write group when grouping creates a bank collision. Bit (0) controls placement next to bank conflict
W2R_SPLIT_EN	16	0x0	0x0-0x1	Enable splitting of commands to the same chip select from a write to
CS_SAME_EN	8	0x0	0x0-0x1	Enable chip select grouping when read/write grouping as a rule for command queue placement. This
RW_SAME_PAGE_EN	0	0x0	0x0-0x1	Enable page grouping when read/ write grouping as a rule for command queue placement. This

DENALI_CTL_195 (Address 0xc3)

31 26	25 24	23 17	16 16	15 9	8 8	7 3	2 0
RESV	INHIBIT_DRA M_CMD	RESV	DISABLE_RD_ INTERLEAVE	RESV	SWAP_EN	RESV	NUM_Q_ENTR IES_ACT_DIS

Name	Bits	Default	Range	Description
INHIBIT_DRAM_CMD	25:24	0x0	0x0-0x3	Inhibit command types from being executed from the command queue. Clear to 0 to enable any command, program to 1 to inhibit read/write and bank commands,
DISABLE_RD_INTERLEAVE	16	0x0	0x0-0x1	Disable read data interleaving for commands from the same port,
SWAP_EN	8	0x0	0x0-0x1	Enable command swapping logic in
NUM_Q_ENTRIES_ACT_DISABLE	2:0	0x0	0x0-0x7	Number of queue entries in which ACT requests will be disabled. Setting to X will disable ACT

DENALI_CTL_196 (Address 0xc4)

31 25	24 24	23 17	16 16	15 12	11 8	7 2	1 0
RESV	BIG_ENDIAN_	RESV	REDUC	RESV	BURST_ON_F	RESV	CS_MAP

Name	Bits	Default	Range	Description
BIG_ENDIAN_EN	24	0x0	0x0-0x1	Set byte ordering as little endian or
REDUC	16	0x0	0x0-0x1	Enable the half datapath feature of
BURST_ON_FLY_BIT	11:8	0x0	0x0-0xf	Identifies the burst-on-fly bit in the
CS_MAP	1:0	0x0	0x0-0x3	Defines which chip selects are

DENALI_CTL_197 (Address 0xc5)

31 28	27 24	23 20	19 16	15 12	11 8	7 3	2 0
RESV	RESERVED	RESV	RESERVED	RESV	RESERVED	RESV	MEMDATA_RA

Name	Bits	Default	Range	Description
RESERVED	27:24	0x0	0x0-0xf	Reserved for future use. Refer to the regconfig files for the default
RESERVED	19:16	0x0	0x0-0xf	Reserved for future use. Refer to the regconfig files for the default
RESERVED	11:8	0x0	0x0-0xf	Reserved for future use. Refer to the regconfig files for the default
MEMDATA_RATIO_0	2:0	0x0	0x0-0x7	Defines the ratio of the DRAM device size on chip select 0 to the memory data width. Program with

DENALI_CTL_198 (Address 0xc6)

31 28	27 24	23 20	19 16	15 11	10 8	7 4	3 0
RESV	RESERVED	RESV	RESERVED	RESV	MEMDATA_RA	RESV	RESERVED

Name	Bits	Default	Range	Description

RESERVED	27:24	0x0	0x0-0xf	Reserved for future use. Refer to the regconfig files for the default
RESERVED	19:16	0x0	0x0-0xf	Reserved for future use. Refer to the regconfig files for the default
MEMDATA_RATIO_1	10:8	0x0	0x0-0x7	Defines the ratio of the DRAM device size on chip select 1 to the memory data width. Program with
RESERVED	3:0	0x0	0x0-0xf	Reserved for future use. Refer to the regconfig files for the default

DENALI_CTL_199 (Address 0xc7)

31 25	24 24	23 19	18 16	15 12	11 8	7 4	3 0
RESV	IN_ORDER_A	RESV	Q_FULLNESS	RESV	RESERVED	RESV	RESERVED

Name	Bits	Default	Range	Description
IN_ORDER_ACCEPT	24	0x0	0x0-0x1	Forces the controller to accept commands in the order in which
Q_FULLNESS	18:16	0x0	0x0-0x7	Quantity that determines command
RESERVED	11:8	0x0	0x0-0xf	Reserved for future use. Refer to the regconfig files for the default
RESERVED	3:0	0x0	0x0-0xf	Reserved for future use. Refer to the regconfig files for the default

DENALI_CTL_200 (Address 0xc8)

31 26	25 24	23 17	16 16	15 9	8 8	7 1	0 0
RESV	PREAMBLE_SUPPORT	RESV	CTRLUPD_REQ_PER_AREF_EN	RESV	CTRLUPD_REQ	RESV	CONTROLLER_BUSY

Name	Bits	Default	Range	Description
PREAMBLE_SUPPORT	25:24	0x0	0x0-0x3	Selection of one or two cycle preamble for read and write burst
CTRLUPD_REQ_PER_AREF_EN	16	0x0	0x0-0x1	Enable an automatic controller-initiated update (dfi_ctrlupd_req)
CTRLUPD_REQ	8	0x0	0x0-0x1	Assert the DFI controller-initiated update request signal
CONTROLLER_BUSY	0	0x0	0x0-0x1	Indicator that the controller is processing a command. Evaluates all ports for outstanding

DENALI_CTL_201 (Address 0xc9)

31 29	28 24	23 17	16 16	15 9	8 8	7 1	0 0
RESV	DFI_ERROR	RESV	RD_DBI_EN	RESV	WR_DBI_EN	RESV	RD_PREAMBLE_TRAINING

Name	Bits	Default	Range	Description

DFI_ERROR	28:24	0x00	0x0-0x1f	Indicates that the DFI error flag has
RD_DBI_EN	16	0x0	0x0-0x1	Enables controller support of DRAM DBI feature for read data
WR_DBI_EN	8	0x0	0x0-0x1	Enables controller support of DRAM DBI feature for write data
RD_PREAMBLE_TRAINING_EN	0	0x0	0x0-0x1	Enable read preamble training during gate training. Set to 1 to

DENALI_CTL_202 (Address 0xca)

31 25	24 24	23 20	19 -	- -	- -	- -	- 0
RESV	RESERVED	RESV	DFI_ERROR_I	-	-	-	-

Name	Bits	Default	Range	Description
RESERVED	24	0x0	0x0-0x1	Reserved for future use. Refer to the regconfig files for the default
DFI_ERROR_INFO	19:0	0x00000	0x0-0xfffff	Holds the encoded DFI error type associated with the DFI_ERROR

DENALI_CTL_203 (Address 0xcb)

31 -	- -	- -	- -	- -	- -	- -	- 0
INT_STATUS-	-	-	-	-	-	-	-

Name	Bits	Default	Range	Description
INT_STATUS [31:0]	31:0	0x00000000	0x0-0xffffffff	Status of interrupt features in the

DENALI_CTL_204 (Address 0xcc)

31 -	- -	- -	- -	- -	- 8	7 2	1 0
OBSOLETE	-	-	-	-	-	RESV	INT_STATUS-

Name	Bits	Default	Range	Description
INT_STATUS [33:32]	1:0	0x0	0x0-0x3	Status of interrupt features in the

DENALI_CTL_205 (Address 0xcd)

31 -	- -	- -	- -	- -	- -	- -	- 0
INT_ACK-	-	-	-	-	-	-	-

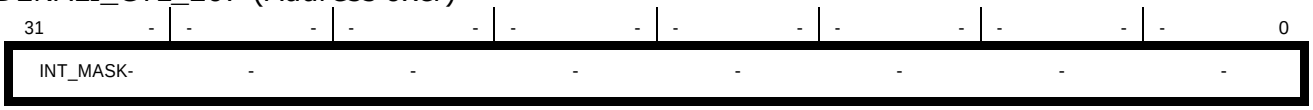
Name	Bits	Default	Range	Description
INT_ACK [31:0]	31:0	0x000000	0x0-0xffffffff	Clear mask of the INT_STATUS

DENALI_CTL_206 (Address 0xce)

31 -	- -	- -	- -	- -	- 8	7 1	0 0
OBSOLETE	-	-	-	-	-	RESV	INT_ACK-[32]

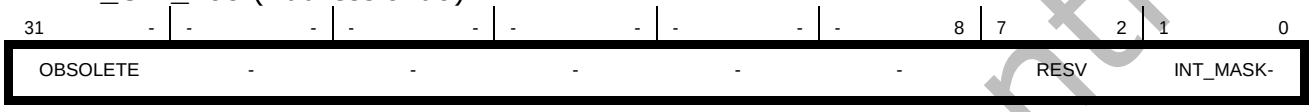
Name	Bits	Default	Range	Description
INT_ACK [32]	0	0x0	0x0-0x1	Clear mask of the INT_STATUS

DENALI_CTL_207 (Address 0xcf)



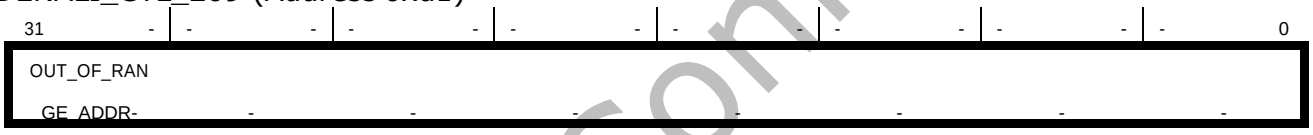
Name	Bits	Default	Range	Description
INT_MASK [31:0]	31:0	0x00000000	0x0-0xffffffff	Mask for the controller_int signal

DENALI_CTL_208 (Address 0xd0)



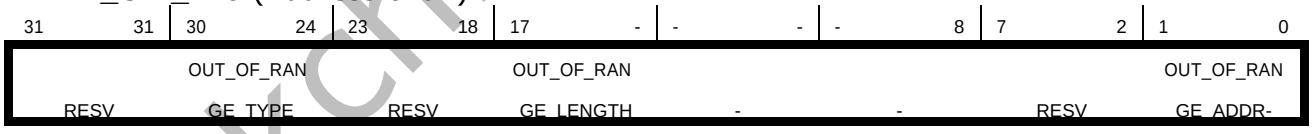
Name	Bits	Default	Range	Description
INT_MASK [33:32]	1:0	0x0	0x0-0x3	Mask for the controller_int signal

DENALI_CTL_209 (Address 0xd1)



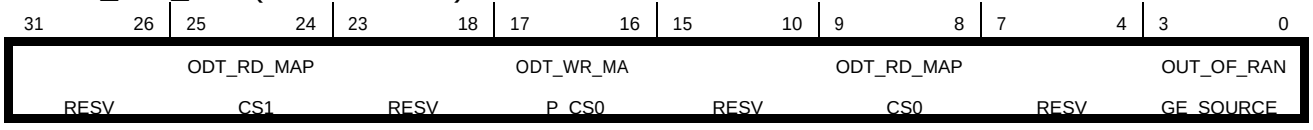
Name	Bits	Default	Range	Description
OUT_OF_RANGE_ADDR [31:0]	31:0	0x00000000	0x0-0xffffffff	Address of command that caused an out-of-range interrupt. READ-

DENALI_CTL_210 (Address 0xd2)



Name	Bits	Default	Range	Description
OUT_OF_RANGE_TYPE	30:24	0x00	0x0-0x7f	Type of command that caused an
OUT_OF_RANGE_LENGTH	17:8	0x000	0x0-0x3ff	Length of command that caused an
OUT_OF_RANGE_ADDR [33:32]	1:0	0x0	0x0-0x3	Address of command that caused an out-of-range interrupt. READ-

DENALI_CTL_211 (Address 0xd3)



Name	Bits	Default	Range	Description

ODT_RD_MAP_CS1	25:24	0x0	0x0-0x3	Determines which chip(s) will have termination when a read occurs on chip select 1. Set bit X to enable
ODT_WR_MAP_CS0	17:16	0x0	0x0-0x3	Determines which chip(s) will have termination when a write occurs on chip select 0. Set bit X to enable
ODT_RD_MAP_CS0	9:8	0x0	0x0-0x3	Determines which chip(s) will have termination when a read occurs on chip select 0. Set bit X to enable
OUT_OF_RANGE_SOURCE_ID	3:0	0x0	0x0-0xf	Source ID of command that caused an out-of-range interrupt. READ-

DENALI_CTL_212 (Address 0xd4)

31 - 24	23 - 16	15 - 8	7 - 2	1 - 0
TODTL_2CMD_F2	TODTL_2CMD_F1	TODTL_2CMD_F0	RESV	ODT_WR_MA

Name	Bits	Default	Range	Description
TODTL_2CMD_F2	31:24	0x00	0x0-0xff	Defines the DRAM delay from an ODT de-assertion to the next non-
TODTL_2CMD_F1	23:16	0x00	0x0-0xff	Defines the DRAM delay from an ODT de-assertion to the next non-
TODTL_2CMD_F0	15:8	0x00	0x0-0xff	Defines the DRAM delay from an ODT de-assertion to the next non-
ODT_WR_MAP_CS1	1:0	0x0	0x0-0x3	Determines which chip(s) will have termination when a write occurs on chip select 1. Set bit X to enable

DENALI_CTL_213 (Address 0xd5)

31 - 25	24 - 24	23 - 17	16 - 16	15 - 12	11 - 8	7 - 4	3 - 0
RESV	ODT_EN_F1	RESV	ODT_EN_F0	RESV	TODTH_RD	RESV	TODTH_WR

Name	Bits	Default	Range	Description
ODT_EN_F1	24	0x0	0x0-0x1	Enable support of DRAM ODT. When enabled, controller will
ODT_EN_F0	16	0x0	0x0-0x1	Enable support of DRAM ODT. When enabled, controller will
TODTH_RD	11:8	0x0	0x0-0xf	Defines the DRAM minimum ODT high time after an ODT assertion
TODTH_WR	3:0	0x0	0x0-0xf	Defines the DRAM minimum ODT high time after an ODT assertion

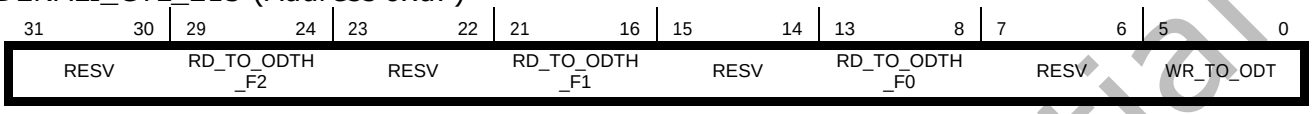
DENALI_CTL_214 (Address 0xd6)

31 - 30	29 - 24	23 - 22	21 - 16	15 - 9	8 - 8	7 - 1	0 - 0
RESV	WR_TO_ODTH_F1	RESV	WR_TO_ODTH_F0	RESV	EN_ODT_ASSERT_EXCEPT	RESV	ODT_EN_F2

Name	Bits	Default	Range	Description

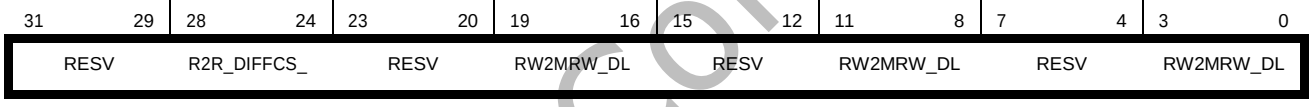
WR_TO_ODTH_F1	29:24	0x00	0x0-0x3f	Defines the delay from a write
WR_TO_ODTH_F0	21:16	0x00	0x0-0x3f	Defines the delay from a write
EN_ODT_ASSERT_EXCEPT_RD	8	0x0	0x0-0x1	Enable controller to assert ODT at all times except during reads.
ODT_EN_F2	0	0x0	0x0-0x1	Enable support of DRAM ODT. When enabled, controller will

DENALI_CTL_215 (Address 0xd7)



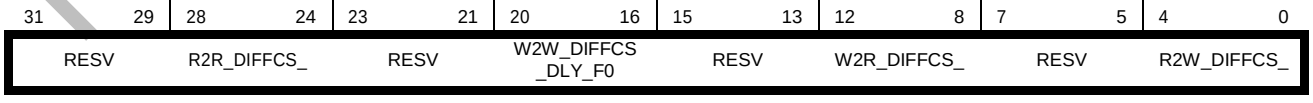
Name	Bits	Default	Range	Description
RD_TO_ODTH_F2	29:24	0x00	0x0-0x3f	Defines the delay from a read
RD_TO_ODTH_F1	21:16	0x00	0x0-0x3f	Defines the delay from a read
RD_TO_ODTH_F0	13:8	0x00	0x0-0x3f	Defines the delay from a read
WR_TO_ODTH_F2	5:0	0x00	0x0-0x3f	Defines the delay from a write

DENALI_CTL_216 (Address 0xd8)



Name	Bits	Default	Range	Description
R2R_DIFFCS_DLY_F0	28:24	0x01	0x0-0x1f	Additional delay to insert between reads to different chip selects.
RW2MRW_DLY_F2	19:16	0x8	0x0-0xf	Additional delay to insert between read or write and mode_reg_write.
RW2MRW_DLY_F1	11:8	0x8	0x0-0xf	Additional delay to insert between read or write and mode_reg_write.
RW2MRW_DLY_F0	3:0	0x8	0x0-0xf	Additional delay to insert between read or write and mode_reg_write.

DENALI_CTL_217 (Address 0xd9)



Name	Bits	Default	Range	Description
R2R_DIFFCS_DLY_F1	28:24	0x01	0x0-0x1f	Additional delay to insert between reads to different chip selects.
W2W_DIFFCS_DLY_F0	20:16	0x01	0x0-0x1f	Additional delay to insert between writes to different chip selects.

W2R_DIFFCS_DLY_F0	12:8	0x01	0x0-0x1f	Additional delay to insert between writes and reads to different chip
R2W_DIFFCS_DLY_F0	4:0	0x01	0x0-0x1f	Additional delay to insert between reads and writes to different chip

DENALI_CTL_218 (Address 0xda)

31 29	28 24	23 21	20 16	15 13	12 8	7 5	4 0
RESV	R2R_DIFFCS_	RESV	W2W_DIFFCS_DLY_F1	RESV	W2R_DIFFCS_	RESV	R2W_DIFFCS_

Name	Bits	Default	Range	Description
R2R_DIFFCS_DLY_F2	28:24	0x01	0x0-0x1f	Additional delay to insert between reads to different chip selects.
W2W_DIFFCS_DLY_F1	20:16	0x01	0x0-0x1f	Additional delay to insert between writes to different chip selects.
W2R_DIFFCS_DLY_F1	12:8	0x01	0x0-0x1f	Additional delay to insert between writes and reads to different chip
R2W_DIFFCS_DLY_F1	4:0	0x01	0x0-0x1f	Additional delay to insert between reads and writes to different chip

DENALI_CTL_219 (Address 0xdb)

31 29	28 24	23 21	20 16	15 13	12 8	7 5	4 0
RESV	R2R_SAMECS_DLY	RESV	W2W_DIFFCS_DLY_F2	RESV	W2R_DIFFCS_	RESV	R2W_DIFFCS_

Name	Bits	Default	Range	Description
R2R_SAMECS_DLY	28:24	0x00	0x0-0x1f	Additional delay to insert between two reads to the same chip select.
W2W_DIFFCS_DLY_F2	20:16	0x01	0x0-0x1f	Additional delay to insert between writes to different chip selects.
W2R_DIFFCS_DLY_F2	12:8	0x01	0x0-0x1f	Additional delay to insert between writes and reads to different chip
R2W_DIFFCS_DLY_F2	4:0	0x01	0x0-0x1f	Additional delay to insert between reads and writes to different chip

DENALI_CTL_220 (Address 0xdc)

31 29	28 24	23 21	20 16	15 13	12 8	7 5	4 0
RESV	W2R_SAMEC	RESV	R2W_SAMEC	RESV	R2W_SAMEC	RESV	R2W_SAMEC

Name	Bits	Default	Range	Description
W2R_SAMECS_DLY	28:24	0x00	0x0-0x1f	Additional delay to insert between writes and reads to the same chip
R2W_SAMECS_DLY_F2	20:16	0x02	0x0-0x1f	Additional delay to insert between reads and writes to the same chip

R2W_SAMECS_DLY_F1	12:8	0x02	0x0-0x1f	Additional delay to insert between reads and writes to the same chip
R2W_SAMECS_DLY_F0	4:0	0x02	0x0-0x1f	Additional delay to insert between reads and writes to the same chip

DENALI_CTL_221 (Address 0xdd)

31 28	27 24	23 18	17 16	15 12	11 8	7 5	4 0
RESV	TDQSCK_MAX_F1	RESV	TDQSCK_MIN_F0	RESV	TDQSCK_MAX_F0	RESV	W2W_SAMEC

Name	Bits	Default	Range	Description
TDQSCK_MAX_F1	27:24	0x0	0x0-0xf	Additional delay needed for
TDQSCK_MIN_F0	17:16	0x0	0x0-0x3	Additional delay needed for
TDQSCK_MAX_F0	11:8	0x0	0x0-0xf	Additional delay needed for
W2W_SAMECS_DLY	4:0	0x00	0x0-0x1f	Additional delay to insert between two writes to the same chip select.

DENALI_CTL_222 (Address 0xde)

31 27	26 24	23 18	17 16	15 12	11 8	7 2	1 0
RESV	SW_LEVELIN	RESV	TDQSCK_MIN_F2	RESV	TDQSCK_MAX_F2	RESV	TDQSCK_MIN_F1

Name	Bits	Default	Range	Description
SW_LEVELING_MODE	26:24	0x0	0x0-0x7	Defines the leveling operation for software leveling. Clear to 0 for none, program to 1 for write
TDQSCK_MIN_F2	17:16	0x0	0x0-0x3	Additional delay needed for
TDQSCK_MAX_F2	11:8	0x0	0x0-0xf	Additional delay needed for
TDQSCK_MIN_F1	1:0	0x0	0x0-0x3	Additional delay needed for

DENALI_CTL_223 (Address 0xdf)

31 25	24 24	23 17	16 16	15 9	8 8	7 1	0 0
RESV	SWLVL_OP_D	RESV	SWLVL_EXIT	RESV	SWLVL_STAR	RESV	SWLVL_LOAD

Name	Bits	Default	Range	Description
SWLVL_OP_DONE	24	0x0	0x0-0x1	Signals that software leveling is currently in progress. Value of 1
SWLVL_EXIT	16	0x0	0x0-0x1	User request to exit software leveling. Set to 1 to exit. WRITE-
SWLVL_START	8	0x0	0x0-0x1	User request to initiate software leveling of type in the
SWLVL_LOAD	0	0x0	0x0-0x1	User request to load delays and execute software leveling. Set to 1

DENALI_CTL_224 (Address 0xe0)

31 25	24 24	23 17	16 16	15 9	8 8	7 1	0 0
RESV	SWLVL_RESP	RESV	SWLVL_RESP	RESV	SWLVL_RESP	RESV	SWLVL_RESP

Name	Bits	Default	Range	Description
SWLVL_RESP_3	24	0x0	0x0-0x1	Leveling response for data slice 3.
SWLVL_RESP_2	16	0x0	0x0-0x1	Leveling response for data slice 2.
SWLVL_RESP_1	8	0x0	0x0-0x1	Leveling response for data slice 1.
SWLVL_RESP_0	0	0x0	0x0-0x1	Leveling response for data slice 0.

DENALI_CTL_225 (Address 0xe1)

31 30	29 24	23 17	16 16	15 9	8 8	7 1	0 0
RESV	WLDQSEN	RESV	WRLVL_CS	RESV	WRLVL_REQ	RESV	PHYUPD_APP

Name	Bits	Default	Range	Description
WLDQSEN	29:24	0x00	0x0-0x3f	Delay from issuing MRS to first
WRLVL_CS	16	0x0	0x0-0x1	Specifies the target chip select for the write leveling operation initiated
WRLVL_REQ	8	0x0	0x0-0x1	User request to initiate write leveling. Set to 1 to trigger. WRITE-
PHYUPD_APPEND_EN	0	0x0	0x0-0x1	Specifies if a PHY update will be run prior to completing a training

DENALI_CTL_226 (Address 0xe2)

31 25	24 24	23 17	16 16	15 9	8 8	7 6	5 0
RESV	WRLVL_PERI	RESV	DFI_PHY_WR	RESV	WRLVL_EN	RESV	WLMRD

Name	Bits	Default	Range	Description
WRLVL_PERIODIC	24	0x0	0x0-0x1	Enables the use of the dfi_lvl_periodic signal during write
DFI_PHY_WRLVL_MODE	16	0x0	0x0-0x1	Specifies the PHY support for DFI write leveling. Set to 1 for
WRLVL_EN	8	0x0	0x0-0x1	Enable the MC write leveling
WLMRD	5:0	0x00	0x0-0x3f	Delay from issuing MRS to first

DENALI_CTL_227 (Address 0xe3)

31 25	24 24	23 17	16 16	15 12	11 8	7 1	0 0
RESV	WRLVL_ROTA	RESV	WRLVL_AREF _EN	RESV	WRLVL_RESP _MASK	RESV	WRLVL_ON_S

Name	Bits	Default	Range	Description
WRLVL_ROTATE	24	0x0	0x0-0x1	Enables rotational CS for interval write leveling. Set to 1 for rotating

WRLVL_AREF_EN	16	0x0	0x0-0x1	Enables refreshes and other non-data commands to execute in the
WRLVL_RESP_MASK	11:8	0x0	0x0-0xf	Mask for the dfi_wrlvl_resp signal
WRLVL_ON_SREF_EXIT	0	0x0	0x0-0x1	Enables automatic write leveling on a self-refresh exit. Set to 1 to

DENALI_CTL_228 (Address 0xe4)

31 -	- -	- -	- 16	15 10	9 8	7 2	1 0
WRLVL_NORM_THRESHOL	-	-	-	RESV	WRLVL_ERRO R_STATUS	RESV	WRLVL_CS_MAP

Name	Bits	Default	Range	Description
WRLVL_NORM_THRESHOLD_F0	31:16	0x0000	0x0-0xffff	Write leveling normal threshold number of long counts until the
WRLVL_ERROR_STATUS	9:8	0x0	0x0-0x3	Holds the error associated with the write level error interrupt. Bit (0) set indicates a TDFI_WRLVL_MAX
WRLVL_CS_MAP	1:0	0x0	0x0-0x3	Defines the chip select map for write leveling operations. Bit (0) controls cs0, bit (1) controls cs1,

DENALI_CTL_229 (Address 0xe5)

31 -	- -	- -	- 16	15 -	- -	- -	- 0
WRLVL_TIMEOUT_F0	-	-	-	WRLVL_HIGH_THRESHOLD_F0	-	-	-

Name	Bits	Default	Range	Description
WRLVL_TIMEOUT_F0	31:16	0x0000	0x0-0xffff	Write leveling timeout number of long counts until the timeout is
WRLVL_HIGH_THRESHOLD_F0	15:0	0x0000	0x0-0xffff	Write leveling high threshold number of long counts until the high

DENALI_CTL_230 (Address 0xe6)

31 -	- -	- -	- 16	15 -	- -	- -	- 0
WRLVL_DFI_PROMOTE_TH	-	-	-	WRLVL_SW_PROMOTE_TH	-	-	-

Name	Bits	Default	Range	Description
WRLVL_DFI_PROMOTE_THRESHOLD_F0	31:16	0x0000	0x0-0xffff	Write leveling promotion number of long counts until the high priority
WRLVL_SW_PROMOTE_THRESHOLD_F0	15:0	0x0000	0x0-0xffff	Write leveling promotion number of long counts until the high priority

DENALI_CTL_231 (Address 0xe7)

31 -	- -	- -	- 16	15 -	- -	- -	- 0

WRLVL_HIGH_THRESHOLD_F1	-	-	-	WRLVL_NORM_THRESHOL	-	-	-

Name	Bits	Default	Range	Description
WRLVL_HIGH_THRESHOLD_F1	31:16	0x0000	0x0-0xffff	Write leveling high threshold number of long counts until the high
WRLVL_NORM_THRESHOLD_F1	15:0	0x0000	0x0-0xffff	Write leveling normal threshold number of long counts until the

DENALI_CTL_232 (Address 0xe8)

31 -	-	-	-	-	-	16	15 -	-	-	-	-	-	0

WRLVL_SW_PROMOTE_TH	-	-	-	WRLVL_TIMEOUT_F1	-	-	-

Name	Bits	Default	Range	Description
WRLVL_SW_PROMOTE_THRESHOLD_F1	31:16	0x0000	0x0-0xffff	Write leveling promotion number of long counts until the high priority
WRLVL_TIMEOUT_F1	15:0	0x0000	0x0-0xffff	Write leveling timeout number of long counts until the timeout is

DENALI_CTL_233 (Address 0xe9)

31 -	-	-	-	-	-	16	15 -	-	-	-	-	-	0

WRLVL_NORM_THRESHOL	-	-	-	WRLVL_DFI_PROMOTE_TH	-	-	-

Name	Bits	Default	Range	Description
WRLVL_NORM_THRESHOLD_F2	31:16	0x0000	0x0-0xffff	Write leveling normal threshold number of long counts until the
WRLVL_DFI_PROMOTE_THRESHOLD_F1	15:0	0x0000	0x0-0xffff	Write leveling promotion number of long counts until the high priority

DENALI_CTL_234 (Address 0xea)

31 -	-	-	-	-	-	16	15 -	-	-	-	-	-	0

WRLVL_TIMEOUT_F2	-	-	-	WRLVL_HIGH_THRESHOLD_F2	-	-	-

Name	Bits	Default	Range	Description
WRLVL_TIMEOUT_F2	31:16	0x0000	0x0-0xffff	Write leveling timeout number of long counts until the timeout is
WRLVL_HIGH_THRESHOLD_F2	15:0	0x0000	0x0-0xffff	Write leveling high threshold number of long counts until the high

DENALI_CTL_235 (Address 0xeb)

31 -	-	-	-	-	-	16	15 -	-	-	-	-	-	0

WRLVL_DFI_PROMOTE_TH	-	-	-	WRLVL_SW_PROMOTE_TH	-	-	-

Name	Bits	Default	Range	Description
WRLVL_DFI_PROMOTE_THRESHOLD_F2	31:16	0x0000	0x0-0xffff	Write leveling promotion number of long counts until the high priority
WRLVL_SW_PROMOTE_THRESHOLD_F2	15:0	0x0000	0x0-0xffff	Write leveling promotion number of long counts until the high priority

DENALI_CTL_236 (Address 0xec)

31 28	27 24	23 17	16 16	15 9	8 8	7 1	0 0
RESV	RDLVL_SEQ_	RESV	RDLVL_CS	RESV	RDLVL_GATE_	RESV	RDLVL_REQ

Name	Bits	Default	Range	Description
RDLVL_SEQ_EN	27:24	0x0	0x0-0xf	Specifies the pattern, format and
RDLVL_CS	16	0x0	0x0-0x1	Specifies the target chip select for the data eye training operation initiated through the RDLVL_REQ
RDLVL_GATE_REQ	8	0x0	0x0-0x1	User request to initiate gate training. Set to 1 to trigger. WRITE-
RDLVL_REQ	0	0x0	0x0-0x1	User request to initiate data eye training. Set to 1 to trigger. WRITE-

DENALI_CTL_237 (Address 0xed)

31 25	24 24	23 17	16 16	15 9	8 8	7 4	3 0
RESV	RDLVL_PERIODIC	RESV	DFI_PHY_RDLVL_GATE_MO	RESV	DFI_PHY_RDLVL_MODE	RESV	RDLVL_GATE_SEQ_EN

Name	Bits	Default	Range	Description
RDLVL_PERIODIC	24	0x0	0x0-0x1	Enables the use of the dfi_lvl_periodic signal during data
DFI_PHY_RDLVL_GATE_MODE	16	0x0	0x0-0x1	Specifies the PHY support for DFI gate training. Set to 1 for
DFI_PHY_RDLVL_MODE	8	0x0	0x0-0x1	Specifies the PHY support for DFI data eye training. Set to 1 for
RDLVL_GATE_SEQ_EN	3:0	0x0	0x0-0xf	Specifies the pattern, format and

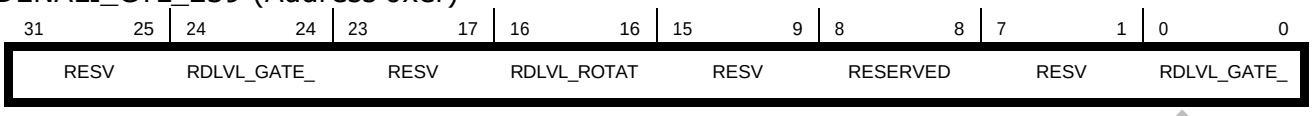
DENALI_CTL_238 (Address 0xee)

31 25	24 24	23 17	16 16	15 9	8 8	7 1	0 0
RESV	RDLVL_AREF_EN	RESV	RDLVL_GATE_ON_SREF_EXI	RESV	RDLVL_GATE_PERIODIC	RESV	RDLVL_ON_SREF_EXIT

Name	Bits	Default	Range	Description
RDLVL_AREF_EN	24	0x0	0x0-0x1	Enables refreshes and other non-data commands to execute in the
RDLVL_GATE_ON_SREF_EXIT	16	0x0	0x0-0x1	Enables automatic gate training on a self-refresh exit. Set to 1 to

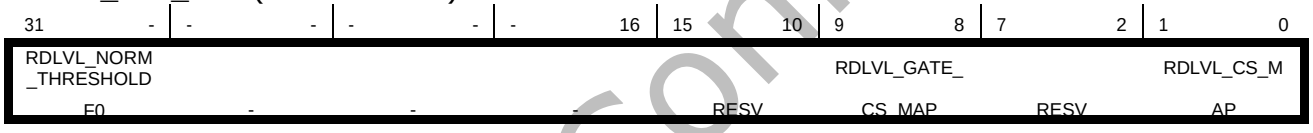
RDLVL_GATE_PERIODIC	8	0x0	0x0-0x1	Enables the use of the dfi_lvl_periodic signal during gate
RDLVL_ON_SREF_EXIT	0	0x0	0x0-0x1	Enables automatic data eye training on a self-refresh exit. Set to

DENALI_CTL_239 (Address 0xef)



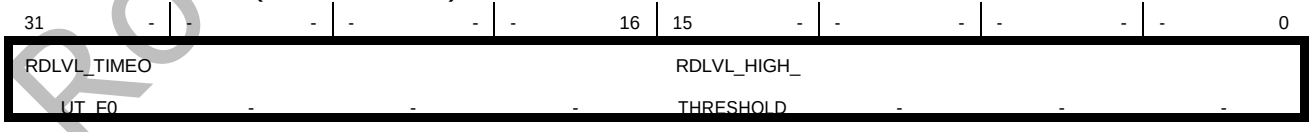
Name	Bits	Default	Range	Description
RDLVL_GATE_ROTATE	24	0x0	0x0-0x1	Enables rotational CS for interval gate training. Set to 1 for rotating
RDLVL_ROTATE	16	0x0	0x0-0x1	Enables rotational CS for interval data eye training. Set to 1 for
RESERVED	8	0x0	0x0-0x1	Reserved for future use. Refer to the regconfig files for the default
RDLVL_GATE_AREF_EN	0	0x0	0x0-0x1	Enables refreshes and other non-data commands to execute in the

DENALI_CTL_240 (Address 0xf0)



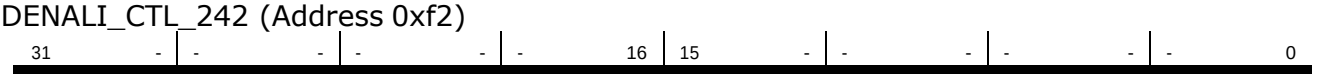
Name	Bits	Default	Range	Description
RDLVL_NORM_THRESHOLD_F0	31:16	0x0000	0x0-0xffff	Read leveling normal threshold number of long counts until the
RDLVL_GATE_CS_MAP	9:8	0x0	0x0-0x3	Defines the chip select map for gate training operations. Bit (0) controls cs0, bit (1) controls cs1,
RDLVL_CS_MAP	1:0	0x0	0x0-0x3	Defines the chip select map for data eye training operations. Bit (0) controls cs0, bit (1) controls cs1,

DENALI_CTL_241 (Address 0xf1)



Name	Bits	Default	Range	Description
RDLVL_TIMEOUT_F0	31:16	0x0000	0x0-0xffff	Read leveling timeout number of long counts until the timeout is
RDLVL_HIGH_THRESHOLD_F0	15:0	0x0000	0x0-0xffff	Read leveling high threshold number of long counts until the high

DENALI_CTL_242 (Address 0xf2)



RDLVL_DFI_P ROMOTE_TH	-	-	-	RDLVL_SW_P ROMOTE_TH	-	-	-

Name	Bits	Default	Range	Description
RDLVL_DFI_PROMOTE_THRESHOLD_F0	31:16	0x0000	0x0-0xffff	Read leveling promotion number of long counts until the high priority
RDLVL_SW_PROMOTE_THRESHOLD_F0	15:0	0x0000	0x0-0xffff	Read leveling promotion number of long counts until the high priority

DENALI_CTL_243 (Address 0xf3)

31	-	-	-	-	-	16	15	-	-	-	-	-	0

RDLVL_GATE_ HIGH_THRES	-	-	-	RDLVL_GATE_ NORM_THRE	-	-	-

Name	Bits	Default	Range	Description
RDLVL_GATE_HIGH_THRESHOLD_F0	31:16	0x0000	0x0-0xffff	Gate training high threshold number of long counts until the high
RDLVL_GATE_NORM_THRESHOLD_F0	15:0	0x0000	0x0-0xffff	Gate training normal threshold number of long counts until the

DENALI_CTL_244 (Address 0xf4)

31	-	-	-	-	-	16	15	-	-	-	-	-	0

RDLVL_GATE_ SW_PROMOT	-	-	-	RDLVL_GATE_	-	-	-

Name	Bits	Default	Range	Description
RDLVL_GATE_SW_PROMOTE_THRESHO	31:16	0x0000	0x0-0xffff	Gate training promotion number of long counts until the high priority
RDLVL_GATE_TIMEOUT_F0	15:0	0x0000	0x0-0xffff	Gate training timeout number of long counts until the timeout is

DENALI_CTL_245 (Address 0xf5)

31	-	-	-	-	-	16	15	-	-	-	-	-	0

RDLVL_NORM _THRESHOLD _F1	-	-	-	RDLVL_GATE_ DFI_PROMOT	-	-	-

Name	Bits	Default	Range	Description
RDLVL_NORM_THRESHOLD_F1	31:16	0x0000	0x0-0xffff	Read leveling normal threshold number of long counts until the
RDLVL_GATE_DFI_PROMOTE_THRESHO	15:0	0x0000	0x0-0xffff	Gate training promotion number of long counts until the high priority

DENALI_CTL_246 (Address 0xf6)

31	-	-	-	-	-	16	15	-	-	-	-	-	0

RDLVL_TIMEOUT_F1	-	-	-	RDLVL_HIGH_THRESHOLD	-	-	-

Name	Bits	Default	Range	Description
RDLVL_TIMEOUT_F1	31:16	0x0000	0x0-0xffff	Read leveling timeout number of long counts until the timeout is
RDLVL_HIGH_THRESHOLD_F1	15:0	0x0000	0x0-0xffff	Read leveling high threshold number of long counts until the high

DENALI_CTL_247 (Address 0xf7)

31	-	-	-	-	-	-	16	15	-	-	-	-	-	0

RDLVL_DFI_PROMOTE_TH	-	-	-	RDLVL_SW_PROMOTE_TH	-	-	-

Name	Bits	Default	Range	Description
RDLVL_DFI_PROMOTE_THRESHOLD_F1	31:16	0x0000	0x0-0xffff	Read leveling promotion number of long counts until the high priority
RDLVL_SW_PROMOTE_THRESHOLD_F1	15:0	0x0000	0x0-0xffff	Read leveling promotion number of long counts until the high priority

DENALI_CTL_248 (Address 0xf8)

31	-	-	-	-	-	-	16	15	-	-	-	-	-	0

RDLVL_GATE_HIGH_THRES	-	-	-	RDLVL_GATE_NORM_THRE	-	-	-

Name	Bits	Default	Range	Description
RDLVL_GATE_HIGH_THRESHOLD_F1	31:16	0x0000	0x0-0xffff	Gate training high threshold number of long counts until the high
RDLVL_GATE_NORM_THRESHOLD_F1	15:0	0x0000	0x0-0xffff	Gate training normal threshold number of long counts until the

DENALI_CTL_249 (Address 0xf9)

31	-	-	-	-	-	-	16	15	-	-	-	-	-	0

RDLVL_GATE_SW_PROMOT	-	-	-	RDLVL_GATE_	-	-	-

Name	Bits	Default	Range	Description
RDLVL_GATE_SW_PROMOTE_THRESHO	31:16	0x0000	0x0-0xffff	Gate training promotion number of long counts until the high priority
RDLVL_GATE_TIMEOUT_F1	15:0	0x0000	0x0-0xffff	Gate training timeout number of long counts until the timeout is

DENALI_CTL_250 (Address 0xfa)

31	-	-	-	-	-	-	16	15	-	-	-	-	-	0

RDLVL_NORM _THRESHOLD _F2	-	-	-	RDLVL_GATE_ DFI_PROMOT	-	-	-

Name	Bits	Default	Range	Description
RDLVL_NORM_THRESHOLD_F2	31:16	0x0000	0x0-0xffff	Read leveling normal threshold number of long counts until the
RDLVL_GATE_DFI_PROMOTE_THRESHO	15:0	0x0000	0x0-0xffff	Gate training promotion number of long counts until the high priority

DENALI_CTL_251 (Address 0xfb)

31 -	-	-	-	-	-	16	15 -	-	-	-	-	-	0

RDLVL_TIMEO UT_F2	-	-	-	RDLVL_HIGH_ THRESHOLD	-	-	-

Name	Bits	Default	Range	Description
RDLVL_TIMEOUT_F2	31:16	0x0000	0x0-0xffff	Read leveling timeout number of long counts until the timeout is
RDLVL_HIGH_THRESHOLD_F2	15:0	0x0000	0x0-0xffff	Read leveling high threshold number of long counts until the high

DENALI_CTL_252 (Address 0xfc)

31 -	-	-	-	-	-	16	15 -	-	-	-	-	-	0

RDLVL_DFI_P ROMOTE_TH	-	-	-	RDLVL_SW_P ROMOTE_TH	-	-	-

Name	Bits	Default	Range	Description
RDLVL_DFI_PROMOTE_THRESHOLD_F2	31:16	0x0000	0x0-0xffff	Read leveling promotion number of long counts until the high priority
RDLVL_SW_PROMOTE_THRESHOLD_F2	15:0	0x0000	0x0-0xffff	Read leveling promotion number of long counts until the high priority

DENALI_CTL_253 (Address 0xfd)

31 -	-	-	-	-	-	16	15 -	-	-	-	-	-	0

RDLVL_GATE_ HIGH_THRES	-	-	-	RDLVL_GATE_ NORM_THRE	-	-	-

Name	Bits	Default	Range	Description
RDLVL_GATE_HIGH_THRESHOLD_F2	31:16	0x0000	0x0-0xffff	Gate training high threshold number of long counts until the high
RDLVL_GATE_NORM_THRESHOLD_F2	15:0	0x0000	0x0-0xffff	Gate training normal threshold number of long counts until the

DENALI_CTL_254 (Address 0xfe)

31 -	-	-	-	-	-	16	15 -	-	-	-	-	-	0

RDLVL_GATE_ SW_PROMOT	-	-	-	RDLVL_GATE_	-	-	-

Name	Bits	Default	Range	Description
RDLVL_GATE_SW_PROMOTE_THRESHO	31:16	0x0000	0x0-0xffff	Gate training promotion number of long counts until the high priority
RDLVL_GATE_TIMEOUT_F2	15:0	0x0000	0x0-0xffff	Gate training timeout number of long counts until the timeout is

DENALI_CTL_255 (Address 0xff)

31 25	24 24	23 17	16 16	15 -	- -	- -	- 0
RESV	CALVL_CS	RESV	CALVL_REQ	RDLVL_GATE_ DFI_PROMOT	-	-	-

Name	Bits	Default	Range	Description
CALVL_CS	24	0x0	0x0-0x1	Specifies the target chip select for the CA training operation initiated
CALVL_REQ	16	0x0	0x0-0x1	User request to initiate CA training.
RDLVL_GATE_DFI_PROMOTE_THRESHO	15:0	0x0000	0x0-0xffff	Gate training promotion number of long counts until the high priority

DENALI_CTL_256 (Address 0x100)

31 -	- 24	23 20	19 -	- -	- -	- -	- 0
OBSOLETE	-	RESV	CALVL_PAT_0	-	-	-	-

Name	Bits	Default	Range	Description
CALVL_PAT_0	19:0	0x00000	0x0-0xfffff	CA Training pattern 0 driven on the CA bus during a calibration

DENALI_CTL_257 (Address 0x101)

31 -	- 24	23 20	19 -	- -	- -	- -	- 0
OBSOLETE	-	RESV	CALVL_BG_PA	-	-	-	-

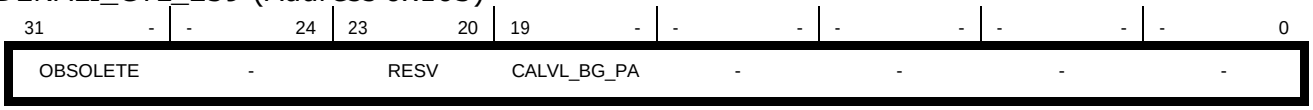
Name	Bits	Default	Range	Description
CALVL_BG_PAT_0	19:0	0x00000	0x0-0xfffff	CA Training pattern 0 driven on the CA bus before and after a

DENALI_CTL_258 (Address 0x102)

31 -	- 24	23 20	19 -	- -	- -	- -	- 0
OBSOLETE	-	RESV	CALVL_PAT_1	-	-	-	-

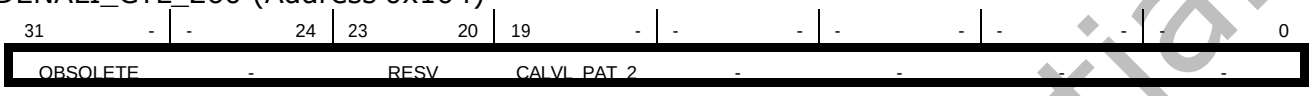
Name	Bits	Default	Range	Description
CALVL_PAT_1	19:0	0x00000	0x0-0xfffff	CA Training pattern 1 driven on the CA bus during a calibration

DENALI_CTL_259 (Address 0x103)



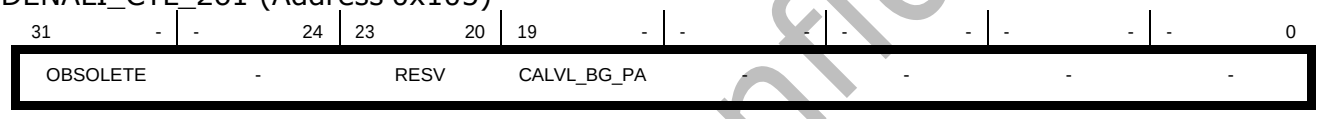
Name	Bits	Default	Range	Description
CALVL_BG_PAT_1	19:0	0x00000	0x0-0xfffff	CA Training pattern 1 driven on the CA bus before and after a

DENALI_CTL_260 (Address 0x104)



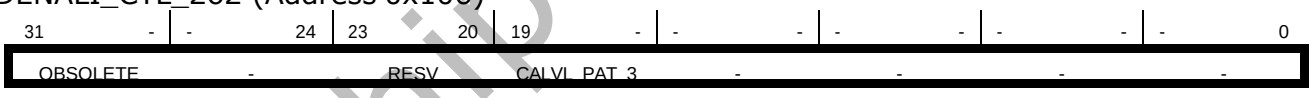
Name	Bits	Default	Range	Description
CALVL_PAT_2	19:0	0x00000	0x0-0xfffff	CA Training pattern 2 driven on the CA bus during a calibration

DENALI_CTL_261 (Address 0x105)



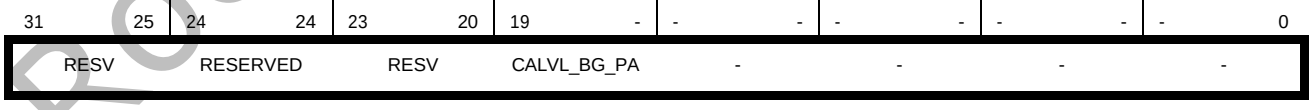
Name	Bits	Default	Range	Description
CALVL_BG_PAT_2	19:0	0x00000	0x0-0xfffff	CA Training pattern 2 driven on the CA bus before and after a

DENALI_CTL_262 (Address 0x106)



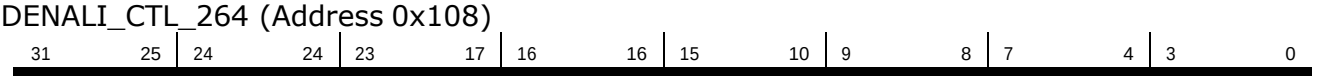
Name	Bits	Default	Range	Description
CALVL_PAT_3	19:0	0x00000	0x0-0xfffff	CA Training pattern 3 driven on the CA bus during a calibration

DENALI_CTL_263 (Address 0x107)



Name	Bits	Default	Range	Description
RESERVED	24	0x0	0x0-0x1	Reserved for future use. Refer to the regconfig files for the default
CALVL_BG_PAT_3	19:0	0x00000	0x0-0xfffff	CA Training pattern 3 driven on the CA bus before and after a

DENALI_CTL_264 (Address 0x108)



RESV	CALVL_PERIO	RESV	DFI_PHY_CAL	RESV	CALVL_SEQ_	RESV	RESERVED

Name	Bits	Default	Range	Description
CALVL_PERIODIC	24	0x0	0x0-0x1	Enables the use of the dfi_lvl_periodic signal during CA
DFI_PHY_CALVL_MODE	16	0x0	0x0-0x1	Specifies the PHY support for DFI
CALVL_SEQ_EN	9:8	0x0	0x0-0x3	Specifies which CA training patterns will be used. Clear to 0 for pattern 0 only, program to 1 for
RESERVED	3:0	0x0	0x0-0xf	Reserved for future use. Refer to the regconfig files for the default

DENALI_CTL_265 (Address 0x109)

31 26	25 24	23 17	16 16	15 9	8 8	7 1	0 0
RESV	CALVL_CS_M	RESV	CALVL_ROTAT	RESV	CALVL_AREF_	RESV	CALVL_ON_S

Name	Bits	Default	Range	Description
CALVL_CS_MAP	25:24	0x0	0x0-0x3	Defines the chip select map for CA training operations. Bit (0) controls cs0, bit (1) controls cs1, etc. Set
CALVL_ROTATE	16	0x0	0x0-0x1	Enables rotational CS for interval CA training. Set to 1 for rotating
CALVL_AREF_EN	8	0x0	0x0-0x1	Enables refreshes and other non-data commands to execute in the
CALVL_ON_SREF_EXIT	0	0x0	0x0-0x1	Enables automatic CA training on a

DENALI_CTL_266 (Address 0x10a)

31 -	- -	- -	- 16	15 -	- -	- -	- 0
CALVL_HIGH_THRESHOLD	-	-	-	CALVL_NORM_THRESHOLD	-	-	-

Name	Bits	Default	Range	Description
CALVL_HIGH_THRESHOLD_F0	31:16	0x0000	0x0-0xffff	CA training high threshold number of long counts until the high priority
CALVL_NORM_THRESHOLD_F0	15:0	0x0000	0x0-0xffff	CA training normal threshold number of long counts until the

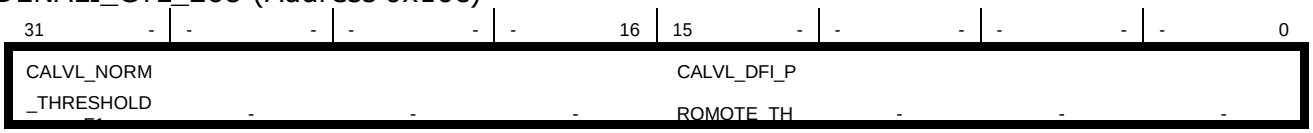
DENALI_CTL_267 (Address 0x10b)

31 -	- -	- -	- 16	15 -	- -	- -	- 0
CALVL_SW_PROMOTE_TH	-	-	-	CALVL_TIMEOUT_F0	-	-	-

Name	Bits	Default	Range	Description
CALVL_SW_PROMOTE_THRESHOLD_F0	31:16	0x0000	0x0-0xffff	CA training promotion number of long counts until the high priority

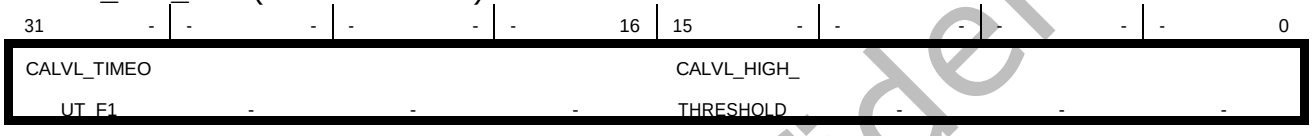
CALVL_TIMEOUT_F0	15:0	0x0000	0x0-0xffff	CA training timeout number of long

DENALI_CTL_268 (Address 0x10c)



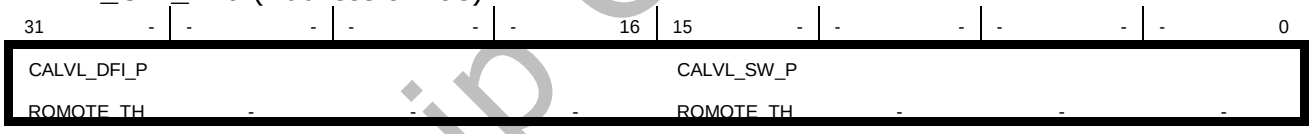
Name	Bits	Default	Range	Description
CALVL_NORM_THRESHOLD_F1	31:16	0x0000	0x0-0xffff	CA training normal threshold number of long counts until the
CALVL_DFI_PROMOTE_THRESHOLD_F0	15:0	0x0000	0x0-0xffff	CA training promotion number of long counts until the high priority

DENALI_CTL_269 (Address 0x10d)



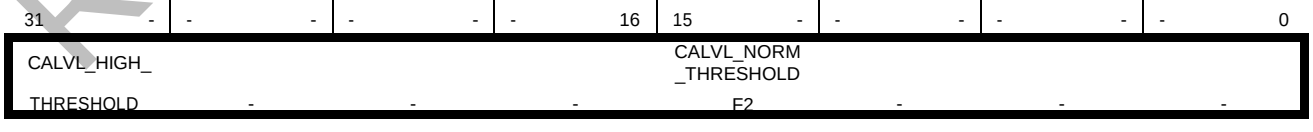
Name	Bits	Default	Range	Description
CALVL_TIMEOUT_F1	31:16	0x0000	0x0-0xffff	CA training timeout number of long
CALVL_HIGH_THRESHOLD_F1	15:0	0x0000	0x0-0xffff	CA training high threshold number of long counts until the high priority

DENALI_CTL_270 (Address 0x10e)



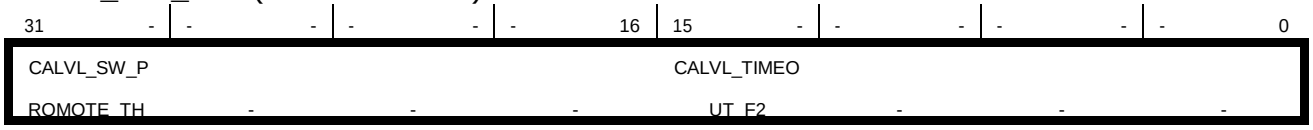
Name	Bits	Default	Range	Description
CALVL_DFI_PROMOTE_THRESHOLD_F1	31:16	0x0000	0x0-0xffff	CA training promotion number of long counts until the high priority
CALVL_SW_PROMOTE_THRESHOLD_F1	15:0	0x0000	0x0-0xffff	CA training promotion number of long counts until the high priority

DENALI_CTL_271 (Address 0x10f)



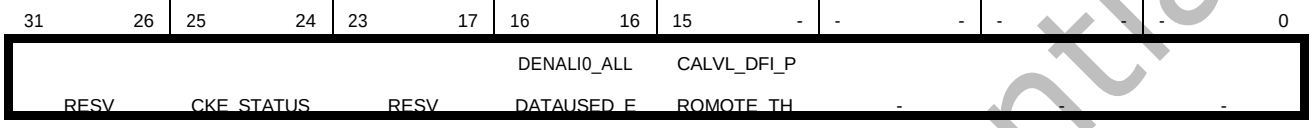
Name	Bits	Default	Range	Description
CALVL_HIGH_THRESHOLD_F2	31:16	0x0000	0x0-0xffff	CA training high threshold number of long counts until the high priority
CALVL_NORM_THRESHOLD_F2	15:0	0x0000	0x0-0xffff	CA training normal threshold number of long counts until the

DENALI_CTL_272 (Address 0x110)



Name	Bits	Default	Range	Description
CALVL_SW_PROMOTE_THRESHOLD_F2	31:16	0x0000	0x0-0xffff	CA training promotion number of long counts until the high priority
CALVL_TIMEOUT_F2	15:0	0x0000	0x0-0xffff	CA training timeout number of long

DENALI_CTL_273 (Address 0x111)

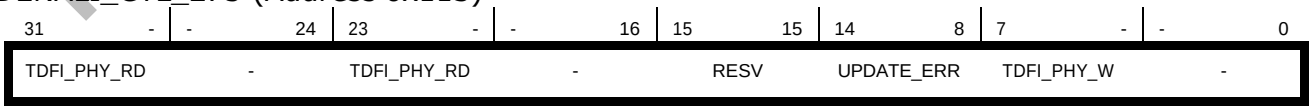


Name	Bits	Default	Range	Description
CKE_STATUS	25:24	0x0	0x0-0x3	Register access to cke_status
DENALI0_ALLDATAUSED_ENABLE	16	0x0	0x0-0x1	Enables use of the ALLDATAUSED signal for DENALI port 0. Set to 1
CALVL_DFI_PROMOTE_THRESHOLD_F2	15:0	0x0000	0x0-0xffff	CA training promotion number of long counts until the high priority

DENALI_CTL_274 (Address 0x112)

Name	Bits	Default	Range	Description
DLL_RST_ADJ_DLY	31:24	0x00	0x0-0xff	Minimum cycles after setting master delay in DLL until the DLL reset signal dll_rst_n may be
DLL_RST_DELAY	23:8	0x0000	0x0-0xffff	Minimum cycles required for DLL reset signal dll_rst_n to be held. If this signal is not being used by the
MEM_RST_VALID	0	0x0	0x0-0x1	Register access to mem_rst_valid

DENALI_CTL_275 (Address 0x113)



Name	Bits	Default	Range	Description
TDFI_PHY_RDLAT_F1	31:24	0x06	0x0-0xff	Defines the DFI tPHY_RDLAT timing parameter (in DFI PHY clocks), the maximum cycles

TDFI_PHY_RDLAT_F0	23:16	0x06	0x0-0xff	Defines the DFI tPHY_RDLAT timing parameter (in DFI PHY clocks), the maximum cycles
UPDATE_ERROR_STATUS	14:8	0x00	0x0-0x7f	Identifies the source of any DFI MC-initiated or PHY-initiated update errors. Value of 1 indicates
TDFI_PHY_WRLAT	7:0	Calc Value	0x0-0xff	Holds the calculated DFI tPHY_WRLAT timing parameter (in DFI PHY clocks), the maximum

DENALI_CTL_276 (Address 0x114)

31 28	27 24	23 18	17 16	15 -	- 8	7 -	- 0
RESV	TDFI_CTRLUP	RESV	DRAM_CLK_D	TDFI_RDDATA _EN	-	TDFI_PHY_RD	-

Name	Bits	Default	Range	Description
TDFI_CTRLUPD_MIN	27:24	0x0	0x0-0xf	Reports the DFI tCTRLUPD_MIN timing parameter (in DFI clocks),
DRAM_CLK_DISABLE	17:16	0x0	0x0-0x3	Set value for the dfi_dram_clk_disable signal. Bit(0)
TDFI_RDDATA_EN	15:8	Calc Value	0x0-0xff	Holds the calculated DFI tRDDATA_EN timing parameter (in DFI PHY clocks), the maximum
TDFI_PHY_RDLAT_F2	7:0	0x06	0x0-0xff	Defines the DFI tPHY_RDLAT timing parameter (in DFI PHY clocks), the maximum cycles

DENALI_CTL_277 (Address 0x115)

31 -	- -	- -	- 16	15 -	- -	- -	- 0
OBSOLETE	-	-	-	TDFI_CTRLUP	-	-	-

Name	Bits	Default	Range	Description
TDFI_CTRLUPD_MAX_F0	15:0	0x0000	0x0-0xffff	Defines the DFI tCTRLUPD_MAX timing parameter (in DFI clocks), the maximum cycles that dfi_ctrlupd_req can be asserted. If programmed to a non-zero, a

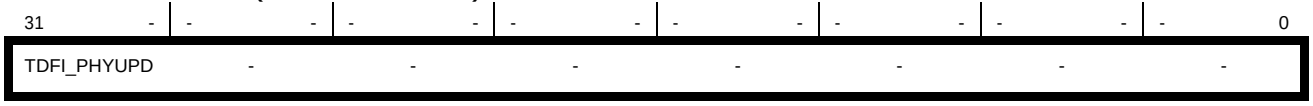
DENALI_CTL_278 (Address 0x116)

31 -	- -	- -	- -	- -	- -	- -	- 0
TDFI_PHYUPD _TYPE0_F0	-	-	-	-	-	-	-

Name	Bits	Default	Range	Description
				Defines the DFI tPHYUPD_TYPE0 timing parameter (in DFI clocks), the maximum cycles that dfi_phyupd_req can assert after

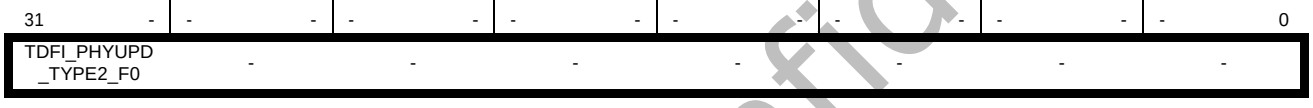
TDFI_PHYUPD_TYPE0_F0	31:0	0x00000000	0x0-0xffffffff	dfi_phyupd_ack for to a non-zero, a timing violation will cause an interrupt and bit (2) set in the UPDATE_ERROR_STATUS parameter.

DENALI_CTL_279 (Address 0x117)



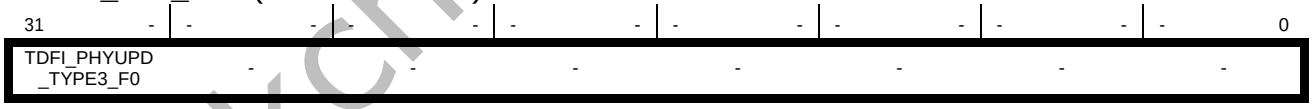
Name	Bits	Default	Range	Description
TDFI_PHYUPD_TYPE1_F0	31:0	0x00000000	0x0-0xffffffff	Defines the DFI tPHYUPD_TYPE1 timing parameter (in DFI clocks), the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for to a non-zero, a timing violation will cause an interrupt and bit (3) set in the UPDATE_ERROR_STATUS parameter.

DENALI_CTL_280 (Address 0x118)



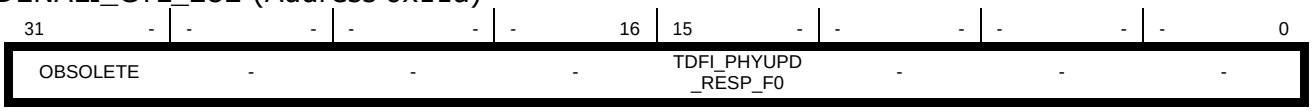
Name	Bits	Default	Range	Description
TDFI_PHYUPD_TYPE2_F0	31:0	0x00000000	0x0-0xffffffff	Defines the DFI tPHYUPD_TYPE2 timing parameter (in DFI clocks), the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for to a non-zero, a timing violation will cause an interrupt and bit (4) set in the UPDATE_ERROR_STATUS parameter.

DENALI_CTL_281 (Address 0x119)



Name	Bits	Default	Range	Description
TDFI_PHYUPD_TYPE3_F0	31:0	0x00000000	0x0-0xffffffff	Defines the DFI tPHYUPD_TYPE3 timing parameter (in DFI clocks), the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for to a non-zero, a timing violation will cause an interrupt and bit (5) set in the UPDATE_ERROR_STATUS parameter.

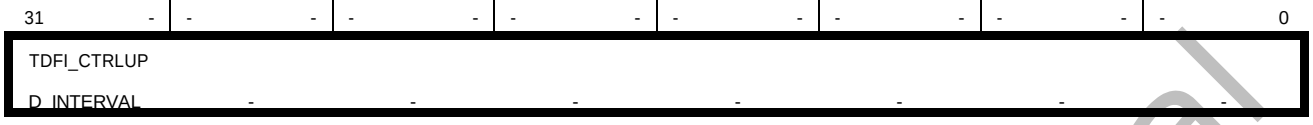
DENALI_CTL_282 (Address 0x11a)



Name	Bits	Default	Range	Description

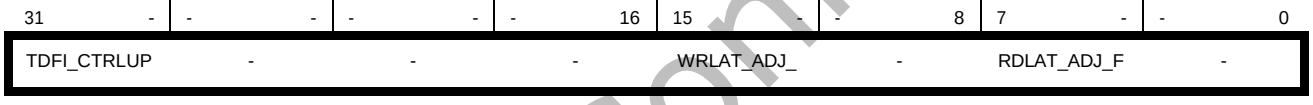
TDFI_PHYUPD_RESP_F0	15:0	0x0000	0x0-0xffff	Defines the DFI tPHYUPD_RESP timing parameter (in DFI clocks), the maximum cycles between a dfi_phyupd_req assertion and a dfi_phyupd_ack assertion. If

DENALI_CTL_283 (Address 0x11b)



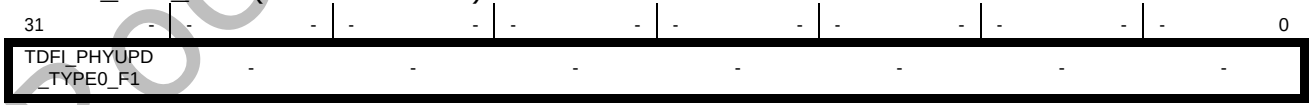
Name	Bits	Default	Range	Description
TDFI_CTRLUPD_INTERVAL_F0	31:0	0x00000000	0x0-0xffffffff	Defines the DFI tCTRLUPD_INTERVAL timing parameter (in DFI clocks), the maximum cycles between dfi_ctrlupd_req assertions. If timing violation will cause an interrupt and bit (0) set in the UPDATE_ERROR_STATUS parameter.

DENALI_CTL_284 (Address 0x11c)



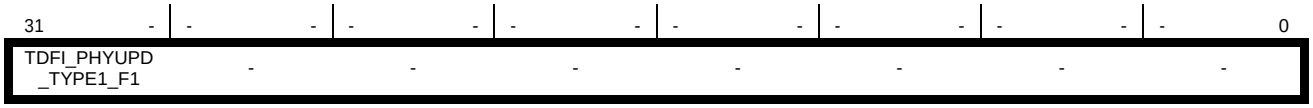
Name	Bits	Default	Range	Description
TDFI_CTRLUPD_MAX_F1	31:16	0x0000	0x0-0xffff	Defines the DFI tCTRLUPD_MAX timing parameter (in DFI clocks), the maximum cycles that dfi_ctrlupd_req can be asserted. If programmed to a non-zero, a
WRLAT_ADJ_F0	15:8	0x00	0x0-0xff	Adjustment value for PHY write
RDLAT_ADJ_F0	7:0	0x00	0x0-0xff	Adjustment value for PHY read

DENALI_CTL_285 (Address 0x11d)



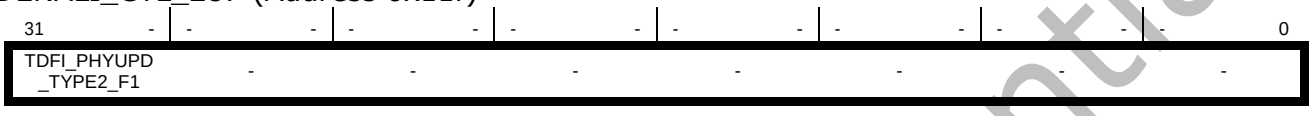
Name	Bits	Default	Range	Description
TDFI_PHYUPD_TYPE0_F1	31:0	0x00000000	0x0-0xffffffff	Defines the DFI tPHYUPD_TYPE0 timing parameter (in DFI clocks), the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for to a non-zero, a timing violation will cause an interrupt and bit (2) set in the UPDATE_ERROR_STATUS parameter.

DENALI_CTL_286 (Address 0x11e)



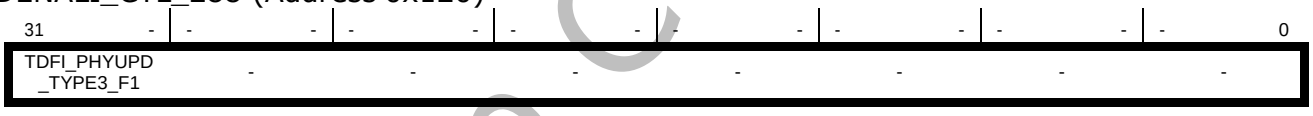
Name	Bits	Default	Range	Description
TDFI_PHYUPD_TYPE1_F1	31:0	0x000000 00	0x0-0xffffffff	Defines the DFI tPHYUPD_TYPE1 timing parameter (in DFI clocks), the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for to a non-zero, a timing violation will cause an interrupt and bit (3) set in the UPDATE_ERROR_STATUS parameter.

DENALI_CTL_287 (Address 0x11f)



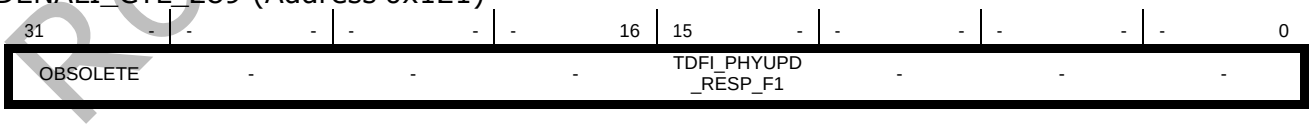
Name	Bits	Default	Range	Description
TDFI_PHYUPD_TYPE2_F1	31:0	0x000000 00	0x0-0xffffffff	Defines the DFI tPHYUPD_TYPE2 timing parameter (in DFI clocks), the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for to a non-zero, a timing violation will cause an interrupt and bit (4) set in the UPDATE_ERROR_STATUS parameter.

DENALI_CTL_288 (Address 0x120)



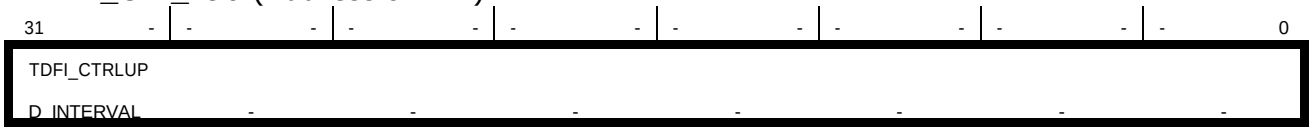
Name	Bits	Default	Range	Description
TDFI_PHYUPD_TYPE3_F1	31:0	0x000000 00	0x0-0xffffffff	Defines the DFI tPHYUPD_TYPE3 timing parameter (in DFI clocks), the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for to a non-zero, a timing violation will cause an interrupt and bit (5) set in the UPDATE_ERROR_STATUS parameter.

DENALI_CTL_289 (Address 0x121)



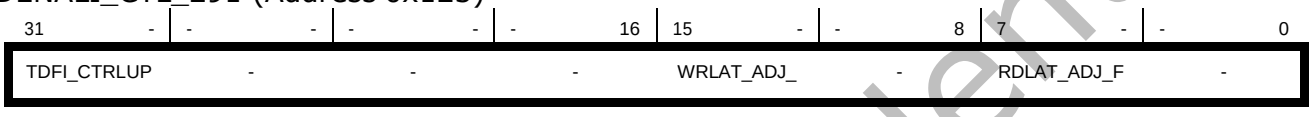
Name	Bits	Default	Range	Description
TDFI_PHYUPD_RESP_F1	15:0	0x0000	0x0-0xffff	Defines the DFI tPHYUPD_RESP timing parameter (in DFI clocks), the maximum cycles between a dfi_phyupd_req assertion and a dfi_phyupd_ack assertion. If

DENALI_CTL_290 (Address 0x122)



Name	Bits	Default	Range	Description
TDFI_CTRLUPD_INTERVAL_F1	31:0	0x00000000	0x0-0xffffffff	Defines the DFI tCTRLUPD_INTERVAL timing parameter (in DFI clocks), the maximum cycles between dfi_ctrlupd_req assertions. If timing violation will cause an interrupt and bit (0) set in the UPDATE_ERROR_STATUS parameter.

DENALI_CTL_291 (Address 0x123)

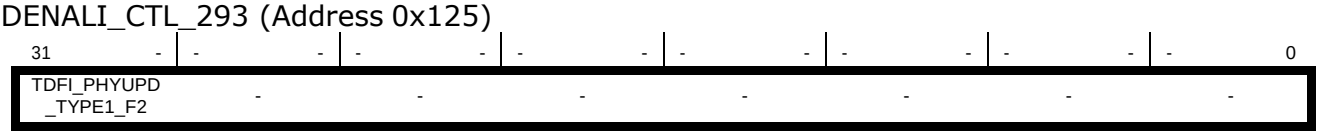


Name	Bits	Default	Range	Description
TDFI_CTRLUPD_MAX_F2	31:16	0x0000	0x0-0xffff	Defines the DFI tCTRLUPD_MAX timing parameter (in DFI clocks), the maximum cycles that dfi_ctrlupd_req can be asserted. If programmed to a non-zero, a
WRLAT_ADJ_F1	15:8	0x00	0x0-0xff	Adjustment value for PHY write
RDLAT_ADJ_F1	7:0	0x00	0x0-0xff	Adjustment value for PHY read

DENALI_CTL_292 (Address 0x124)

Name	Bits	Default	Range	Description
TDFI_PHYUPD_TYPE0_F2	31:0	0x00000000	0x0-0xffffffff	Defines the DFI tPHYUPD_TYPE0 timing parameter (in DFI clocks), the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for to a non-zero, a timing violation will cause an interrupt and bit (2) set in the UPDATE_ERROR_STATUS parameter.

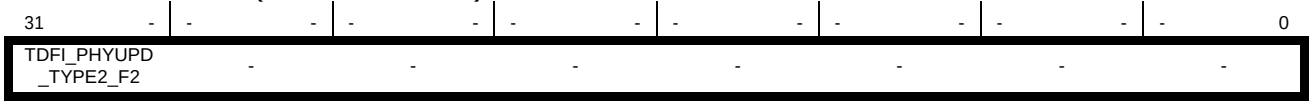
DENALI_CTL_293 (Address 0x125)



Name	Bits	Default	Range	Description
				Defines the DFI tPHYUPD_TYPE1 timing parameter (in DFI clocks), the maximum cycles that dfi_phyupd_req can assert after

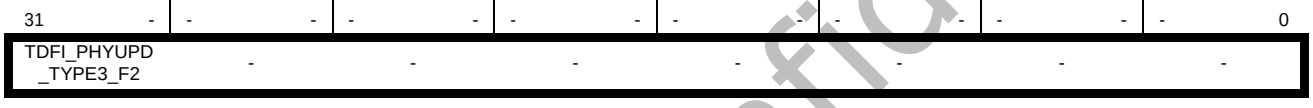
TDFI_PHYUPD_TYPE1_F2	31:0	0x000000 00	0x0-0xffffffff	dfi_phyupd_ack for to a non-zero, a timing violation will cause an interrupt and bit (3) set in the UPDATE_ERROR_STATUS parameter.

DENALI_CTL_294 (Address 0x126)



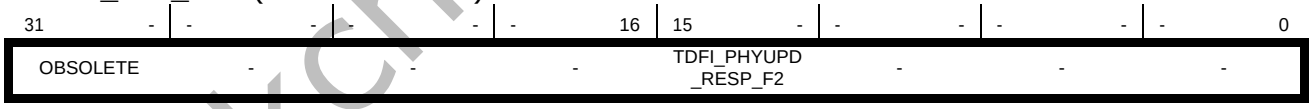
Name	Bits	Default	Range	Description
TDFI_PHYUPD_TYPE2_F2	31:0	0x000000 00	0x0-0xffffffff	Defines the DFI tPHYUPD_TYPE2 timing parameter (in DFI clocks), the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for to a non-zero, a timing violation will cause an interrupt and bit (4) set in the UPDATE_ERROR_STATUS parameter.

DENALI_CTL_295 (Address 0x127)



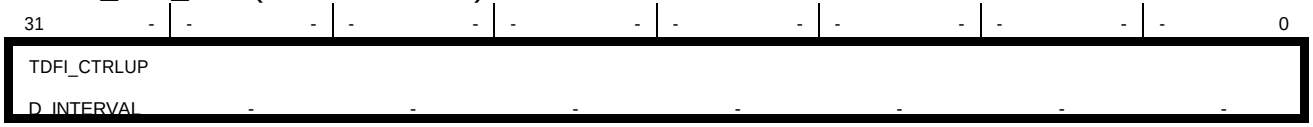
Name	Bits	Default	Range	Description
TDFI_PHYUPD_TYPE3_F2	31:0	0x000000 00	0x0-0xffffffff	Defines the DFI tPHYUPD_TYPE3 timing parameter (in DFI clocks), the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for to a non-zero, a timing violation will cause an interrupt and bit (5) set in the UPDATE_ERROR_STATUS parameter.

DENALI_CTL_296 (Address 0x128)



Name	Bits	Default	Range	Description
TDFI_PHYUPD_RESP_F2	15:0	0x0000	0x0-0xffff	Defines the DFI tPHYUPD_RESP timing parameter (in DFI clocks), the maximum cycles between a dfi_phyupd_req assertion and a dfi_phyupd_ack assertion. If

DENALI_CTL_297 (Address 0x129)



Name	Bits	Default	Range	Description
				Defines the DFI

TDFI_CTRLUPD_INTERVAL_F2	31:0	0x000000 00	0x0-0xffffffff	tCTRLUPD_INTERVAL timing parameter (in DFI clocks), the maximum cycles between dfi_ctrlupd_req assertions. If timing violation will cause an interrupt and bit (0) set in the UPDATE_ERROR_STATUS parameter.

DENALI_CTL_298 (Address 0x12a)

31 28	27 24	23 20	19 16	15 -	- 8	7 -	- 0
RESV	TDFI_CTRL_D	RESV	TDFI_CTRL_D	WRLAT_ADJ_	-	RDLAT_ADJ_F	-

Name	Bits	Default	Range	Description
TDFI_CTRL_DELAY_F1	27:24	0x2	0x0-0xf	Defines the DFI tCTRL_DELAY timing parameter (in DFI clocks),
TDFI_CTRL_DELAY_F0	19:16	0x2	0x0-0xf	Defines the DFI tCTRL_DELAY timing parameter (in DFI clocks),
WRLAT_ADJ_F2	15:8	0x00	0x0-0xff	Adjustment value for PHY write
RDLAT_ADJ_F2	7:0	0x00	0x0-0xff	Adjustment value for PHY read

DENALI_CTL_299 (Address 0x12b)

31 -	- 24	23 20	19 16	15 12	11 8	7 4	3 0
TDFI_WRLVL_	-	RESV	TDFI_DRAM_	RESV	TDFI_DRAM_	RESV	TDFI_CTRL_D

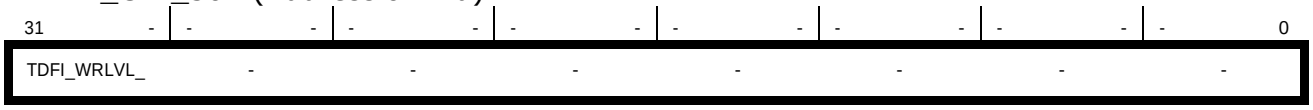
Name	Bits	Default	Range	Description
TDFI_WRLVL_EN	31:24	0x00	0x0-0xff	Defines the DFI tWRLVL_EN timing parameter (in DFI clocks), the minimum cycles from a
TDFI_DRAM_CLK_ENABLE	19:16	0x0	0x0-0xf	Defines the DFI tDRAM_CLK_ENABLE timing parameter (in DFI clocks), the
TDFI_DRAM_CLK_DISABLE	11:8	0x0	0x0-0xf	Defines the DFI tDRAM_CLK_DISABLE timing parameter (in DFI clocks), the
TDFI_CTRL_DELAY_F2	3:0	0x2	0x0-0xf	Defines the DFI tCTRL_DELAY timing parameter (in DFI clocks),

DENALI_CTL_300 (Address 0x12c)

31 -	- -	- -	- 16	15 10	9 -	- -	- 0
OBSOLETE	-	-	-	RESV	TDFI_WRLVL_	-	-

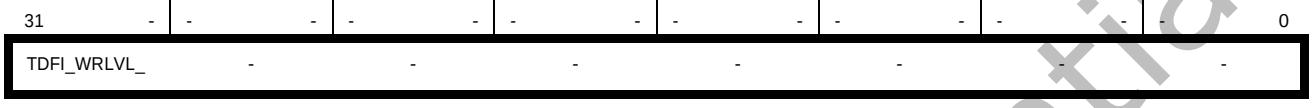
Name	Bits	Default	Range	Description
TDFI_WRLVL_WW	9:0	0x000	0x0-0x3ff	Defines the DFI tWRLVL_WW timing parameter (in DFI clocks),

DENALI_CTL_301 (Address 0x12d)



Name	Bits	Default	Range	Description
TDFI_WRLVL_RESP	31:0	0x00000000	0x0-0xffffffff	Defines the DFI tWRLVL_RESP timing parameter (in DFI clocks), the maximum cycles between a dfi_wrlvl_en assertion.

DENALI_CTL_302 (Address 0x12e)



Name	Bits	Default	Range	Description
TDFI_WRLVL_MAX	31:0	0x00000000	0x0-0xffffffff	Defines the DFI tWRLVL_MAX timing parameter (in DFI clocks), the maximum cycles between a dfi_wrlvl_resp.

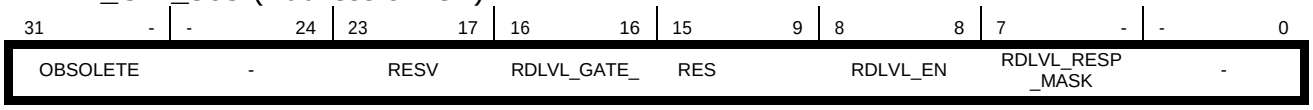
DENALI_CTL_303 (Address 0x12f)

Name	Bits	Default	Range	Description
TDFI_RDLVL_RR	17:8	0x000	0x0-0x3ff	Defines the DFI tRDLVL_RR timing parameter (in DFI clocks), the
TDFI_RDLVL_EN	7:0	0x00	0x0-0xff	Defines the DFI tRDLVL_EN timing parameter (in DFI clocks), the minimum cycles from a dfi_rdlvl_en

DENALI_CTL_304 (Address 0x130)

Name	Bits	Default	Range	Description
TDFI_RDLVL_RESP	31:0	0x00000000	0x0-0xffffffff	Defines the DFI tRDLVL_RESP timing parameter (in DFI clocks), the maximum cycles between a assertion and a dfi_rdlvl_en or dfi_rdlvl_gate_en assertion.

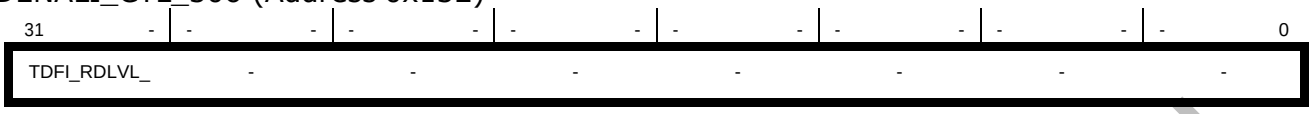
DENALI_CTL_305 (Address 0x131)



Name	Bits	Default	Range	Description

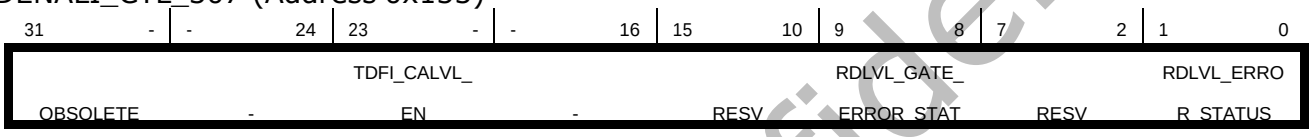
RDLVL_GATE_EN	16	0x0	0x0-0x1	Enable the MC gate training
RDLVL_EN	8	0x0	0x0-0x1	Enable the MC data eye training
RDLVL_RESP_MASK	7:0	0x00	0x0-0xff	Mask for the dfi_rdlvl_resp signal

DENALI_CTL_306 (Address 0x132)



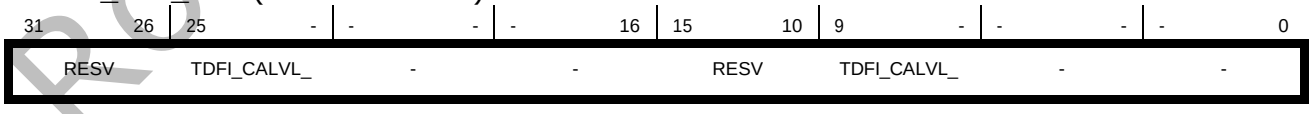
Name	Bits	Default	Range	Description
TDFI_RDLVL_MAX	31:0	0x00000000	0x0-0xffffffff	Defines the DFI tRDLVL_MAX timing parameter (in DFI clocks), the maximum cycles between a assertion and a valid dfi_rdlvl_resp.

DENALI_CTL_307 (Address 0x133)



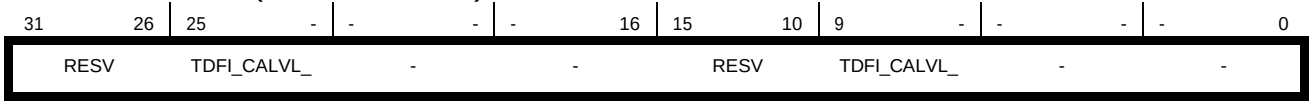
Name	Bits	Default	Range	Description
TDFI_CALVL_EN	23:16	0x00	0x0-0xff	Defines the DFI tCALVL_EN timing parameter (in DFI clocks), the minimum cycles between a
RDLVL_GATE_ERROR_STATUS	9:8	0x0	0x0-0x3	Holds the error associated with the read gate training error or gate training error interrupt. Uppermost bit set indicates a TDFI_RDLVL_RESP parameter
RDLVL_ERROR_STATUS	1:0	0x0	0x0-0x3	Holds the error associated with the data eye training error or gate training error interrupt. Uppermost bit set indicates a TDFI_RDLVL_RESP parameter

DENALI_CTL_308 (Address 0x134)



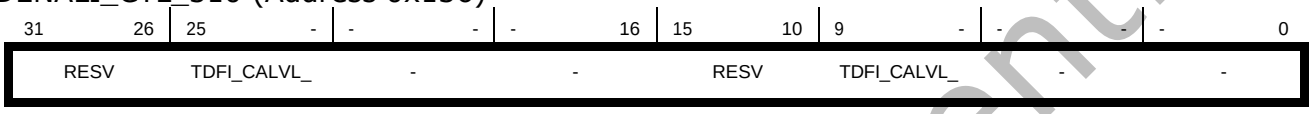
Name	Bits	Default	Range	Description
TDFI_CALVL_CAPTURE_F0	25:16	0x000	0x0-0x3ff	Defines the DFI tCALVL_CAPTURE timing parameter (in DFI clocks), the
TDFI_CALVL_CC_F0	9:0	0x000	0x0-0x3ff	Defines the DFI tCALVL_CC timing parameter (in DFI clocks), the

DENALI_CTL_309 (Address 0x135)



Name	Bits	Default	Range	Description
TDFI_CALVL_CAPTURE_F1	25:16	0x000	0x0-0x3ff	Defines the DFI tCALVL_CAPTURE timing parameter (in DFI clocks), the
TDFI_CALVL_CC_F1	9:0	0x000	0x0-0x3ff	Defines the DFI tCALVL_CC timing parameter (in DFI clocks), the

DENALI_CTL_310 (Address 0x136)

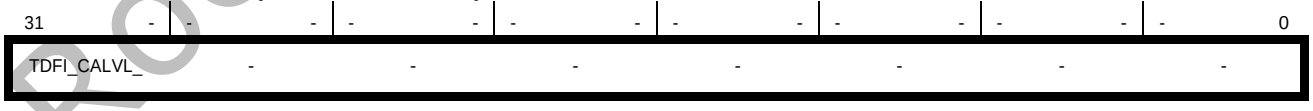


Name	Bits	Default	Range	Description
TDFI_CALVL_CAPTURE_F2	25:16	0x000	0x0-0x3ff	Defines the DFI tCALVL_CAPTURE timing parameter (in DFI clocks), the
TDFI_CALVL_CC_F2	9:0	0x000	0x0-0x3ff	Defines the DFI tCALVL_CC timing parameter (in DFI clocks), the

DENALI_CTL_311 (Address 0x137)

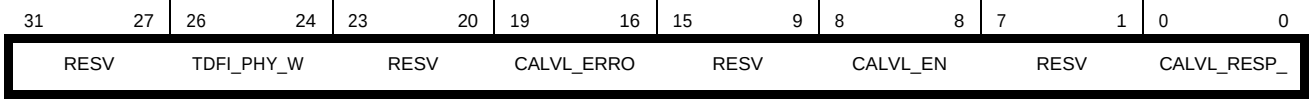
Name	Bits	Default	Range	Description
TDFI_CALVL_RESP	31:0	0x00000000	0x0-0xffffffff	Defines the DFI tCALVL_RESP timing parameter (in DFI clocks), the maximum cycles between a dfi_calvl_en assertion.

DENALI_CTL_312 (Address 0x138)



Name	Bits	Default	Range	Description
TDFI_CALVL_MAX	31:0	0x00000000	0x0-0xffffffff	Defines the DFI tCALVL_MAX timing parameter (in DFI clocks), the maximum cycles between a dfi_calvl_resp.

DENALI_CTL_313 (Address 0x139)



Name	Bits	Default	Range	Description
TDFI_PHY_WRDATA	26:24	0x0	0x0-0x7	Defines the DFI tPHY_WRDATA timing parameter (in DFI PHY clocks), the maximum cycles
CALVL_ERROR_STATUS	19:16	0x0	0x0-0xf	Holds the error associated with the CA training error interrupt. Bit (0) set indicates a TDFI_CALVL_RESP parameter
CALVL_EN	8	0x0	0x0-0x1	Enable the MC CA training module.
CALVL_RESP_MASK	0	0x0	0x0-0x1	Mask for the dfi_calvl_resp signal

DENALI_CTL_314 (Address 0x13a)

31 - - 24	23 - - 16	15 - - 8	7 - - 0
TDFI_WRCSL -	TDFI_RDCSLA -	TDFI_WRCSL -	TDFI_RDCSLA -

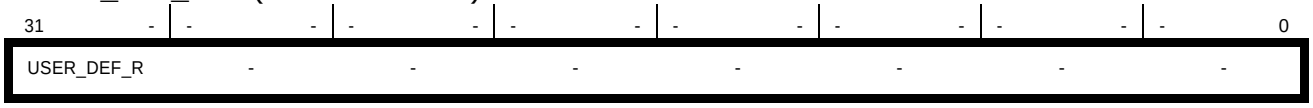
Name	Bits	Default	Range	Description
TDFI_WRCSLAT_F1	31:24	0x00	0x0-0xff	Defines the DFI tPHY_WRCSLAT timing parameter (in DFI PHY clocks), the maximum cycles
TDFI_RDCSLAT_F1	23:16	0x00	0x0-0xff	Defines the DFI tPHY_RDCSLAT timing parameter (in DFI PHY clocks), the maximum cycles
TDFI_WRCSLAT_F0	15:8	0x00	0x0-0xff	Defines the DFI tPHY_WRCSLAT timing parameter (in DFI PHY clocks), the maximum cycles
TDFI_RDCSLAT_F0	7:0	0x00	0x0-0xff	Defines the DFI tPHY_RDCSLAT timing parameter (in DFI PHY clocks), the maximum cycles

DENALI_CTL_315 (Address 0x13b)

31 - - 24	23 - - 16	15 - - 8	7 - - 0
OBSOLETE -	TDFI_WRDATA -	TDFI_WRCSL -	TDFI_RDCSLA -

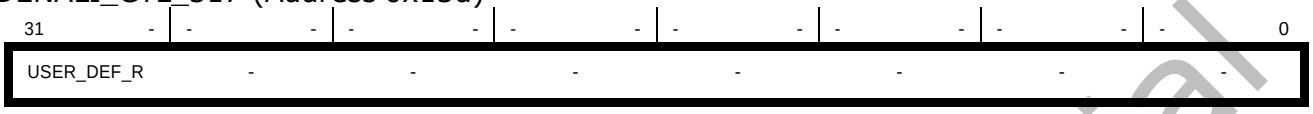
Name	Bits	Default	Range	Description
TDFI_WRDATA_DELAY	23:16	0x00	0x0-0xff	Defines the tWRDATA_DELAY timing parameter (in DFI PHY clocks), the maximum cycles between when the dfi_wrdata_en
TDFI_WRCSLAT_F2	15:8	0x00	0x0-0xff	Defines the DFI tPHY_WRCSLAT timing parameter (in DFI PHY clocks), the maximum cycles
TDFI_RDCSLAT_F2	7:0	0x00	0x0-0xff	Defines the DFI tPHY_RDCSLAT timing parameter (in DFI PHY clocks), the maximum cycles

DENALI_CTL_316 (Address 0x13c)



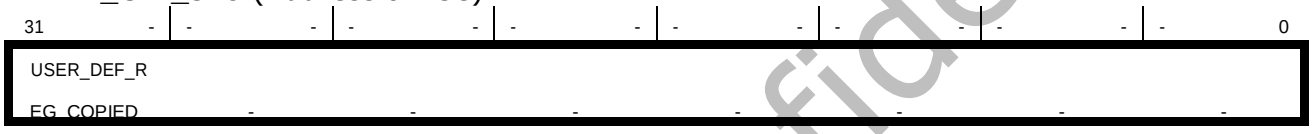
Name	Bits	Default	Range	Description
USER_DEF_REG_0	31:0	0x00000000	0x0-0xffffffff	User-defined output register 0.

DENALI_CTL_317 (Address 0x13d)



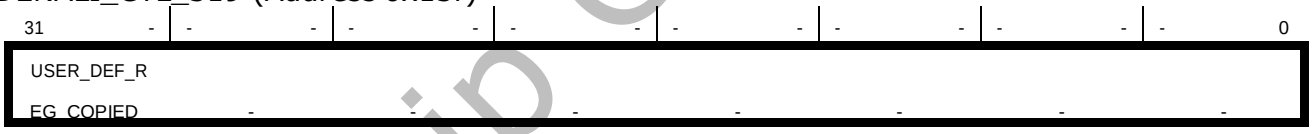
Name	Bits	Default	Range	Description
USER_DEF_REG_RO_0	31:0	0x000000	0x0-0xffffffff	User-defined input register 0.

DENALI_CTL_318 (Address 0x13e)



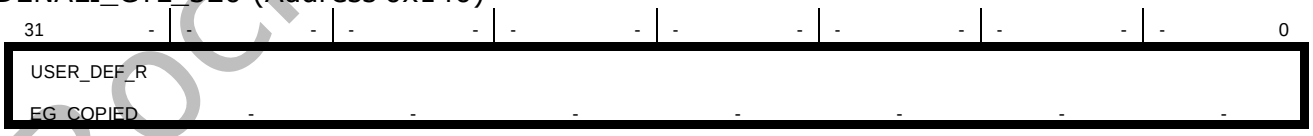
Name	Bits	Default	Range	Description
USER_DEF_REG_COPIED_F0_0	31:0	0x00000000	0x0-0xffffffff	User-defined copied output register

DENALI_CTL_319 (Address 0x13f)



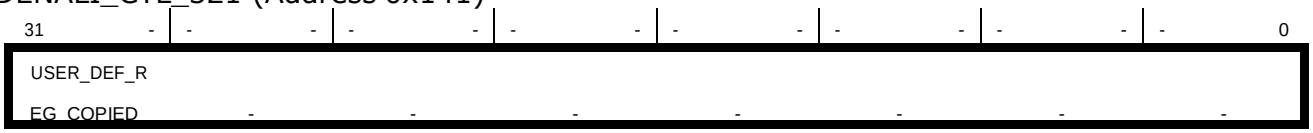
Name	Bits	Default	Range	Description
USER_DEF_REG_COPIED_F0_1	31:0	0x00000000	0x0-0xffffffff	User-defined copied output register

DENALI_CTL_320 (Address 0x140)



Name	Bits	Default	Range	Description
USER_DEF_REG_COPIED_F1_0	31:0	0x00000000	0x0-0xffffffff	User-defined copied output register

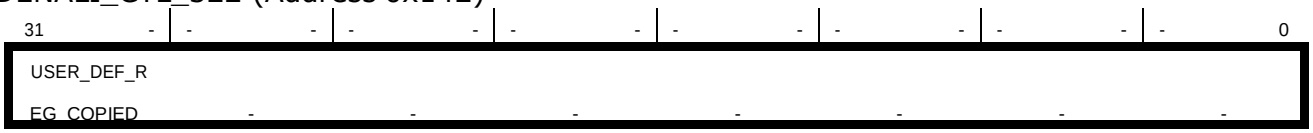
DENALI_CTL_321 (Address 0x141)



Name	Bits	Default	Range	Description

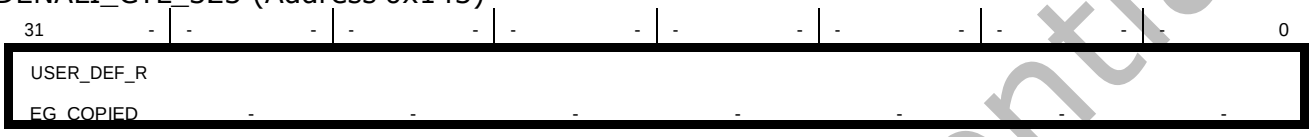
USER_DEF_REG_COPIED_F1_1	31:0	0x00000000	0x0-0xffffffff	User-defined copied output register

DENALI_CTL_322 (Address 0x142)



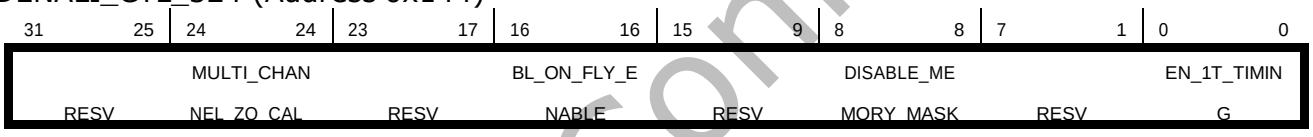
Name	Bits	Default	Range	Description
USER_DEF_REG_COPIED_F2_0	31:0	0x000000	0x0-0xffffffff	User-defined copied output register

DENALI_CTL_323 (Address 0x143)



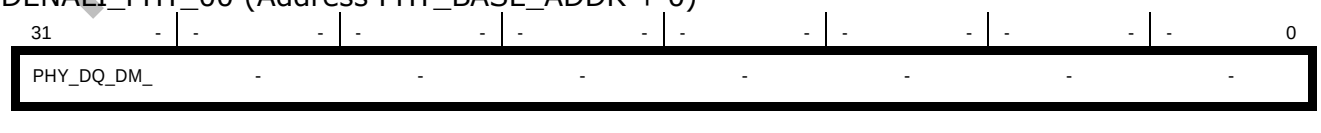
Name	Bits	Default	Range	Description
USER_DEF_REG_COPIED_F2_1	31:0	0x000000	0x0-0xffffffff	User-defined copied output register

DENALI_CTL_324 (Address 0x144)



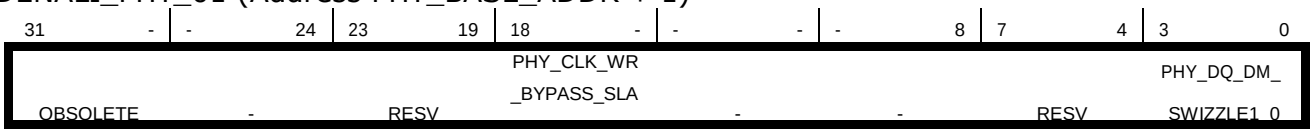
Name	Bits	Default	Range	Description
MULTI_CHANNEL_ZQ_CAL_MASTER	24	0x0	0x0-0x1	In a two controller scenario, defines if this controller will issue ZQ calibration start commands when neither controller is in a low power mode. Set to 1 to define this controller as the master that issues
BL_ON_FLY_ENABLE	16	0x0	0x0-0x1	Enables the burst length on the fly
DISABLE_MEMORY_MASKED_WRITE	8	0x0	0x0-0x1	Restricts the controller from masked write commands. Set to 1
EN_1T_TIMING	0	0x0	0x0-0x1	Enable 1T timing in a system supporting both 1T and 2T timing.

DENALI_PHY_00 (Address PHY_BASE_ADDR + 0)



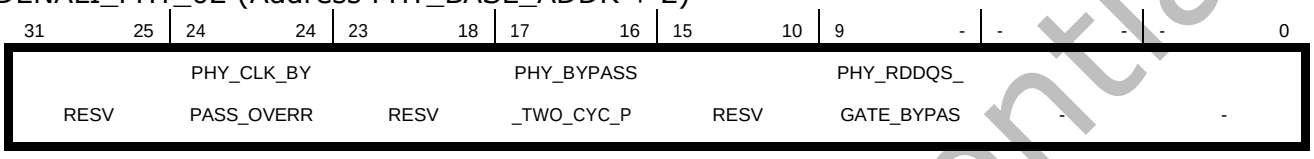
Name	Bits	Default	Range	Description
PHY_DQ_DM_SWIZZLE0_0	31:0	0x00000000	0x0-0xffffffff	DQ/DM bit swizzling 0 for slice 0. Bits (3:0) inform the PHY which bit in {DM,DQ} map to DQ0, Bits (7:4) {DM,DQ} map to DQ1, etc.

DENALI_PHY_01 (Address PHY_BASE_ADDR + 1)



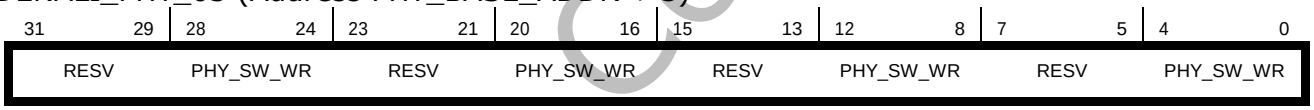
Name	Bits	Default	Range	Description
PHY_CLK_WR_BYPASS_SLAVE_DELAY_0	18:8	0x000	0x0-0x7ff	Write data clock bypass mode
PHY_DQ_DM_SWIZZLE1_0	3:0	0x0	0x0-0xf	DQ/DM bit swizzling 1 for slice 0. Bits (3:0) inform the PHY which bit

DENALI_PHY_02 (Address PHY_BASE_ADDR + 2)



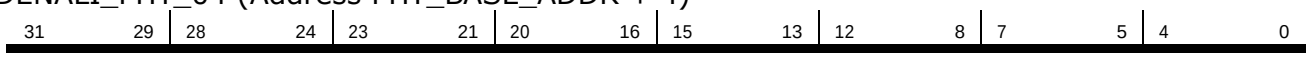
Name	Bits	Default	Range	Description
PHY_CLK_BYPASS_OVERRIDE_0	24	0x0	0x0-0x1	Bypass mode override setting for
PHY_BYPASS_TWO_CYC_PREAMBLE_0	17:16	0x0	0x0-0x3	PHY two_cycle_preamble for
PHY_RDDQS_GATE_BYPASS_SLAVE_DE	9:0	0x000	0x0-0x3ff	Read DQS bypass mode slave

DENALI_PHY_03 (Address PHY_BASE_ADDR + 3)



Name	Bits	Default	Range	Description
PHY_SW_WRDQ3_SHIFT_0	28:24	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for write DQ3 for slice 0. Bit (0) enables override of half_cycle_shift. Bit (1)
PHY_SW_WRDQ2_SHIFT_0	20:16	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for write DQ2 for slice 0. Bit (0) enables override of half_cycle_shift. Bit (1)
PHY_SW_WRDQ1_SHIFT_0	12:8	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for write DQ1 for slice 0. Bit (0) enables override of half_cycle_shift. Bit (1)
PHY_SW_WRDQ0_SHIFT_0	4:0	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for write DQ0 for slice 0. Bit (0) enables override of half_cycle_shift. Bit (1)

DENALI_PHY_04 (Address PHY_BASE_ADDR + 4)



RESV	PHY_SW_WR	RESV	PHY_SW_WR	RESV	PHY_SW_WR	RESV	PHY_SW_WR

Name	Bits	Default	Range	Description
PHY_SW_WRDQ7_SHIFT_0	28:24	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for write DQ7 for slice 0. Bit (0) enables override of half_cycle_shift. Bit (1)
PHY_SW_WRDQ6_SHIFT_0	20:16	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for write DQ6 for slice 0. Bit (0) enables override of half_cycle_shift. Bit (1)
PHY_SW_WRDQ5_SHIFT_0	12:8	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for write DQ5 for slice 0. Bit (0) enables override of half_cycle_shift. Bit (1)
PHY_SW_WRDQ4_SHIFT_0	4:0	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for write DQ4 for slice 0. Bit (0) enables override of half_cycle_shift. Bit (1)

DENALI_PHY_05 (Address PHY_BASE_ADDR + 5)

31 - 24	23 19	18 16	15 12	11 8	7 5	4 0
OBSOLETE -	RESV	PHY_DQ_TSE	RESV	PHY_SW_WR	RESV	PHY_SW_WR

Name	Bits	Default	Range	Description
PHY_DQ_TSEL_ENABLE_0	18:16	0x0	0x0-0x7	Operation type tsel enables for DQ/DM signals for slice 0. Bit (0) enables tsel_en during read cycles. Bit (1) enables tsel_en during write
PHY_SW_WRDQS_SHIFT_0	11:8	0x0	0x0-0xf	Manual override of automatic half_cycle_shift/cycle_shift for write DQS for slice 0. Bit (0) enables override of half_cycle_shift. Bit (1)
PHY_SW_WRDM_SHIFT_0	4:0	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for write DM for slice 0. Bit (0) enables override of half_cycle_shift. Bit (1)

DENALI_PHY_06 (Address PHY_BASE_ADDR + 6)

31 27	26 24	23 -	- -	- -	- -	- -	- 0
RESV	PHY_DQS_TS	PHY_DQ_TSE	-	-	-	-	-

Name	Bits	Default	Range	Description

PHY_DQS_TSEL_ENABLE_0	26:24	0x0	0x0-0x7	Operation type tsel enables for DQS signals for slice 0. Bit (0) enables tsel_en during read cycles. Bit (1) enables tsel_en during write
PHY_DQ_TSEL_SELECT_0	23:0	0x000000	0x0-0xffffff	Operation type tsel select values for DQ/DM signals for slice 0. Bits (3:0) are tsel_sel values during read cycles. Bits (7:4) are tsel_sel

DENALI_PHY_07 (Address PHY_BASE_ADDR + 7)

31 26	25 24	23 -	- -	- -	- -	- -	- 0
RESV	PHY_TWO_CYC_PREAMBLE	PHY_DQS_TSEL_SELECT_0	-	-	-	-	-

Name	Bits	Default	Range	Description
PHY_TWO_CYC_PREAMBLE_0	25:24	0x0	0x0-0x3	2 cycle preamble support for slice 0. Bit (0) controls the 2 cycle read preamble. Bit (1) controls the 2
PHY_DQS_TSEL_SELECT_0	23:0	0x000000	0x0-0xffffff	Operation type tsel select values for DQS signals for slice 0. Bits (3:0) are tsel_sel values during read cycles. Bits (7:4) are tsel_sel

DENALI_PHY_08 (Address PHY_BASE_ADDR + 8)

31 25	24 24	23 17	16 16	15 10	9 8	7 1	0 0
RESV	PHY_PER_CS_TRAINING_INDEX_0	RESV	PHY_PER_CS_TRAINING_M	RESV	PHY_PER_RANK_CS_MAP_	RESV	PHY_DBI_MO

Name	Bits	Default	Range	Description
PHY_PER_CS_TRAINING_INDEX_0	24	0x0	0x0-0x1	For per-rank training, indicates which ranksparamtersareread/
PHY_PER_CS_TRAINING_MULTICAST_EN_0	16	0x1	0x0-0x1	When set, a register write will update parameters for all ranks at
PHY_PER_RANK_CS_MAP_0	9:8	0x0	0x0-0x3	Per-rank CS map for slice 0.
PHY_DBI_MODE_0	0	0x0	0x0-0x1	DBI mode for slice 0. Bit (0) enables return of DBI read data. Bit

DENALI_PHY_09 (Address PHY_BASE_ADDR + 9)

31 28	27 24	23 20	19 16	15 12	11 8	7 2	1 0
RESV	PHY_LP4_BOOT_RPTR_UP	RESV	PHY_LP4_BOOT_RDDATA_	RESV	PHY_LP4_BOOT_RDDATA_	RESV	PHY_LP4_BOOT_RDDATA_

Name	Bits	Default	Range	Description
PHY_LP4_BOOT_RPTR_UPDATE_0	27:24	0x0	0x0-0xf	For LPDDR4 boot frequency, the offset in cycles from the

PHY_LP4_BOOT_RDDATA_EN_TSEL_DLY_0	19:16	0x0	0x0-0xf	For LPDDR4 boot frequency, the number of cycles that the dfi_rddata_en signal is earlier than
PHY_LP4_BOOT_RDDATA_EN_DLY_0	11:8	0x0	0x0-0xf	For LPDDR4 boot frequency, the number of cycles that the
PHY_LP4_BOOT_RDDATA_EN_IE_DLY_0	1:0	0x0	0x0-0x3	For LPDDR4 boot frequency, the number of cycles that the dfi_rddata_en signal is earlier than

DENALI_PHY_10 (Address PHY_BASE_ADDR + 10)

31 - 24	23 17	16 16	15 15	14 8	7 4	3 0
OBSOLETE -	RESV	PHY_SLICE_PWR_RDC_DIS	RESV	PHY_LPBK_C	RESV	PHY_LP4_BOOT_RDDQS_L

Name	Bits	Default	Range	Description
PHY_SLICE_PWR_RDC_DISABLE_0	16	0x0	0x0-0x1	data slice power reduction disable
PHY_LPBK_CONTROL_0	14:8	0x00	0x0-0x7f	Loopback control bits for slice 0.
PHY_LP4_BOOT_RDDQS_LATENCY_ADJ	3:0	0x0	0x0-0xf	For LPDDR4 boot frequency, the number of cycles to delay the

DENALI_PHY_11 (Address PHY_BASE_ADDR + 11)

31 25	24 24	23 21	20 16	15 10	9 -	- -	- 0
RESV	SC_PHY_SNAP_OBS_REGS	RESV	PHY_GATE_ERROR_DELAY_SELECT	RESV	PHY_RDDQS_DQ_BYPASS_	-	-

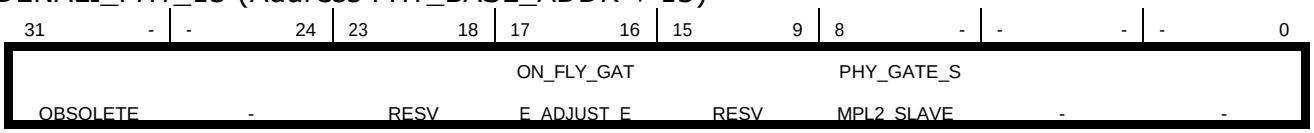
Name	Bits	Default	Range	Description
SC_PHY_SNAP_OBS_REGS_0	24	0x0	0x0-0x1	Initiates a snapshot of the internal observation registers for slice 0.
PHY_GATE_ERROR_DELAY_SELECT_0	20:16	0x00	0x0-0x1f	Number of cycles to wait for the DQS gate to close before flagging
PHY_RDDQS_DQ_BYPASS_SLAVE_DELAY_0	9:0	0x000	0x0-0x3ff	Read DQS data clock bypass mode

DENALI_PHY_12 (Address PHY_BASE_ADDR + 12)

31 25	24 -	- -	- 16	15 10	9 8	7 1	0 0
RESV	PHY_GATE_SMPL1_SLAVE	-	-	RESV	PHY_LPDDR_TYPE_0	RESV	PHY_LPDDR_0

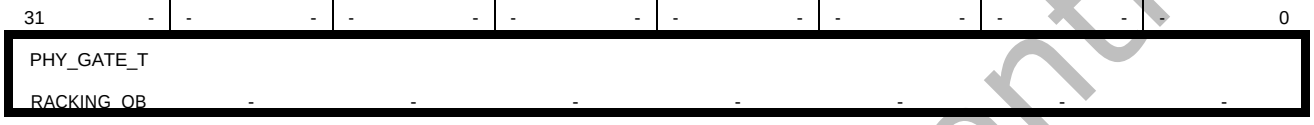
Name	Bits	Default	Range	Description
PHY_GATE_SMPL1_SLAVE_DELAY_0	24:16	0x000	0x0-0x1ff	Number of cycles to delay the read DQS gate signal to generate gate1
PHY_LPDDR_TYPE_0	9:8	0x0	0x0-0x3	Indicates the type of DRAM for slice 0. Clear to 0 for DDR3 or
PHY_LPDDR_0	0	0x0	0x0-0x1	Indicates a cycle of delay for the

DENALI_PHY_13 (Address PHY_BASE_ADDR + 13)



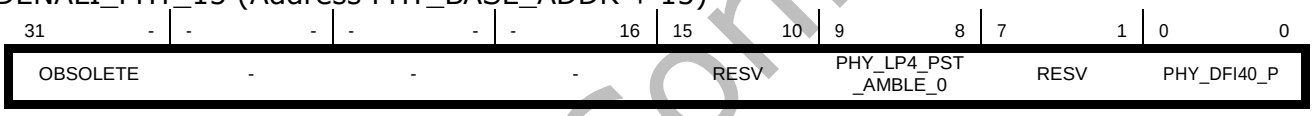
Name	Bits	Default	Range	Description
ON_FLY_GATE_ADJUST_EN_0	17:16	0x0	0x0-0x3	Control the on the fly gate
PHY_GATE_SMPL2_SLAVE_DELAY_0	8:0	0x000	0x0-0x1ff	Number of cycles to delay the read DQS gate signal to generate gate2

DENALI_PHY_14 (Address PHY_BASE_ADDR + 14)



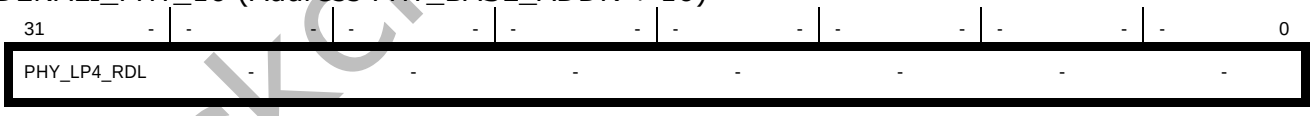
Name	Bits	Default	Range	Description
PHY_GATE_TRACKING_OBS_0	31:0	0x00000000	0x0-0xffffffff	Report the on the fly gate

DENALI_PHY_15 (Address PHY_BASE_ADDR + 15)



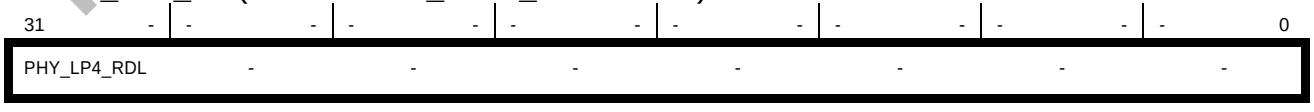
Name	Bits	Default	Range	Description
PHY_LP4_PST_AMBLE_0	9:8	0x0	0x0-0x3	Controls the read postamble
PHY_DFI40_POLARITY_0	0	0x0	0x0-0x1	Indicates the dfi_wrdata_cs_n and dfi_rddata_cs_n is low active or

DENALI_PHY_16 (Address PHY_BASE_ADDR + 16)



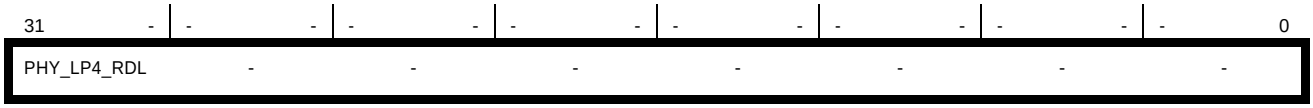
Name	Bits	Default	Range	Description
PHY_LP4_RDLVL_PATT8_0	31:0	0x00000000	0x0-0xffffffff	LPDDR4 read leveling pattern 8

DENALI_PHY_17 (Address PHY_BASE_ADDR + 17)



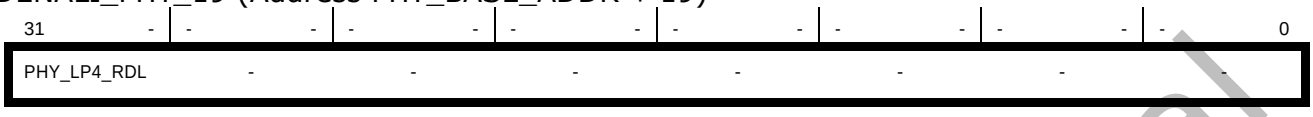
Name	Bits	Default	Range	Description
PHY_LP4_RDLVL_PATT9_0	31:0	0x000000	0x0-0xffffffff	LPDDR4 read leveling pattern 9

DENALI_PHY_18 (Address PHY_BASE_ADDR + 18)



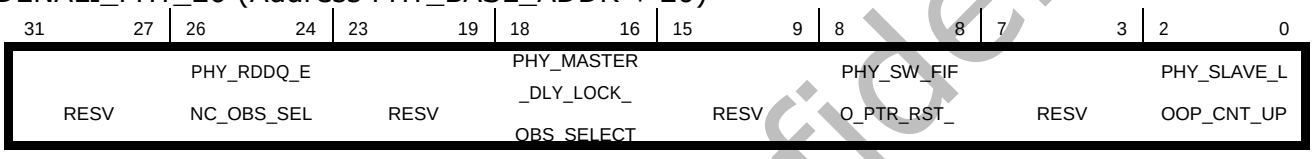
Name	Bits	Default	Range	Description
PHY_LP4_RDLVL_PATT10_0	31:0	0x000000	0x0-0xffffffff	LPDDR4 read leveling pattern 10

DENALI_PHY_19 (Address PHY_BASE_ADDR + 19)



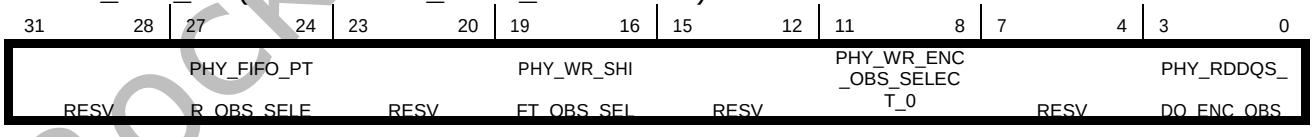
Name	Bits	Default	Range	Description
PHY_LP4_RDLVL_PATT11_0	31:0	0x000000 00	0x0-0xffffffff	LPDDR4 read leveling pattern 11

DENALI_PHY_20 (Address PHY_BASE_ADDR + 20)



Name	Bits	Default	Range	Description
PHY_RDDQ_ENC_OBS_SELECT_0	26:24	0x0	0x0-0x7	Select value to map the internal read DQ slave delay encoded settings to the accessible read DQ
PHY_MASTER_DLY_LOCK_OBS_SELECT_0	18:16	0x0	0x0-0x7	Select value to map the internal master delay observation registers
PHY_SW_FIFO_PTR_RST_DISABLE_0	8	0x0	0x0-0x1	Disables automatic reset of the read entry FIFO pointers for slice 0.
PHY_SLAVE_LOOP_CNT_UPDATE_0	2:0	0x0	0x0-0x7	Sets the frequency by which the slave delay encoded value holding

DENALI_PHY_21 (Address PHY_BASE_ADDR + 21)



Name	Bits	Default	Range	Description
PHY_FIFO_PTR_OBS_SELECT_0	27:24	0x0	0x0-0xf	Select value to map the internal read entry FIFO read/write pointers to the accessible read entry FIFO
PHY_WR_SHIFT_OBS_SELECT_0	19:16	0x0	0x0-0xf	Select value to map the internal write DQ/DQS automatic cycle/ half_cycle shift settings to the
PHY_WR_ENC_OBS_SELECT_0	11:8	0x0	0x0-0xf	Select value to map the internal write DQ slave delay encoded settings to the accessible write DQ

PHY_RDDQS_DQ_ENC_OBS_SELECT_0	3:0	0x0	0x0-0xf	Select value to map the internal read DQS DQ rise/fall slave delay encoded settings to the accessible

DENALI_PHY_22 (Address PHY_BASE_ADDR + 22)

31 28	27 24	23 22	21 16	15 9	8 8	7 1	0 0
RESV	PHY_WRLVL_UPDT_WAIT	RESV	PHY_WRLVL_CAPTURE_CN	RESV	SC_PHY_LVL_DEBUG_CONT	RESV	PHY_LVL_DEBUG_MODE_0

Name	Bits	Default	Range	Description
PHY_WRLVL_UPDT_WAIT_CNT_0	27:24	0x0	0x0-0xf	Number of cycles to wait after changing DQS slave delay setting
PHY_WRLVL_CAPTURE_CNT_0	21:16	0x00	0x0-0x3f	Number of samples to take at each DQS slave delay setting during
SC_PHY_LVL_DEBUG_CONT_0	8	0x0	0x0-0x1	Allows the leveling state machine to advance (when in debug mode)
PHY_LVL_DEBUG_MODE_0	0	0x0	0x0-0x1	Enables leveling debug mode for

DENALI_PHY_23 (Address PHY_BASE_ADDR + 23)

31 28	27 24	23 22	21 16	15 12	11 8	7 6	5 0
RESV	PHY_RDLVL_UPDT_WAIT	RESV	PHY_RDLVL_CAPTURE_CN	RESV	PHY_GTLVL_UPDT_WAIT_C	RESV	PHY_GTLVL_CAPTURE_CNT

Name	Bits	Default	Range	Description
PHY_RDLVL_UPDT_WAIT_CNT_0	27:24	0x0	0x0-0xf	Number of cycles to wait after changing DQS slave delay setting
PHY_RDLVL_CAPTURE_CNT_0	21:16	0x00	0x0-0x3f	Number of samples to take at each DQS slave delay setting during
PHY_GTLVL_UPDT_WAIT_CNT_0	11:8	0x0	0x0-0xf	Number of cycles + 4 to wait after changing DQS slave delay setting
PHY_GTLVL_CAPTURE_CNT_0	5:0	0x00	0x0-0x3f	Number of samples to take at each DQS slave delay setting during

DENALI_PHY_24 (Address PHY_BASE_ADDR + 24)

31 30	29 24	23 -	- 16	15 13	12 8	7 2	1 0
RESV	PHY_WDQLVL_BURST_CNT_0	PHY_RDLVL_DATA_MASK_	-	RESV	PHY_RDLVL_RDDQS_DQ_	RESV	PHY_RDLVL_

Name	Bits	Default	Range	Description
PHY_WDQLVL_BURST_CNT_0	29:24	0x00	0x0-0x3f	Defines the write/read burst length in bytes during the write data
PHY_RDLVL_DATA_MASK_0	23:16	0x00	0x0-0xff	Per-bit mask for read leveling for slice 0. If all bits are not used, only
PHY_RDLVL_RDDQS_DQ_OBS_SELECT_0	12:8	0x00	0x0-0x1f	Select value to map an individual DQ data window leading/trailing edge to the leading/trailing edge

PHY_RDLVL_OP_MODE_0	1:0	0x0	0x0-0x3	Read leveling algorithm select for slice 0. Clear to 0 to move linearly from left to right. Set to 1 to start

DENALI_PHY_25 (Address PHY_BASE_ADDR + 25)

31 28	27 24	23 19	18 -	- -	- 8	7 3	2 0
RESV	PHY_WDQLVL _UPDT_WAIT_	RESV	PHY_WDQLVL _DQDM_SLV_ DLY_JUMP_O	-	-	RESV	PHY_WDQLVL _PATT_0

Name	Bits	Default	Range	Description
PHY_WDQLVL_UPDT_WAIT_CNT_0	27:24	0x0	0x0-0xf	Number of cycles to wait after changing the DQ slave delay
PHY_WDQLVL_DQDM_SLV_DLY_JUMP_OFFSET_0	18:8	0x000	0x0-0x7ff	Defines the write/read burst length in bytes during the write data
PHY_WDQLVL_PATT_0	2:0	0x0	0x0-0x7	Defines the training patterns to be used during the write data leveling sequence for slice 0. Bit (0) corresponds to the LFSR data training pattern. Bit (1) corresponds to the CLK data training pattern. Bit (2) corresponds to user-defined

DENALI_PHY_26 (Address PHY_BASE_ADDR + 26)

31 -	- 24	23 17	16 16	15 12	11 8	7 4	3 0
OBSOLETE	-	RESV	SC_PHY_WD QLVL_CLR_P	RESV	PHY_WDQLVL _QTR_DLY_ST	RESV	PHY_WDQLVL _DQDM_OBS_

Name	Bits	Default	Range	Description
SC_PHY_WDQLVL_CLR_PREV_RESULTS_0	16	0x0	0x0-0x1	Clears the previous result value to allow a clean slate comparison for future write DQ leveling results for
PHY_WDQLVL_QTR_DLY_STEP_0	11:8	0x0	0x0-0xf	Defines the step granularity for the logic to use once an edge is found. When this occurs, the logic jumps back to the previous invalid value
PHY_WDQLVL_DQDM_OBS_SELECT_0	3:0	0x0	0x0-0xf	Select value to map an individual DQ data window leading/trailing edge to the leading/trailing edge

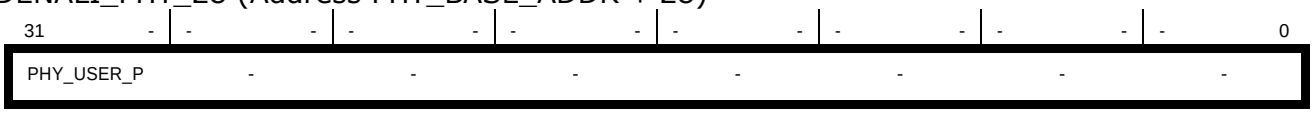
DENALI_PHY_27 (Address PHY_BASE_ADDR + 27)

31 -	- -	- -	- 16	15 9	8 -	- -	- 0
OBSOLETE	-	-	-	RESV	PHY_WDQLVL _DATADM_MA	-	-

Name	Bits	Default	Range	Description

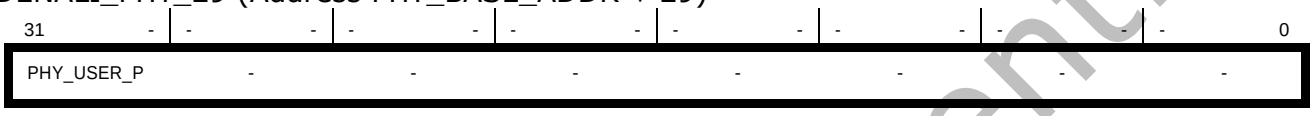
PHY_WDQLVL_DATADM_MASK_0	8:0	0x000	0x0-0x1ff	Per-bit mask for write data leveling for slice 0. Set to 1 to mask any bit

DENALI_PHY_28 (Address PHY_BASE_ADDR + 28)



Name	Bits	Default	Range	Description
PHY_USER_PATT0_0	31:0	0x00000000	0x0-0xffffffff	User-defined pattern to be used during write data leveling for slice 0. This register holds the bytes 3 to 0 written/read from device.

DENALI_PHY_29 (Address PHY_BASE_ADDR + 29)

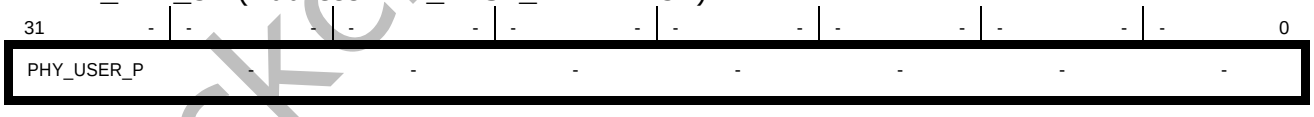


Name	Bits	Default	Range	Description
PHY_USER_PATT1_0	31:0	0x00000000	0x0-0xffffffff	User-defined pattern to be used during write data leveling for slice 0. This register holds the bytes 7 to 4 written/read from device.

DENALI_PHY_30 (Address PHY_BASE_ADDR + 30)

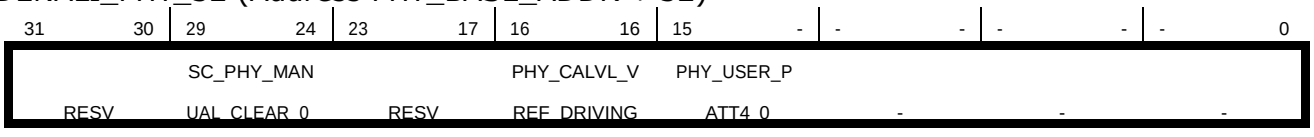
Name	Bits	Default	Range	Description
PHY_USER_PATT2_0	31:0	0x00000000	0x0-0xffffffff	User-defined pattern to be used during write data leveling for slice 0. This register holds the bytes 11 to 8 written/read from device.

DENALI_PHY_31 (Address PHY_BASE_ADDR + 31)



Name	Bits	Default	Range	Description
PHY_USER_PATT3_0	31:0	0x00000000	0x0-0xffffffff	User-defined pattern to be used during write data leveling for slice 0. This register holds the bytes 15 to 12 written/read from device.

DENALI_PHY_32 (Address PHY_BASE_ADDR + 32)



Name	Bits	Default	Range	Description

SC_PHY_MANUAL_CLEAR_0	29:24	0x00	0x0-0x3f	Manual reset/clear of internal logic for slice 0. Bit (0) initiates manual setup of the read DQS gate. Bit (1) is reset of read entry FIFO pointers. Bit (2) is reset of master delay min/ max lock values. Bit (3) is manual reset of master delay unlock
PHY_CALVL_VREF_DRIVING_SLICE_0	16	0x0	0x0-0x1	Indicates if slice 0 is used to drive the VREF value to the device
PHY_USER_PATT4_0	15:0	0x0000	0x0-0xffff	User-defined pattern to be used during write data leveling for slice 0. This register holds the DM bit for

DENALI_PHY_33 (Address PHY_BASE_ADDR + 33)

31 - 8	7 - 0
OBSOLETE -	PHY_FIFO_PT -

Name	Bits	Default	Range	Description
PHY_FIFO_PTR_OBS_0	7:0	0x00	0x0-0xff	Observation register for read entry FIFO pointers for slice 0. READ-

DENALI_PHY_34 (Address PHY_BASE_ADDR + 34)

31 - 0
PHY_LPBK_R -

Name	Bits	Default	Range	Description
PHY_LPBK_RESULT_OBS_0	31:0	0x00000000	0x0-0xffffffff	Observation register containing loopback status/results for slice 0.

DENALI_PHY_35 (Address PHY_BASE_ADDR + 35)

31 26	25 - 16	15 - 0
RESV	PHY_MASTER_DLY_LOCK_ -	PHY_LPBK_ERROR_COUN -

Name	Bits	Default	Range	Description
PHY_MASTER_DLY_LOCK_OBS_0	25:16	0x000	0x0-0x3ff	Observation register for master delay results for slice 0. READ-
PHY_LPBK_ERROR_COUNT_OBS_0	15:0	0x0000	0x0-0xffff	Observation register containing total number of loopback error data

DENALI_PHY_36 (Address PHY_BASE_ADDR + 36)

31 - 24	23 - 16	15 15	14 8	7 6	5 0
PHY_RDDQS_DQ_FALL_AD -	PHY_RDDQS_DQ_RISE_AD -	RESV	PHY_RDDQS_BASE_SLV_DL	RESV	PHY_RDDQ_SLV_DLY_ENC_

Name	Bits	Default	Range	Description

PHY_RDDQS_DQ_FALL_ADDER_SLV_DL	31:24	0x00	0x0-0xff	Observation register for read DQS DQ falling edge adder slave delay
PHY_RDDQS_DQ_RISE_ADDER_SLV_DL	23:16	0x00	0x0-0xff	Observation register for read DQS DQ rising edge adder slave delay
PHY_RDDQS_BASE_SLV_DLY_ENC_OBS_0	14:8	0x00	0x0-0x7f	Observation register for read DQS base slave delay encoded value for
PHY_RDDQ_SLV_DLY_ENC_OBS_0	5:0	0x00	0x0-0x3f	Observation register for read DQ slave delay encoded values for

DENALI_PHY_37 (Address PHY_BASE_ADDR + 37)

31 -	- 24	23 23	22 16	15 10	9 -	- -	- 0
PHY_WRDQ_BASE_SLV_DL	-	RESV	PHY_WRDQS_BASE_SLV_DLY_ENC_OBS	RESV	PHY_RDDQS_GATE_SLV_DL	-	-

Name	Bits	Default	Range	Description
PHY_WRDQ_BASE_SLV_DLY_ENC_OBS_0	31:24	0x00	0x0-0xff	Observation register for write DQ base slave delay encoded value for
PHY_WRDQS_BASE_SLV_DLY_ENC_OBS_0	22:16	0x00	0x0-0x7f	Observation register for write DQS base slave delay encoded value for
PHY_RDDQS_GATE_SLV_DLY_ENC_OBS_0	9:0	0x000	0x0-0x3ff	Observation register for read DQS gate slave delay encoded value for

DENALI_PHY_38 (Address PHY_BASE_ADDR + 38)

31 26	25 -	- -	- 16	15 11	10 8	7 -	- 0
RESV	PHY_WRLVL_HARD0_DELA	-	-	RESV	PHY_WR_SHIFT_OBS_0	PHY_WR_ADDER_SLV_DLY	-

Name	Bits	Default	Range	Description
PHY_WRLVL_HARD0_DELAY_OBS_0	25:16	0x000	0x0-0x3ff	Observation register for write leveling last hard 0 DQS slave
PHY_WR_SHIFT_OBS_0	10:8	0x0	0x0-0x7	Observation register for automatic half cycle and cycle shift values for
PHY_WR_ADDER_SLV_DLY_ENC_OBS_0	7:0	0x00	0x0-0xff	Observation register for write adder slave delay encoded value for slice

DENALI_PHY_39 (Address PHY_BASE_ADDR + 39)

31 -	- -	- -	- 16	15 10	9 -	- -	- 0
OBSOLETE	-	-	-	RESV	PHY_WRLVL_HARD1_DELA	-	-

Name	Bits	Default	Range	Description
PHY_WRLVL_HARD1_DELAY_OBS_0	9:0	0x000	0x0-0x3ff	Observation register for write leveling first hard 1 DQS slave

DENALI_PHY_40 (Address PHY_BASE_ADDR + 40)

31 -	- 24	23 17	16 -	- -	- -	- -	- 0

OBSOLETE	-	RESV	PHY_WRLVL_STATUS_OBS	-	-	-	-								

Name	Bits	Default	Range	Description
PHY_WRLVL_STATUS_OBS_0	16:0	0x00000	0x0-0x1ffff	Observation register for write leveling status for slice 0. READ-

DENALI_PHY_41 (Address PHY_BASE_ADDR + 41)

31	25	24	-	-	-	-	16	15	9	8	-	-	-	-	0
RESV		PHY_GATE_SMPL2_SLV_DL		-		-		RESV		PHY_GATE_SMPL1_SLV_DL		-		-	

Name	Bits	Default	Range	Description
PHY_GATE_SMPL2_SLV_DLY_ENC_OBS_0	24:16	0x000	0x0-0x1ff	Observation register for gate sample1 slave delay encoded
PHY_GATE_SMPL1_SLV_DLY_ENC_OBS_0	8:0	0x000	0x0-0x1ff	Observation register for gate sample1 slave delay encoded

DENALI_PHY_42 (Address PHY_BASE_ADDR + 42)

31	30	29	-	-	-	-	16	15	-	-	-	-	-	-	0
RESV		PHY_GTLVL_HARD0_DELAY		-		-		PHY_WRLVL_ERROR_OBS		-		-		-	

Name	Bits	Default	Range	Description
PHY_GTLVL_HARD0_DELAY_OBS_0	29:16	0x0000	0x0-0x3fff	Observation register for gate training first hard 0 DQS slave
PHY_WRLVL_ERROR_OBS_0	15:0	0x0000	0x0-0xffff	Observation register for write leveling error status for slice 0.

DENALI_PHY_43 (Address PHY_BASE_ADDR + 43)

31	28	27	-	-	-	-	16	15	14	13	-	-	-	-	0
RESV		PHY_GTLVL_STATUS_OBS_0		-		-		RESV		PHY_GTLVL_HARD1_DELAY		-		-	

Name	Bits	Default	Range	Description
PHY_GTLVL_STATUS_OBS_0	27:16	0x000	0x0-0xfff	Observation register for gate training status for slice 0. READ-
PHY_GTLVL_HARD1_DELAY_OBS_0	13:0	0x0000	0x0-0x3fff	Observation register for gate training last hard 1 DQS slave

DENALI_PHY_44 (Address PHY_BASE_ADDR + 44)

31	26	25	-	-	-	-	16	15	10	9	-	-	-	-	0
RESV		PHY_RDLVL_RDDQS_DQ_T		-		-		RESV		PHY_RDLVL_RDDQS_DQ_L		-		-	

Name	Bits	Default	Range	Description

PHY_RDLVL_RDDQS_DQ_TE_DLY_OBS_	25:16	0x000	0x0-0x3ff	Observation register for read leveling data window trailing edge
PHY_RDLVL_RDDQS_DQ_LE_DLY_OBS_0	9:0	0x000	0x0-0x3ff	Observation register for read leveling data window leading edge

DENALI_PHY_45 (Address PHY_BASE_ADDR + 45)

31	-	-	-	-	-	-	-	-	8	7	2	1	0
OBSOLETE		-		-		-		-		RESV		PHY_RDLVL_RDDQS_DQ_N	

Name	Bits	Default	Range	Description
PHY_RDLVL_RDDQS_DQ_NUM_WINDOWS_OBS_0	1:0	0x0	0x0-0x3	Observation register for read leveling number of windows found

DENALI_PHY_46 (Address PHY_BASE_ADDR + 46)

31	-	-	-	-	-	-	-	-	-	-	-	0
PHY_RDLVL_STATUS_OBS		-		-		-		-		-		-

Name	Bits	Default	Range	Description
PHY_RDLVL_STATUS_OBS_0	31:0	0x00000000	0x0-0xffffffff	Observation register for read leveling status for slice 0. READ-

DENALI_PHY_47 (Address PHY_BASE_ADDR + 47)

31	27	26	-	-	-	-	16	15	11	10	-	-	-	-	0
RESV		PHY_WDQLVL_DQDM_TE_D		-		-		RESV		PHY_WDQLVL_DQDM_LE_D		-		-	

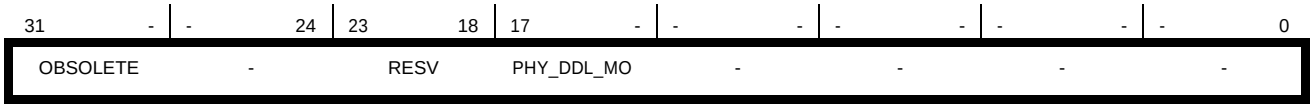
Name	Bits	Default	Range	Description
PHY_WDQLVL_DQDM_TE_DLY_OBS_0	26:16	0x000	0x0-0x7ff	Observation register for write data leveling data window trailing edge
PHY_WDQLVL_DQDM_LE_DLY_OBS_0	10:0	0x000	0x0-0x7ff	Observation register for write data leveling data window leading edge

DENALI_PHY_48 (Address PHY_BASE_ADDR + 48)

31	-	-	-	-	-	-	-	-	-	-	-	0
PHY_WDQLVL_STATUS_OBS_0		-		-		-		-		-		-

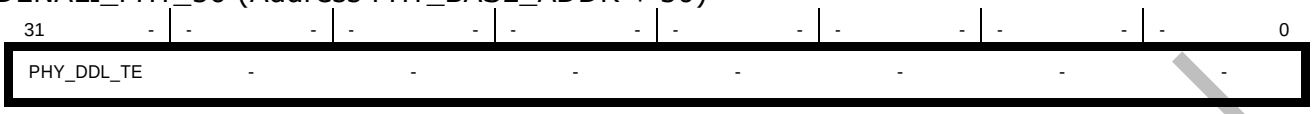
Name	Bits	Default	Range	Description
PHY_WDQLVL_STATUS_OBS_0	31:0	0x00000000	0x0-0xffffffff	Observation register for write data leveling status for slice 0. READ-

DENALI_PHY_49 (Address PHY_BASE_ADDR + 49)



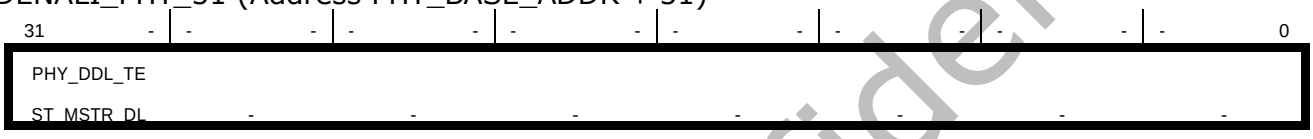
Name	Bits	Default	Range	Description
PHY_DDL_MODE_0	17:0	0x00000	0x0-0x3ffff	DDL mode for slice 0.

DENALI_PHY_50 (Address PHY_BASE_ADDR + 50)



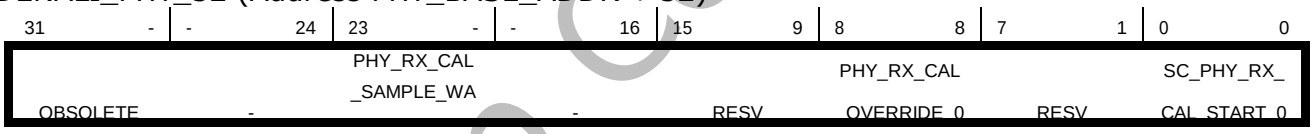
Name	Bits	Default	Range	Description
PHY_DDL_TEST_OBS_0	31:0	0x0000000 00	0x0-0xffffffff	DDL test observation for slice 0.

DENALI_PHY_51 (Address PHY_BASE_ADDR + 51)



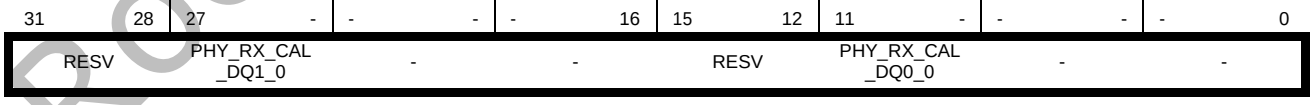
Name	Bits	Default	Range	Description
PHY_DDL_TEST_MSTR_DLY_OBS_0	31:0	0x000000	0x0-0xffffffff	DDL test observation delays for

DENALI_PHY_52 (Address PHY_BASE_ADDR + 52)



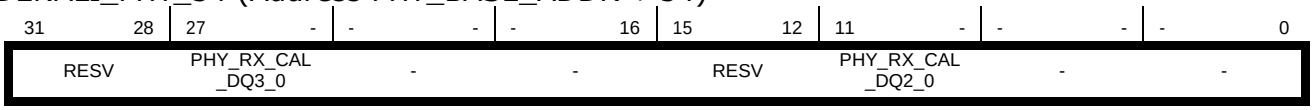
Name	Bits	Default	Range	Description
PHY_RX_CAL_SAMPLE_WAIT_0	23:16	0x00	0x0-0xff	RX Calibration state machine wait
PHY_RX_CAL_OVERRIDE_0	8	0x0	0x0-0x1	Manual setting of RX Calibration
SC_PHY_RX_CAL_START_0	0	0x0	0x0-0x1	Manual RX Calibration start for

DENALI_PHY_53 (Address PHY_BASE_ADDR + 53)



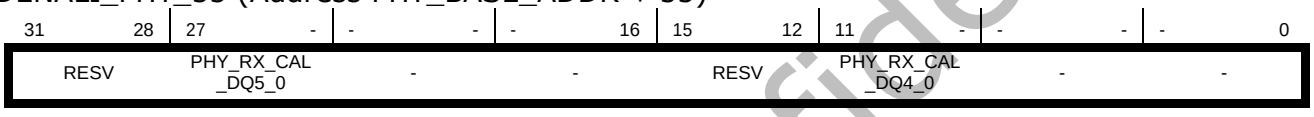
Name	Bits	Default	Range	Description
PHY_RX_CAL_DQ1_0	27:16	0x000	0x0-0xfff	RX Calibration codes for DQ1 for slice 0. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits
PHY_RX_CAL_DQ0_0	11:0	0x000	0x0-0xfff	RX Calibration codes for DQ0 for slice 0. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits

DENALI_PHY_54 (Address PHY_BASE_ADDR + 54)



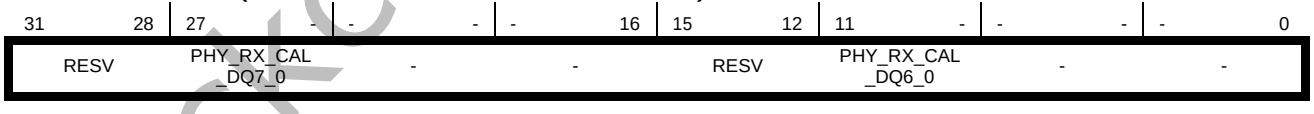
Name	Bits	Default	Range	Description
PHY_RX_CAL_DQ3_0	27:16	0x000	0x0-0xfff	RX Calibration codes for DQ3 for slice 0. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits
PHY_RX_CAL_DQ2_0	11:0	0x000	0x0-0xfff	RX Calibration codes for DQ2 for slice 0. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits

DENALI_PHY_55 (Address PHY_BASE_ADDR + 55)



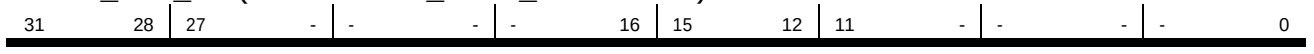
Name	Bits	Default	Range	Description
PHY_RX_CAL_DQ5_0	27:16	0x000	0x0-0xfff	RX Calibration codes for DQ5 for slice 0. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits
PHY_RX_CAL_DQ4_0	11:0	0x000	0x0-0xfff	RX Calibration codes for DQ4 for slice 0. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits

DENALI_PHY_56 (Address PHY_BASE_ADDR + 56)



Name	Bits	Default	Range	Description
PHY_RX_CAL_DQ7_0	27:16	0x000	0x0-0xfff	RX Calibration codes for DQ7 for slice 0. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits
PHY_RX_CAL_DQ6_0	11:0	0x000	0x0-0xfff	RX Calibration codes for DQ6 for slice 0. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits

DENALI_PHY_57 (Address PHY_BASE_ADDR + 57)



RESV	PHY_RX_CAL _DQS_0	-	-	RESV	PHY_RX_CAL _DM_0	-	-

Name	Bits	Default	Range	Description
PHY_RX_CAL_DQS_0	27:16	0x000	0x0-0xfff	RX Calibration codes for DQS for slice 0. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits
PHY_RX_CAL_DM_0	11:0	0x000	0x0-0xfff	RX Calibration codes for DM for slice 0. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits

DENALI_PHY_58 (Address PHY_BASE_ADDR + 58)

31	27	26	-	-	-	-	16	15	12	11	-	-	-	-	0
RESV		PHY_RX_CAL _OBS_0		-		-		RESV		PHY_RX_CAL _FDBK_0		-		-	

Name	Bits	Default	Range	Description
PHY_RX_CAL_OBS_0	26:16	0x000	0x0-0x7ff	RX Calibration results for slice 0. Bits (7:0) contain calibration results from DQ0-7. Bit (8) contains calibration result from DM. Bit (9)
PHY_RX_CAL_FDBK_0	11:0	0x000	0x0-0xfff	RX Calibration codes for FDBK for slice 0. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits

DENALI_PHY_59 (Address PHY_BASE_ADDR + 59)

31	27	26	-	-	-	-	16	15	11	10	-	-	-	-	0
RESV		PHY_CLK_WR DQ1_SLAVE		-		-		RESV		PHY_CLK_WR DQ0_SLAVE		-		-	

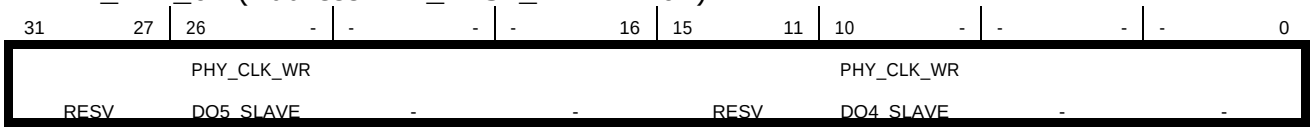
Name	Bits	Default	Range	Description
PHY_CLK_WRDQ1_SLAVE_DELAY_0	26:16	0x000	0x0-0x7ff	Write clock slave delay setting for
PHY_CLK_WRDQ0_SLAVE_DELAY_0	10:0	0x000	0x0-0x7ff	Write clock slave delay setting for

DENALI_PHY_60 (Address PHY_BASE_ADDR + 60)

31	27	26	-	-	-	-	16	15	11	10	-	-	-	-	0
RESV		PHY_CLK_WR DQ3_SLAVE		-		-		RESV		PHY_CLK_WR DQ2_SLAVE		-		-	

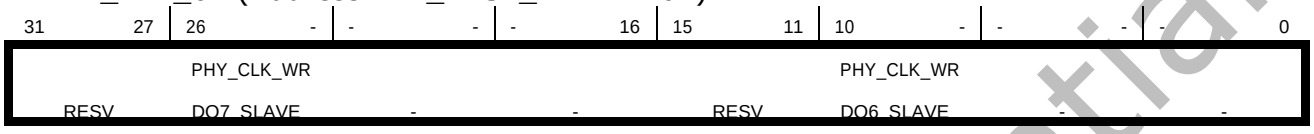
Name	Bits	Default	Range	Description
PHY_CLK_WRDQ3_SLAVE_DELAY_0	26:16	0x000	0x0-0x7ff	Write clock slave delay setting for
PHY_CLK_WRDQ2_SLAVE_DELAY_0	10:0	0x000	0x0-0x7ff	Write clock slave delay setting for

DENALI_PHY_61 (Address PHY_BASE_ADDR + 61)



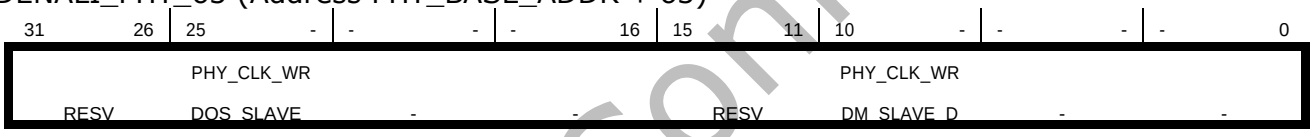
Name	Bits	Default	Range	Description
PHY_CLK_WRDQ5_SLAVE_DELAY_0	26:16	0x000	0x0-0x7ff	Write clock slave delay setting for
PHY_CLK_WRDQ4_SLAVE_DELAY_0	10:0	0x000	0x0-0x7ff	Write clock slave delay setting for

DENALI_PHY_62 (Address PHY_BASE_ADDR + 62)



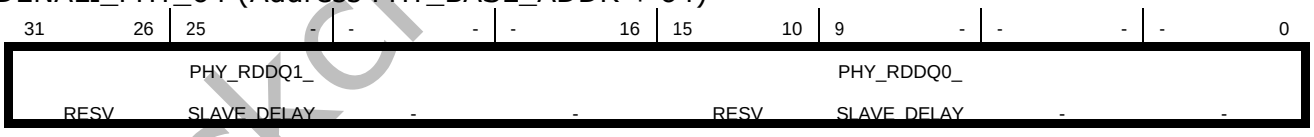
Name	Bits	Default	Range	Description
PHY_CLK_WRDQ7_SLAVE_DELAY_0	26:16	0x000	0x0-0x7ff	Write clock slave delay setting for
PHY_CLK_WRDQ6_SLAVE_DELAY_0	10:0	0x000	0x0-0x7ff	Write clock slave delay setting for

DENALI_PHY_63 (Address PHY_BASE_ADDR + 63)



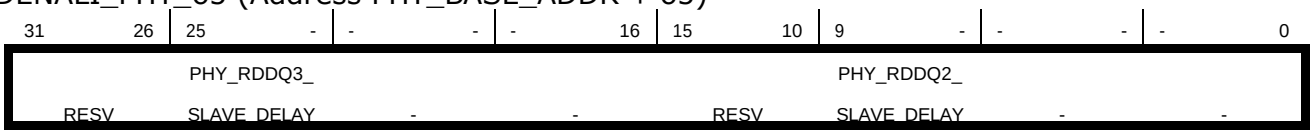
Name	Bits	Default	Range	Description
PHY_CLK_WRDQS_SLAVE_DELAY_0	25:16	0x000	0x0-0x3ff	Write clock slave delay setting for
PHY_CLK_WRDM_SLAVE_DELAY_0	10:0	0x000	0x0-0x7ff	Write clock slave delay setting for

DENALI_PHY_64 (Address PHY_BASE_ADDR + 64)



Name	Bits	Default	Range	Description
PHY_RDDQ1_SLAVE_DELAY_0	25:16	0x000	0x0-0x3ff	Read DQ1 slave delay setting for
PHY_RDDQ0_SLAVE_DELAY_0	9:0	0x000	0x0-0x3ff	Read DQ0 slave delay setting for

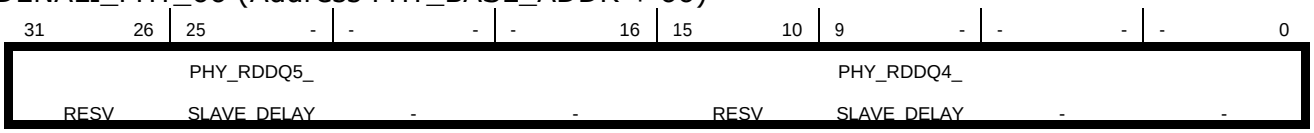
DENALI_PHY_65 (Address PHY_BASE_ADDR + 65)



Name	Bits	Default	Range	Description
PHY_RDDQ3_SLAVE_DELAY_0	25:16	0x000	0x0-0x3ff	Read DQ3 slave delay setting for

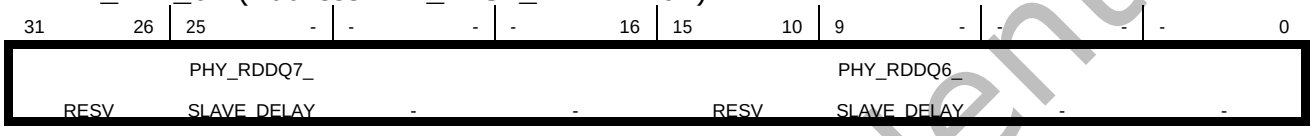
PHY_RDDQ2_SLAVE_DELAY_0	9:0	0x000	0x0-0x3ff	Read DQ2 slave delay setting for

DENALI_PHY_66 (Address PHY_BASE_ADDR + 66)



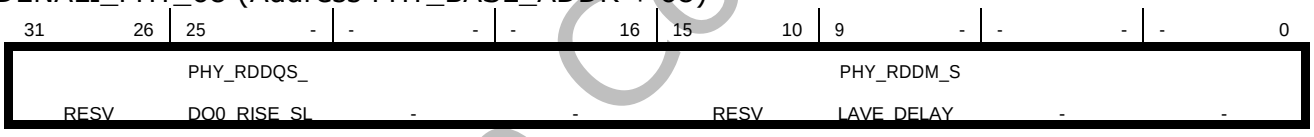
Name	Bits	Default	Range	Description
PHY_RDDQ5_SLAVE_DELAY_0	25:16	0x000	0x0-0x3ff	Read DQ5 slave delay setting for
PHY_RDDQ4_SLAVE_DELAY_0	9:0	0x000	0x0-0x3ff	Read DQ4 slave delay setting for

DENALI_PHY_67 (Address PHY_BASE_ADDR + 67)



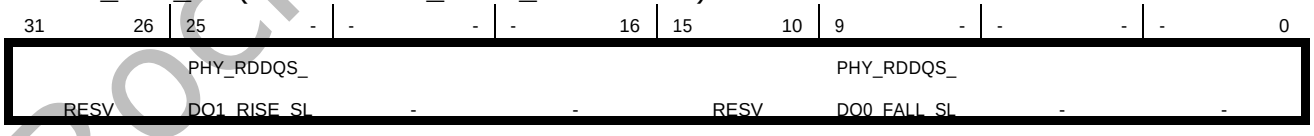
Name	Bits	Default	Range	Description
PHY_RDDQ7_SLAVE_DELAY_0	25:16	0x000	0x0-0x3ff	Read DQ7 slave delay setting for
PHY_RDDQ6_SLAVE_DELAY_0	9:0	0x000	0x0-0x3ff	Read DQ6 slave delay setting for

DENALI_PHY_68 (Address PHY_BASE_ADDR + 68)



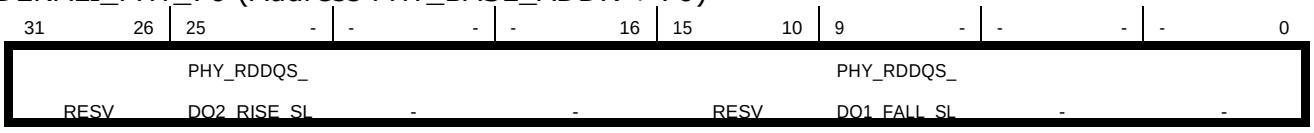
Name	Bits	Default	Range	Description
PHY_RDDQS_DQ0_RISE_SLAVE_DELAY_	25:16	0x000	0x0-0x3ff	Rising edge read DQS slave delay
PHY_RDDM_SLAVE_DELAY_0	9:0	0x000	0x0-0x3ff	Read DM/DBI slave delay setting for slice 0. May be used for data

DENALI_PHY_69 (Address PHY_BASE_ADDR + 69)



Name	Bits	Default	Range	Description
PHY_RDDQS_DQ1_RISE_SLAVE_DELAY_	25:16	0x000	0x0-0x3ff	Rising edge read DQS slave delay
PHY_RDDQS_DQ0_FALL_SLAVE_DELAY_	9:0	0x000	0x0-0x3ff	Falling edge read DQS slave delay

DENALI_PHY_70 (Address PHY_BASE_ADDR + 70)



Name	Bits	Default	Range	Description
PHY_RDDQS_DQ2_RISE_SLAVE_DELAY_	25:16	0x000	0x0-0x3ff	Rising edge read DQS slave delay
PHY_RDDQS_DQ1_FALL_SLAVE_DELAY_	9:0	0x000	0x0-0x3ff	Falling edge read DQS slave delay

DENALI_PHY_71 (Address PHY_BASE_ADDR + 71)

31	26	25	-	-	-	16	15	10	9	-	-	-	0
RESV		PHY_RDDQS_DQ3_RISE_SL		-	-		RESV		PHY_RDDQS_DQ2_FALL_SL		-	-	

Name	Bits	Default	Range	Description
PHY_RDDQS_DQ3_RISE_SLAVE_DELAY_	25:16	0x000	0x0-0x3ff	Rising edge read DQS slave delay
PHY_RDDQS_DQ2_FALL_SLAVE_DELAY_	9:0	0x000	0x0-0x3ff	Falling edge read DQS slave delay

DENALI_PHY_72 (Address PHY_BASE_ADDR + 72)

31	26	25	-	-	-	16	15	10	9	-	-	-	0
RESV		PHY_RDDQS_DQ4_RISE_SL		-	-		RESV		PHY_RDDQS_DQ3_FALL_SL		-	-	

Name	Bits	Default	Range	Description
PHY_RDDQS_DQ4_RISE_SLAVE_DELAY_	25:16	0x000	0x0-0x3ff	Rising edge read DQS slave delay
PHY_RDDQS_DQ3_FALL_SLAVE_DELAY_	9:0	0x000	0x0-0x3ff	Falling edge read DQS slave delay

DENALI_PHY_73 (Address PHY_BASE_ADDR + 73)

31	26	25	-	-	-	16	15	10	9	-	-	-	0
RESV		PHY_RDDQS_DQ5_RISE_SL		-	-		RESV		PHY_RDDQS_DQ4_FALL_SL		-	-	

Name	Bits	Default	Range	Description
PHY_RDDQS_DQ5_RISE_SLAVE_DELAY_	25:16	0x000	0x0-0x3ff	Rising edge read DQS slave delay
PHY_RDDQS_DQ4_FALL_SLAVE_DELAY_	9:0	0x000	0x0-0x3ff	Falling edge read DQS slave delay

DENALI_PHY_74 (Address PHY_BASE_ADDR + 74)

31	26	25	-	-	-	16	15	10	9	-	-	-	0
RESV		PHY_RDDQS_DQ6_RISE_SL		-	-		RESV		PHY_RDDQS_DQ5_FALL_SL		-	-	

Name	Bits	Default	Range	Description
PHY_RDDQS_DQ6_RISE_SLAVE_DELAY_	25:16	0x000	0x0-0x3ff	Rising edge read DQS slave delay
PHY_RDDQS_DQ5_FALL_SLAVE_DELAY_	9:0	0x000	0x0-0x3ff	Falling edge read DQS slave delay

DENALI_PHY_75 (Address PHY_BASE_ADDR + 75)

31	26	25	-	-	-	16	15	10	9	-	-	-	0

RESV	PHY_RDDQS_DQ7_RISE_SL	-	-	RESV	PHY_RDDQS_DQ6_FALL_SL	-	-

Name	Bits	Default	Range	Description
PHY_RDDQS_DQ7_RISE_SLAVE_DELAY_	25:16	0x000	0x0-0x3ff	Rising edge read DQS slave delay
PHY_RDDQS_DQ6_FALL_SLAVE_DELAY_	9:0	0x000	0x0-0x3ff	Falling edge read DQS slave delay

DENALI_PHY_76 (Address PHY_BASE_ADDR + 76)

31	26	25	-	-	-	-	16	15	10	9	-	-	-	-	0

RESV	PHY_RDDQS_DM_RISE_SLA	-	-	RESV	PHY_RDDQS_DQ7_FALL_SL	-	-

Name	Bits	Default	Range	Description
PHY_RDDQS_DM_RISE_SLAVE_DELAY_0	25:16	0x000	0x0-0x3ff	Rising edge read DQS slave delay
PHY_RDDQS_DQ7_FALL_SLAVE_DELAY_	9:0	0x000	0x0-0x3ff	Falling edge read DQS slave delay

DENALI_PHY_77 (Address PHY_BASE_ADDR + 77)

31	26	25	-	-	-	-	16	15	10	9	-	-	-	-	0

RESV	PHY_RDDQS_GATE_SLAVE	-	-	RESV	PHY_RDDQS_DM_FALL_SLA	-	-

Name	Bits	Default	Range	Description
PHY_RDDQS_GATE_SLAVE_DELAY_0	25:16	0x000	0x0-0x3ff	Read DQS slave delay setting for
PHY_RDDQS_DM_FALL_SLAVE_DELAY_0	9:0	0x000	0x0-0x3ff	Falling edge read DQS slave delay

DENALI_PHY_78 (Address PHY_BASE_ADDR + 78)

31	26	25	-	-	-	-	16	15	11	10	8	7	4	3	0

RESV	PHY_WRLVL_DELAY_EARLY_THRESHOLD_0	-	-	RESV	PHY_WRITE_PATH_LAT_AD_0	RESV	PHY_RDDQS_LATENCY_AD_0

Name	Bits	Default	Range	Description
PHY_WRLVL_DELAY_EARLY_THRESHOLD_0	25:16	0x000	0x0-0x3ff	Write level delay threshold above which will be considered in
PHY_WRITE_PATH_LAT_ADD_0	10:8	0x0	0x0-0x7	Number of cycles to delay the incoming dfi_wrdata_en/dfi_wrdata
PHY_RDDQS_LATENCY_ADJUST_0	3:0	0x0	0x0-0xf	Number of cycles to delay the incoming dfi_rddata_en for read

DENALI_PHY_79 (Address PHY_BASE_ADDR + 79)

31	-	-	24	23	17	16	16	15	10	9	-	-	-	-	0

OBSOLETE	-	RESV	PHY_WRLVL_EARLY_FORC	RESV	PHY_WRLVL_DELAY_PERIO	-	-

Name	Bits	Default	Range	Description

PHY_WRLVL_EARLY_FORCE_ZERO_0	16	0x0	0x0-0x1	Force the final write level delay value (that meets the early
PHY_WRLVL_DELAY_PERIOD_THRESHOLD_0	9:0	0x000	0x0-0x3ff	Write level delay threshold below which will add a cycle of write path

DENALI_PHY_80 (Address PHY_BASE_ADDR + 80)

31 -	- 24	23 20	19 16	15 10	9 -	- -	- 0
OBSOLETE	-	RESV	PHY_GTLVL_LAT_ADJ_STAR	RESV	PHY_GTLVL_RDDQS_SLV_D	-	-

Name	Bits	Default	Range	Description
PHY_GTLVL_LAT_ADJ_START_0	19:16	0x0	0x0-0xf	Initial read DQS gate cycle delay from dfi_rddata_en during gate
PHY_GTLVL_RDDQS_SLV_DLY_START_0	9:0	0x000	0x0-0x3ff	Initial read DQS gate slave delay setting during gate training for slice

DENALI_PHY_81 (Address PHY_BASE_ADDR + 81)

31 26	25 -	- -	- 16	15 11	10 -	- -	- 0
RESV	PHY_RDLVL_RDDQS_DQ_S	-	-	RESV	PHY_WDQLVL_DQDM_SLV_	-	-

Name	Bits	Default	Range	Description
PHY_RDLVL_RDDQS_DQ_SLV_DLY_START_0	25:16	0x000	0x0-0x3ff	Read leveling starting value for the DQS/DQ slave delay settings for
PHY_WDQLVL_DQDM_SLV_DLY_START_0	10:0	0x000	0x0-0x7ff	Initial DQ/DM slave delay setting during write data leveling for slice

DENALI_PHY_82 (Address PHY_BASE_ADDR + 82)

31 -	- -	- -	- -	- -	- 8	7 2	1 0
OBSOLETE	-	-	-	-	-	RESV	RESERVED

Name	Bits	Default	Range	Description
RESERVED	1:0	0x0	0x0-0x3	Reserved for future use. Refer to the regconfig files for the default

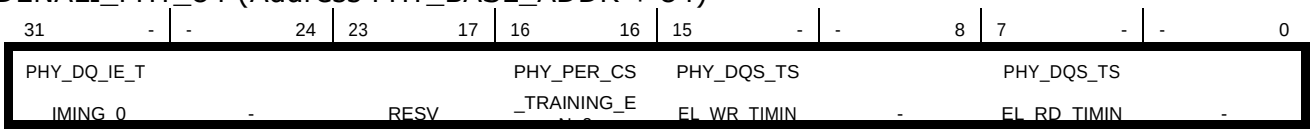
DENALI_PHY_83 (Address PHY_BASE_ADDR + 83)

31 -	- 24	23 -	- 16	15 -	- 8	7 -	- 0
PHY_DQS_OE_TIMING_0	-	PHY_DQ_TSEL_WR_TIMING	-	PHY_DQ_TSEL_RD_TIMING	-	PHY_DQ_OE_TIMING_0	-

Name	Bits	Default	Range	Description
PHY_DQS_OE_TIMING_0	31:24	0x00	0x0-0xff	Start/end timing values for DQS
PHY_DQ_TSEL_WR_TIMING_0	23:16	0x00	0x0-0xff	Start/end timing values for DQ/DM write based termination enable and
PHY_DQ_TSEL_RD_TIMING_0	15:8	0x00	0x0-0xff	Start/end timing values for DQ/DM read based termination enable and

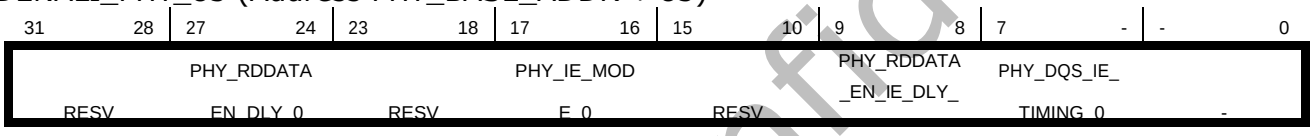
PHY_DQ_OE_TIMING_0	7:0	0x00	0x0-0xff	Start/end timing values for DQ/DM

DENALI_PHY_84 (Address PHY_BASE_ADDR + 84)



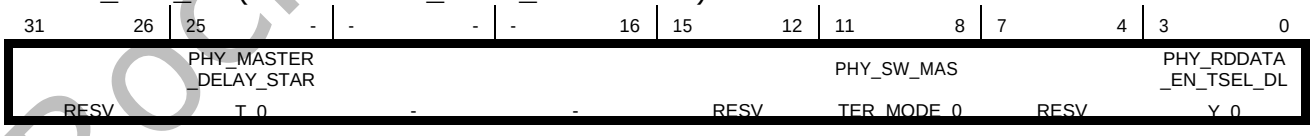
Name	Bits	Default	Range	Description
PHY_DQ_IE_TIMING_0	31:24	0x00	0x0-0xff	Start/end timing values for DQ/DM
PHY_PER_CS_TRAINING_EN_0	16	0x0	0x0-0x1	Enables the per-rank training and read/write timing capabilities. Must
PHY_DQS_TSEL_WR_TIMING_0	15:8	0x00	0x0-0xff	Start/end timing values for DQS write based termination enable and
PHY_DQS_TSEL_RD_TIMING_0	7:0	0x00	0x0-0xff	Start/end timing values for DQS read based termination enable and

DENALI_PHY_85 (Address PHY_BASE_ADDR + 85)



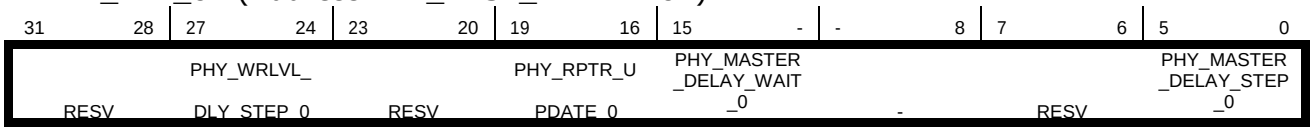
Name	Bits	Default	Range	Description
PHY_RDDATA_EN_DLY_0	27:24	0x0	0x0-0xf	Number of cycles that the dfi_rddata_en signal is early for
PHY_IE_MODE_0	17:16	0x0	0x0-0x3	Input enable mode bits for slice 0. Bit (0) enables the mode where the input enables are always on; set to
PHY_RDDATA_EN_IE_DLY_0	9:8	0x0	0x0-0x3	Number of cycles that the dfi_rddata_en signal is earlier than
PHY_DQS_IE_TIMING_0	7:0	0x00	0x0-0xff	Start/end timing values for DQS

DENALI_PHY_86 (Address PHY_BASE_ADDR + 86)



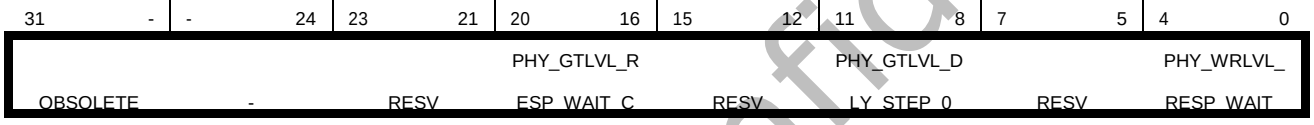
Name	Bits	Default	Range	Description
PHY_MASTER_DELAY_START_0	25:16	0x000	0x0-0x3ff	Start value for master delay line
PHY_SW_MASTER_MODE_0	11:8	0x0	0x0-0xf	Master delay line override settings for slice 0. Bit (0) enables software half clock mode. Bit (1) is the software half clock mode value. Bit
PHY_RDDATA_EN_TSEL_DLY_0	3:0	0x0	0x0-0xf	Number of cycles that the dfi_rddata_en signal is earlier than

DENALI_PHY_87 (Address PHY_BASE_ADDR + 87)



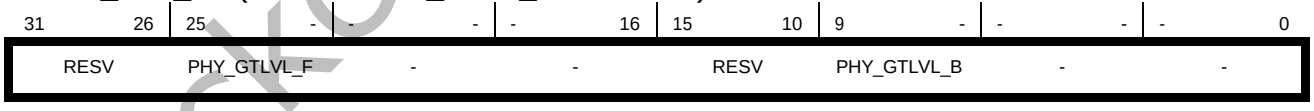
Name	Bits	Default	Range	Description
PHY_WRLVL_DLY_STEP_0	27:24	0x0	0x0-0xf	DQS slave delay step size during
PHY_RPTR_UPDATE_0	19:16	0x0	0x0-0xf	Offset in cycles from the dfi_rddata_en signal to release
PHY_MASTER_DELAY_WAIT_0	15:8	0x00	0x0-0xff	Wait cycles for master delay line locking algorithm for slice 0. Bits (3:0) are the cycle wait count after a calibration clock setting change.
PHY_MASTER_DELAY_STEP_0	5:0	0x00	0x0-0x3f	Incremental step size for master delay line locking algorithm for slice

DENALI_PHY_88 (Address PHY_BASE_ADDR + 88)



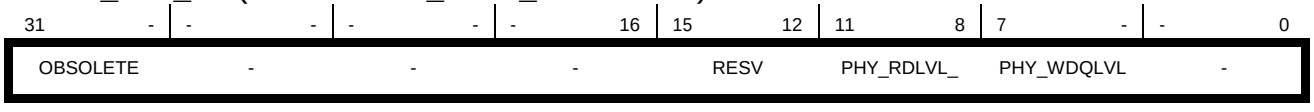
Name	Bits	Default	Range	Description
PHY_GTLVL_RESP_WAIT_CNT_0	20:16	0x00	0x0-0x1f	Number of cycles + 4 to wait between dfi_rddata_en and the sampling of the DQS during gate
PHY_GTLVL_DLY_STEP_0	11:8	0x0	0x0-0xf	DQS slave delay step size during
PHY_WRLVL_RESP_WAIT_CNT_0	4:0	0x00	0x0-0x1f	Number of cycles to wait between dfi_wrlvl_strobe and the sampling

DENALI_PHY_89 (Address PHY_BASE_ADDR + 89)



Name	Bits	Default	Range	Description
PHY_GTLVL_FINAL_STEP_0	25:16	0x000	0x0-0x3ff	Final backup step delay used in
PHY_GTLVL_BACK_STEP_0	9:0	0x000	0x0-0x3ff	Interim backup step delay used in

DENALI_PHY_90 (Address PHY_BASE_ADDR + 90)



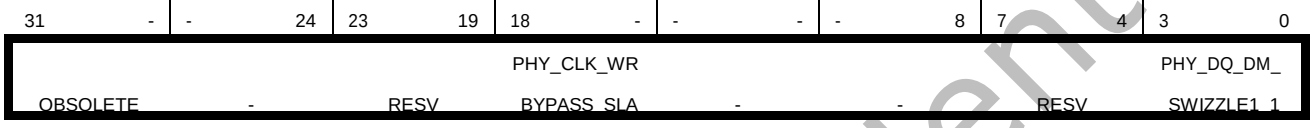
Name	Bits	Default	Range	Description
PHY_RDLVL_DLY_STEP_0	11:8	0x0	0x0-0xf	DQS slave delay step size during

PHY_WDQLVL_DLY_STEP_0	7:0	0x00	0x0-0xff	DQ slave delay step size during

DENALI_PHY_128 (Address PHY_BASE_ADDR + 128)

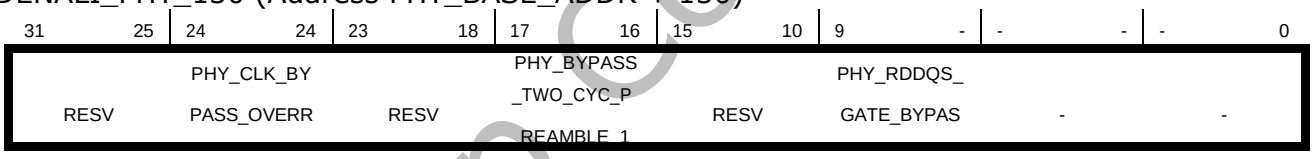
Name	Bits	Default	Range	Description
PHY_DQ_DM_SWIZZLE0_1	31:0	0x00000000	0x0-0xffffffff	DO/DM bit swizzling 0 for slice 1. Bits (3:0) inform the PHY which bit in {DM,DQ} map to DQ0. Bits (7:4) {DM,DQ} map to DQ1, etc.

DENALI_PHY_129 (Address PHY_BASE_ADDR + 129)



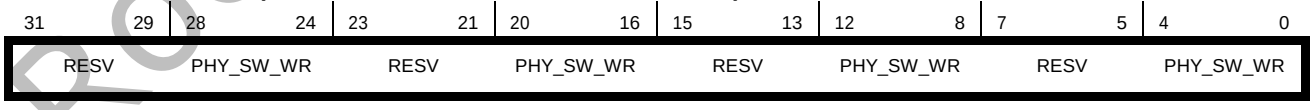
Name	Bits	Default	Range	Description
PHY_CLK_WR_BYPASS_SLAVE_DELAY_1	18:8	0x000	0x0-0x7ff	Write data clock bypass mode
PHY_DQ_DM_SWIZZLE1_1	3:0	0x0	0x0-0xf	DQ/DM bit swizzling 1 for slice 1. Bits (3:0) inform the PHY which bit

DENALI_PHY_130 (Address PHY_BASE_ADDR + 130)



Name	Bits	Default	Range	Description
PHY_CLK_BYPASS_OVERRIDE_1	24	0x0	0x0-0x1	Bypass mode override setting for
PHY_BYPASS_TWO_CYC_PREAMBLE_1	17:16	0x0	0x0-0x3	PHY two_cycle_preamble for
PHY_RDDQS_GATE_BYPASS_SLAVE_DE	9:0	0x000	0x0-0x3ff	Read DQS bypass mode slave

DENALI_PHY_131 (Address PHY_BASE_ADDR + 131)



Name	Bits	Default	Range	Description
PHY_SW_WRDQ3_SHIFT_1	28:24	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for write DQ3 for slice 1. Bit (0) enables override of half_cycle_shift. Bit (1)
PHY_SW_WRDQ2_SHIFT_1	20:16	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for write DQ2 for slice 1. Bit (0) enables override of half_cycle_shift. Bit (1)

PHY_SW_WRDQ1_SHIFT_1	12:8	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for write DQ1 for slice 1. Bit (0) enables override of half_cycle_shift. Bit (1)
PHY_SW_WRDQ0_SHIFT_1	4:0	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for write DQ0 for slice 1. Bit (0) enables override of half_cycle_shift. Bit (1)

DENALI_PHY_132 (Address PHY_BASE_ADDR + 132)

31 29	28 24	23 21	20 16	15 13	12 8	7 5	4 0
RESV	PHY_SW_WR	RESV	PHY_SW_WR	RESV	PHY_SW_WR	RESV	PHY_SW_WR

Name	Bits	Default	Range	Description
PHY_SW_WRDQ7_SHIFT_1	28:24	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for write DQ7 for slice 1. Bit (0) enables override of half_cycle_shift. Bit (1)
PHY_SW_WRDQ6_SHIFT_1	20:16	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for write DQ6 for slice 1. Bit (0) enables override of half_cycle_shift. Bit (1)
PHY_SW_WRDQ5_SHIFT_1	12:8	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for write DQ5 for slice 1. Bit (0) enables override of half_cycle_shift. Bit (1)
PHY_SW_WRDQ4_SHIFT_1	4:0	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for write DQ4 for slice 1. Bit (0) enables override of half_cycle_shift. Bit (1)

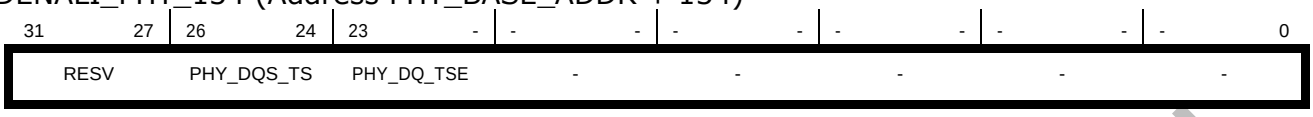
DENALI_PHY_133 (Address PHY_BASE_ADDR + 133)

31 -	- 24	23 19	18 16	15 12	11 8	7 5	4 0
OBSOLETE	-	RESV	PHY_DQ_TSE	RESV	PHY_SW_WR	RESV	PHY_SW_WR

Name	Bits	Default	Range	Description
PHY_DQ_TSEL_ENABLE_1	18:16	0x0	0x0-0x7	Operation type tsel enables for DQ/DM signals for slice 1. Bit (0) enables tsel_en during read cycles. Bit (1) enables tsel_en during write
PHY_SW_WRDQS_SHIFT_1	11:8	0x0	0x0-0xf	Manual override of automatic half_cycle_shift/cycle_shift for write DQS for slice 1. Bit (0) enables override of half_cycle_shift. Bit (1)

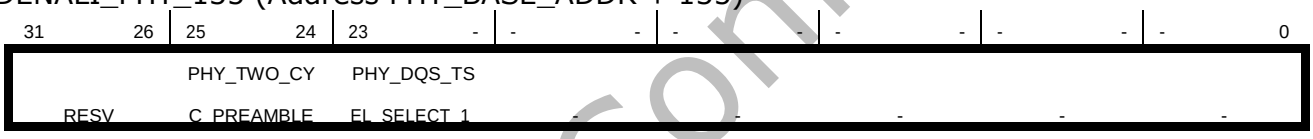
PHY_SW_WRDM_SHIFT_1	4:0	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for write DM for slice 1. Bit (0) enables override of half_cycle_shift. Bit (1)

DENALI_PHY_134 (Address PHY_BASE_ADDR + 134)



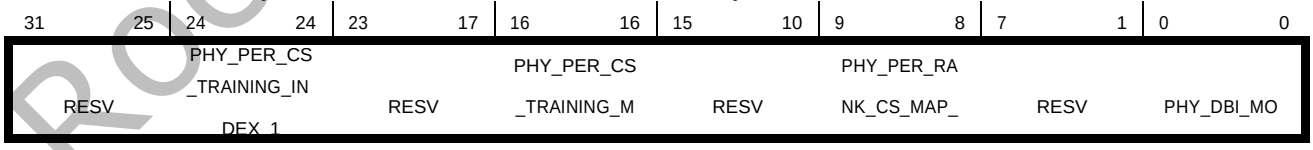
Name	Bits	Default	Range	Description
PHY_DQS_TSEL_ENABLE_1	26:24	0x0	0x0-0x7	Operation type tsel enables for DQS signals for slice 1. Bit (0) enables tsel_en during read cycles. Bit (1) enables tsel_en during write
PHY_DQ_TSEL_SELECT_1	23:0	0x000000	0x0-0xffffff	Operation type tsel select values for DQ/DM signals for slice 1. Bits (3:0) are tsel_sel values during read cycles. Bits (7:4) are tsel_sel

DENALI_PHY_135 (Address PHY_BASE_ADDR + 135)



Name	Bits	Default	Range	Description
PHY_TWO_CYC_PREAMBLE_1	25:24	0x0	0x0-0x3	2 cycle preamble support for slice 1. Bit (0) controls the 2 cycle read preamble. Bit (1) controls the 2
PHY_DQS_TSEL_SELECT_1	23:0	0x000000	0x0-0xffffff	Operation type tsel select values for DQS signals for slice 1. Bits (3:0) are tsel_sel values during read cycles. Bits (7:4) are tsel_sel

DENALI_PHY_136 (Address PHY_BASE_ADDR + 136)



Name	Bits	Default	Range	Description
PHY_PER_CS_TRAINING_INDEX_1	24	0x0	0x0-0x1	For per-rank training, indicates which ranksparamtersareread/
PHY_PER_CS_TRAINING_MULTICAST_EN_1	16	0x1	0x0-0x1	When set, a register write will update parameters for all ranks at
PHY_PER_RANK_CS_MAP_1	9:8	0x0	0x0-0x3	Per-rank CS map for slice 1.
PHY_DBI_MODE_1	0	0x0	0x0-0x1	DBI mode for slice 1. Bit (0) enables return of DBI read data. Bit

DENALI_PHY_137 (Address PHY_BASE_ADDR + 137)

31 28	27 24	23 20	19 16	15 12	11 8	7 2	1 0
RESV	PHY_LP4_BOOT_RPTR_UP	RESV	PHY_LP4_BOOT_RDDATA_	RESV	PHY_LP4_BOOT_RDDATA_	RESV	PHY_LP4_BOOT_RDDATA_

Name	Bits	Default	Range	Description
PHY_LP4_BOOT_RPTR_UPDATE_1	27:24	0x0	0x0-0xf	For LPDDR4 boot frequency, the offset in cycles from the
PHY_LP4_BOOT_RDDATA_EN_TSEL_DLY_1	19:16	0x0	0x0-0xf	For LPDDR4 boot frequency, the number of cycles that the dfi_rddata_en signal is earlier than
PHY_LP4_BOOT_RDDATA_EN_DLY_1	11:8	0x0	0x0-0xf	For LPDDR4 boot frequency, the number of cycles that the
PHY_LP4_BOOT_RDDATA_EN_IE_DLY_1	1:0	0x0	0x0-0x3	For LPDDR4 boot frequency, the number of cycles that the dfi_rddata_en signal is earlier than

DENALI_PHY_138 (Address PHY_BASE_ADDR + 138)

31 -	- 24	23 17	16 16	15 15	14 8	7 4	3 0
OBSOLETE	-	RESV	PHY_SLICE_PWR_RDC_DIS	RESV	PHY_LPBK_C	RESV	PHY_LP4_BOOT_RDDQS_L

Name	Bits	Default	Range	Description
PHY_SLICE_PWR_RDC_DISABLE_1	16	0x0	0x0-0x1	data slice power reduction disable
PHY_LPBK_CONTROL_1	14:8	0x00	0x0-0x7f	Loopback control bits for slice 1.
PHY_LP4_BOOT_RDDQS_LATENCY_ADJ	3:0	0x0	0x0-0xf	For LPDDR4 boot frequency, the number of cycles to delay the

DENALI_PHY_139 (Address PHY_BASE_ADDR + 139)

31 25	24 24	23 21	20 16	15 10	9 -	- -	- 0
RESV	SC_PHY_SNAP_OBS_REGS_1	RESV	PHY_GATE_ERROR_DELAY_SELECT_1	RESV	PHY_RDDQS_DQ_BYPASS_	-	-

Name	Bits	Default	Range	Description
SC_PHY_SNAP_OBS_REGS_1	24	0x0	0x0-0x1	Initiates a snapshot of the internal observation registers for slice 1.
PHY_GATE_ERROR_DELAY_SELECT_1	20:16	0x00	0x0-0x1f	Number of cycles to wait for the DQS gate to close before flagging
PHY_RDDQS_DQ_BYPASS_SLAVE_DELAY_1	9:0	0x000	0x0-0x3ff	Read DQS data clock bypass mode

DENALI_PHY_140 (Address PHY_BASE_ADDR + 140)

31 25	24 -	- -	- 16	15 10	9 8	7 1	0 0

	PHY_GATE_S				PHY_LPDDR_		PHY_LPDDR_
RESV	MPL1_SLAVE	-	-	RESV	TYPE_1	RESV	1

Name	Bits	Default	Range	Description
PHY_GATE_SMPL1_SLAVE_DELAY_1	24:16	0x000	0x0-0x1ff	Number of cycles to delay the read DQS gate signal to generate gate1
PHY_LPDDR_TYPE_1	9:8	0x0	0x0-0x3	Indicates the type of DRAM for slice 1. Clear to 0 for DDR3 or
PHY_LPDDR_1	0	0x0	0x0-0x1	Indicates a cycle of delay for the

DENALI_PHY_141 (Address PHY_BASE_ADDR + 141)

31	-	-	24	23	18	17	16	15	9	8	-	-	-	-	0
						ON_FLY_GAT				PHY_GATE_S					
OBSOLETE		-		RESV		E_ADJUST_E		RESV		MPL2_SLAVE		-		-	

Name	Bits	Default	Range	Description
ON_FLY_GATE_ADJUST_EN_1	17:16	0x0	0x0-0x3	Control the on the fly gate
PHY_GATE_SMPL2_SLAVE_DELAY_1	8:0	0x000	0x0-0x1ff	Number of cycles to delay the read DQS gate signal to generate gate2

DENALI_PHY_142 (Address PHY_BASE_ADDR + 142)

31	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0
PHY_GATE_T															
RACKING_OB		-		-		-		-		-		-		-	

Name	Bits	Default	Range	Description
PHY_GATE_TRACKING_OBS_1	31:0	0x00000000	0x0-0xffffffff	Report the on the fly gate

DENALI_PHY_143 (Address PHY_BASE_ADDR + 143)

31	-	-	-	-	-	-	16	15	10	9	8	7	1	0	0
OBSOLETE		-		-		-		RESV		PHY_LP4_PST_AMBLE_1		RESV		PHY_DFI40_P	

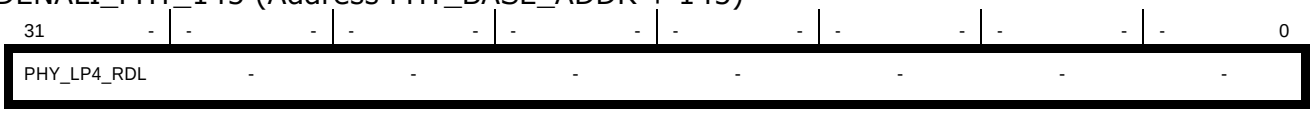
Name	Bits	Default	Range	Description
PHY_LP4_PST_AMBLE_1	9:8	0x0	0x0-0x3	Controls the read postamble
PHY_DFI40_POLARITY_1	0	0x0	0x0-0x1	Indicates the dfi_wrdata_cs_n and dfi_rddata_cs_n is low active or

DENALI_PHY_144 (Address PHY_BASE_ADDR + 144)

31	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0
PHY_LP4_RDL		-		-		-		-		-		-		-	

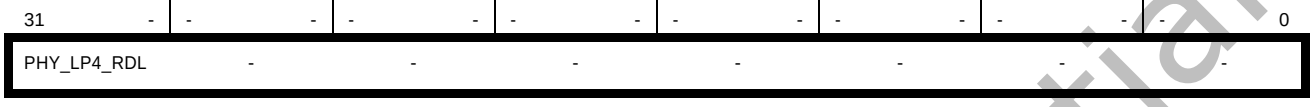
Name	Bits	Default	Range	Description
PHY_LP4_RDLVL_PATT8_1	31:0	0x00000000	0x0-0xffffffff	LPDDR4 read leveling pattern 8

DENALI_PHY_145 (Address PHY_BASE_ADDR + 145)



Name	Bits	Default	Range	Description
PHY_LP4_RDLVL_PATT9_1	31:0	0x000000	0x0-0xffffffff	LPDDR4 read leveling pattern 9

DENALI_PHY_146 (Address PHY_BASE_ADDR + 146)

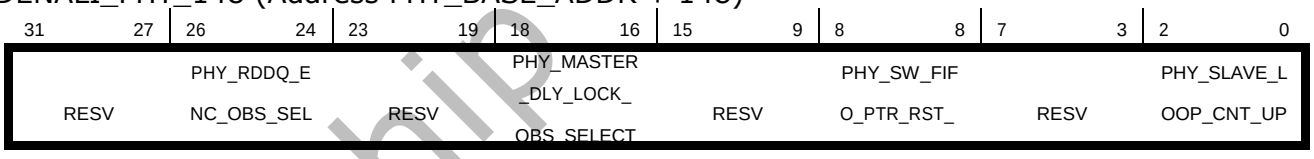


Name	Bits	Default	Range	Description
PHY_LP4_RDLVL_PATT10_1	31:0	0x000000	0x0-0xffffffff	LPDDR4 read leveling pattern 10

DENALI_PHY_147 (Address PHY_BASE_ADDR + 147)

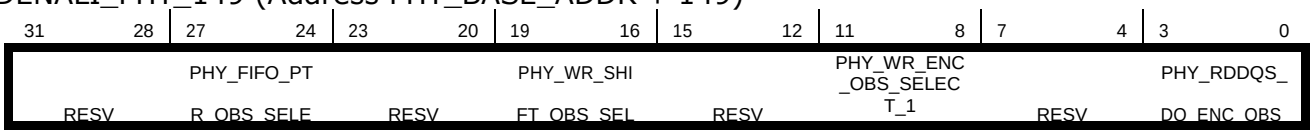
Name	Bits	Default	Range	Description
PHY_LP4_RDLVL_PATT11_1	31:0	0x00000000	0x0-0xffffffff	LPDDR4 read leveling pattern 11

DENALI_PHY_148 (Address PHY_BASE_ADDR + 148)



Name	Bits	Default	Range	Description
PHY_RDDQ_ENC_OBS_SELECT_1	26:24	0x0	0x0-0x7	Select value to map the internal read DQ slave delay encoded settings to the accessible read DQ
PHY_MASTER_DLY_LOCK_OBS_SELECT_1	18:16	0x0	0x0-0x7	Select value to map the internal master delay observation registers
PHY_SW_FIFO_PTR_RST_DISABLE_1	8	0x0	0x0-0x1	Disables automatic reset of the read entry FIFO pointers for slice 1.
PHY_SLAVE_LOOP_CNT_UPDATE_1	2:0	0x0	0x0-0x7	Sets the frequency by which the slave delay encoded value holding

DENALI_PHY_149 (Address PHY_BASE_ADDR + 149)



Name	Bits	Default	Range	Description
PHY_FIFO_PTR_OBS_SELECT_1	27:24	0x0	0x0-0xf	Select value to map the internal read entry FIFO read/write pointers to the accessible read entry FIFO
PHY_WR_SHIFT_OBS_SELECT_1	19:16	0x0	0x0-0xf	Select value to map the internal write DQ/DQS automatic cycle/ half_cycle shift settings to the
PHY_WR_ENC_OBS_SELECT_1	11:8	0x0	0x0-0xf	Select value to map the internal write DQ slave delay encoded settings to the accessible write DQ
PHY_RDDQS_DQ_ENC_OBS_SELECT_1	3:0	0x0	0x0-0xf	Select value to map the internal read DQS DQ rise/fall slave delay encoded settings to the accessible

DENALI_PHY_150 (Address PHY_BASE_ADDR + 150)

31 28	27 24	23 22	21 16	15 9	8 8	7 1	0 0
RESV	PHY_WRLVL_UPDT_WAIT	RESV	PHY_WRLVL_CAPTURE_CN	RESV	SC_PHY_LVL_DEBUG_CONT	RESV	PHY_LVL_DEBUG_MODE_1

Name	Bits	Default	Range	Description
PHY_WRLVL_UPDT_WAIT_CNT_1	27:24	0x0	0x0-0xf	Number of cycles to wait after changing DQS slave delay setting
PHY_WRLVL_CAPTURE_CNT_1	21:16	0x00	0x0-0x3f	Number of samples to take at each DQS slave delay setting during
SC_PHY_LVL_DEBUG_CONT_1	8	0x0	0x0-0x1	Allows the leveling state machine to advance (when in debug mode)
PHY_LVL_DEBUG_MODE_1	0	0x0	0x0-0x1	Enables leveling debug mode for

DENALI_PHY_151 (Address PHY_BASE_ADDR + 151)

31 28	27 24	23 22	21 16	15 12	11 8	7 6	5 0
RESV	PHY_RDLVL_UPDT_WAIT	RESV	PHY_RDLVL_CAPTURE_CN	RESV	PHY_GTLVL_UPDT_WAIT_C	RESV	PHY_GTLVL_CAPTURE_CNT

Name	Bits	Default	Range	Description
PHY_RDLVL_UPDT_WAIT_CNT_1	27:24	0x0	0x0-0xf	Number of cycles to wait after changing DQS slave delay setting
PHY_RDLVL_CAPTURE_CNT_1	21:16	0x00	0x0-0x3f	Number of samples to take at each DQS slave delay setting during
PHY_GTLVL_UPDT_WAIT_CNT_1	11:8	0x0	0x0-0xf	Number of cycles + 4 to wait after changing DQS slave delay setting
PHY_GTLVL_CAPTURE_CNT_1	5:0	0x00	0x0-0x3f	Number of samples to take at each DQS slave delay setting during

DENALI_PHY_152 (Address PHY_BASE_ADDR + 152)

31 30	29 24	23 -	- 16	15 13	12 8	7 2	1 0

RESV	PHY_WDQLVL_BURST_CNT_1	PHY_RDLVL_DATA_MASK_	-	RESV	PHY_RDLVL_RDDQS_DQ_	RESV	PHY_RDLVL_

Name	Bits	Default	Range	Description
PHY_WDQLVL_BURST_CNT_1	29:24	0x00	0x0-0x3f	Defines the write/read burst length in bytes during the write data
PHY_RDLVL_DATA_MASK_1	23:16	0x00	0x0-0xff	Per-bit mask for read leveling for slice 1. If all bits are not used, only
PHY_RDLVL_RDDQS_DQ_OBS_SELECT_1	12:8	0x00	0x0-0x1f	Select value to map an individual DQ data window leading/trailing edge to the leading/trailing edge
PHY_RDLVL_OP_MODE_1	1:0	0x0	0x0-0x3	Read leveling algorithm select for slice 1. Clear to 0 to move linearly from left to right. Set to 1 to start

DENALI_PHY_153 (Address PHY_BASE_ADDR + 153)

31 28	27 24	23 19	18 -	- -	- 8	7 3	2 0
RESV	PHY_WDQLVL_UPDT_WAIT_	RESV	PHY_WDQLVL_DQDM_SLV_DLY_JUMP_O	-	-	RESV	PHY_WDQLVL_PATT_1

Name	Bits	Default	Range	Description
PHY_WDQLVL_UPDT_WAIT_CNT_1	27:24	0x0	0x0-0xf	Number of cycles to wait after changing the DQ slave delay
PHY_WDQLVL_DQDM_SLV_DLY_JUMP_OFFSET_1	18:8	0x000	0x0-0x7ff	Defines the write/read burst length in bytes during the write data
PHY_WDQLVL_PATT_1	2:0	0x0	0x0-0x7	Defines the training patterns to be used during the write data leveling sequence for slice 1. Bit (0) corresponds to the LFSR data training pattern. Bit (1) corresponds to the CLK data training pattern. Bit (2) corresponds to user-defined

DENALI_PHY_154 (Address PHY_BASE_ADDR + 154)

31 -	- 24	23 17	16 16	15 12	11 8	7 4	3 0
OBSOLETE	-	RESV	SC_PHY_WDQLVL_CLR_P	RESV	PHY_WDQLVL_QTR_DLY_ST	RESV	PHY_WDQLVL_DQDM_OBS_

Name	Bits	Default	Range	Description
SC_PHY_WDQLVL_CLR_PREV_RESULTS_1	16	0x0	0x0-0x1	Clears the previous result value to allow a clean slate comparison for future write DQ leveling results for
PHY_WDQLVL_QTR_DLY_STEP_1	11:8	0x0	0x0-0xf	Defines the step granularity for the logic to use once an edge is found. When this occurs, the logic jumps back to the previous invalid value

PHY_WDQLVL_DQDM_OBS_SELECT_1	3:0	0x0	0x0-0xf	Select value to map an individual DQ data window leading/trailing edge to the leading/trailing edge

DENALI_PHY_155 (Address PHY_BASE_ADDR + 155)

31 - 16	15 - 9	8	7 - 0
OBSOLETE	RESV	PHY_WDQLVL_DATADM_MA	-

Name	Bits	Default	Range	Description
PHY_WDQLVL_DATADM_MASK_1	8:0	0x000	0x0-0x1ff	Per-bit mask for write data leveling for slice 1. Set to 1 to mask any bit

DENALI_PHY_156 (Address PHY_BASE_ADDR + 156)

31 - 0
PHY_USER_P -

Name	Bits	Default	Range	Description
PHY_USER_PATT0_1	31:0	0x00000000	0x0-0xffffffff	User-defined pattern to be used during write data leveling for slice 1. This register holds the bytes 3 to 0 written/read from device.

DENALI_PHY_157 (Address PHY_BASE_ADDR + 157)

31 - 0
PHY_USER_P -

Name	Bits	Default	Range	Description
PHY_USER_PATT1_1	31:0	0x00000000	0x0-0xffffffff	User-defined pattern to be used during write data leveling for slice 1. This register holds the bytes 7 to 4 written/read from device.

DENALI_PHY_158 (Address PHY_BASE_ADDR + 158)

31 - 0
PHY_USER_P -

Name	Bits	Default	Range	Description
PHY_USER_PATT2_1	31:0	0x00000000	0x0-0xffffffff	User-defined pattern to be used during write data leveling for slice 1. This register holds the bytes 11 to 8 written/read from device.

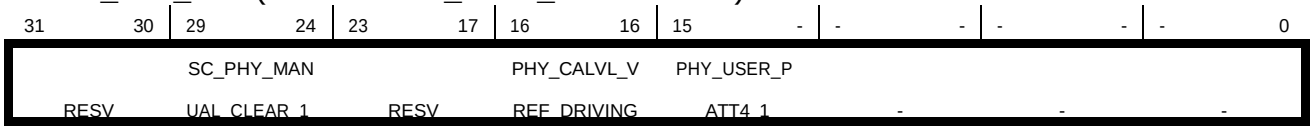
DENALI_PHY_159 (Address PHY_BASE_ADDR + 159)

31 - 0
PHY_USER_P -

Name	Bits	Default	Range	Description
PHY_USER_PATT3_1	31:0	0x00000000	0x0-0xffffffff	User-defined pattern to be used during write data leveling for slice 1. This register holds the bytes 15

				to 12 written/read from device.

DENALI_PHY_160 (Address PHY_BASE_ADDR + 160)

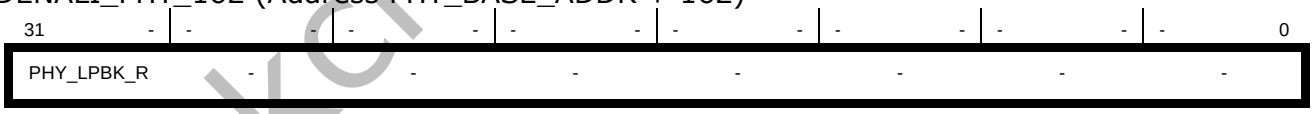


Name	Bits	Default	Range	Description
SC_PHY_MANUAL_CLEAR_1	29:24	0x00	0x0-0x3f	Manual reset/clear of internal logic for slice 1. Bit (0) initiates manual setup of the read DQS gate. Bit (1) is reset of read entry FIFO pointers. Bit (2) is reset of master delay min/ max lock values. Bit (3) is manual reset of master delay unlock
PHY_CALVL_VREF_DRIVING_SLICE_1	16	0x0	0x0-0x1	Indicates if slice 1 is used to drive the VREF value to the device
PHY_USER_PATT4_1	15:0	0x0000	0x0-0xffff	User-defined pattern to be used during write data leveling for slice 1. This register holds the DM bit for

DENALI_PHY_161 (Address PHY_BASE_ADDR + 161)

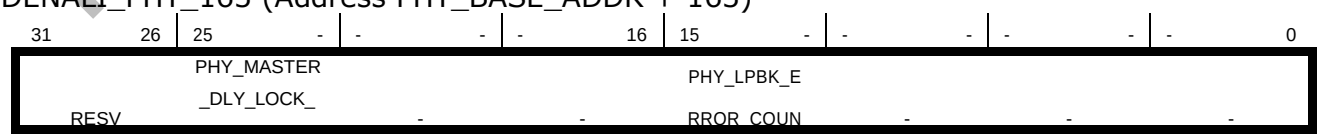
Name	Bits	Default	Range	Description
PHY_FIFO_PTR_OBS_1	7:0	0x00	0x0-0xff	Observation register for read entry FIFO pointers for slice 1. READ-

DENALI_PHY_162 (Address PHY_BASE_ADDR + 162)



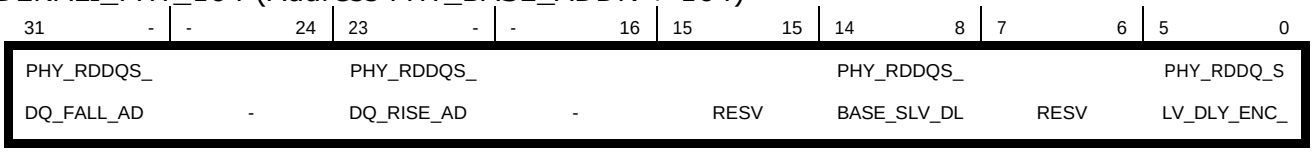
Name	Bits	Default	Range	Description
PHY_LPBK_RESULT_OBS_1	31:0	0x00000000	0x0-0xffffffff	Observation register containing loopback status/results for slice 1.

DENALI_PHY_163 (Address PHY_BASE_ADDR + 163)



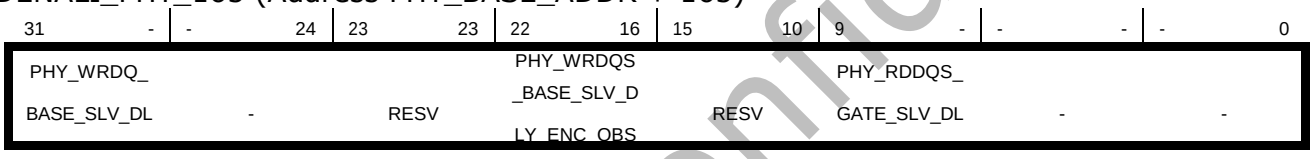
Name	Bits	Default	Range	Description
PHY_MASTER_DLY_LOCK_OBS_1	25:16	0x000	0x0-0x3ff	Observation register for master delay results for slice 1. READ-
PHY_LPBK_ERROR_COUNT_OBS_1	15:0	0x0000	0x0-0xffff	Observation register containing total number of loopback error data

DENALI_PHY_164 (Address PHY_BASE_ADDR + 164)



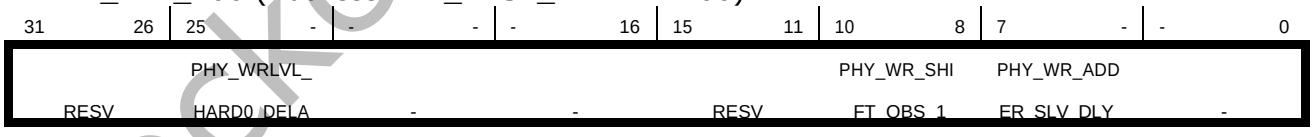
Name	Bits	Default	Range	Description
PHY_RDDQS_DQ_FALL_ADDER_SLV_DL	31:24	0x00	0x0-0xff	Observation register for read DQS DQ falling edge adder slave delay
PHY_RDDQS_DQ_RISE_ADDER_SLV_DL	23:16	0x00	0x0-0xff	Observation register for read DQS DQ rising edge adder slave delay
PHY_RDDQS_BASE_SLV_DLY_ENC_OBS_1	14:8	0x00	0x0-0x7f	Observation register for read DQS base slave delay encoded value for
PHY_RDDQ_SLV_DLY_ENC_OBS_1	5:0	0x00	0x0-0x3f	Observation register for read DQ slave delay encoded values for

DENALI_PHY_165 (Address PHY_BASE_ADDR + 165)



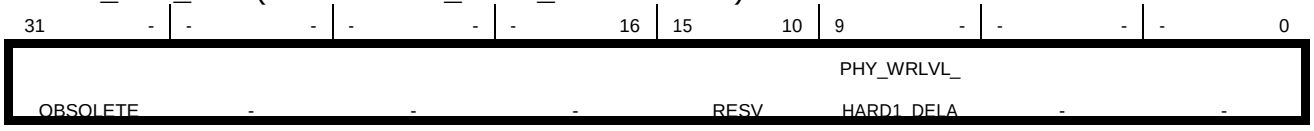
Name	Bits	Default	Range	Description
PHY_WRDQ_BASE_SLV_DLY_ENC_OBS_1	31:24	0x00	0x0-0xff	Observation register for write DQ base slave delay encoded value for
PHY_WRDQS_BASE_SLV_DLY_ENC_OBS_1	22:16	0x00	0x0-0x7f	Observation register for write DQS base slave delay encoded value for
PHY_RDDQS_GATE_SLV_DLY_ENC_OBS_1	9:0	0x000	0x0-0x3ff	Observation register for read DQS gate slave delay encoded value for

DENALI_PHY_166 (Address PHY_BASE_ADDR + 166)



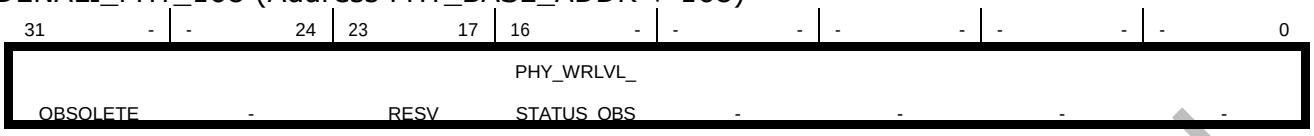
Name	Bits	Default	Range	Description
PHY_WRLVL_HARD0_DELAY_OBS_1	25:16	0x000	0x0-0x3ff	Observation register for write leveling last hard 0 DQS slave
PHY_WR_SHIFT_OBS_1	10:8	0x0	0x0-0x7	Observation register for automatic half cycle and cycle shift values for
PHY_WR_ADDER_SLV_DLY_ENC_OBS_1	7:0	0x00	0x0-0xff	Observation register for write adder slave delay encoded value for slice

DENALI_PHY_167 (Address PHY_BASE_ADDR + 167)



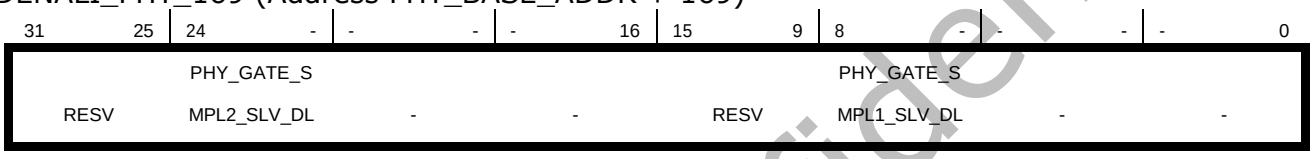
Name	Bits	Default	Range	Description
PHY_WRLVL_HARD1_DELAY_OBS_1	9:0	0x000	0x0-0x3ff	Observation register for write leveling first hard 1 DQS slave

DENALI_PHY_168 (Address PHY_BASE_ADDR + 168)



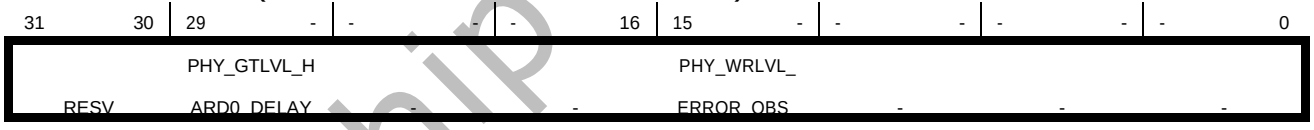
Name	Bits	Default	Range	Description
PHY_WRLVL_STATUS_OBS_1	16:0	0x00000	0x0-0x1ffff	Observation register for write leveling status for slice 1. READ-

DENALI_PHY_169 (Address PHY_BASE_ADDR + 169)



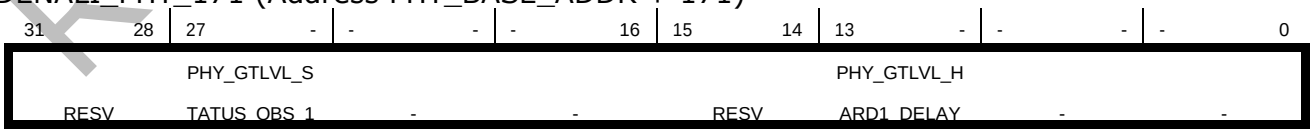
Name	Bits	Default	Range	Description
PHY_GATE_SMPL2_SLV_DLY_ENC_OBS_1	24:16	0x000	0x0-0x1ff	Observation register for gate sample1 slave delay encoded
PHY_GATE_SMPL1_SLV_DLY_ENC_OBS_1	8:0	0x000	0x0-0x1ff	Observation register for gate sample1 slave delay encoded

DENALI_PHY_170 (Address PHY_BASE_ADDR + 170)



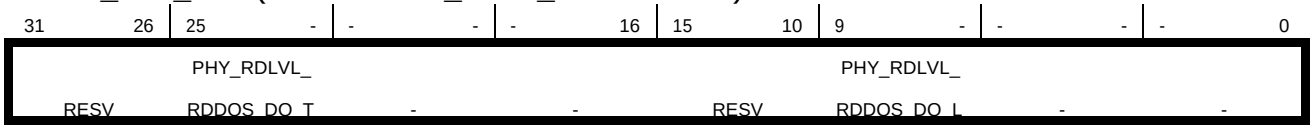
Name	Bits	Default	Range	Description
PHY_GTLVL_HARD0_DELAY_OBS_1	29:16	0x0000	0x0-0x3fff	Observation register for gate training first hard 0 DQS slave
PHY_WRLVL_ERROR_OBS_1	15:0	0x0000	0x0-0xffff	Observation register for write leveling error status for slice 1.

DENALI_PHY_171 (Address PHY_BASE_ADDR + 171)



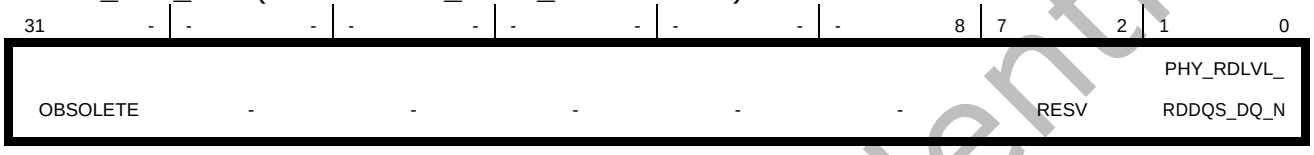
Name	Bits	Default	Range	Description
PHY_GTLVL_STATUS_OBS_1	27:16	0x000	0x0-0xfff	Observation register for gate training status for slice 1. READ-
PHY_GTLVL_HARD1_DELAY_OBS_1	13:0	0x0000	0x0-0x3fff	Observation register for gate training last hard 1 DQS slave

DENALI_PHY_172 (Address PHY_BASE_ADDR + 172)



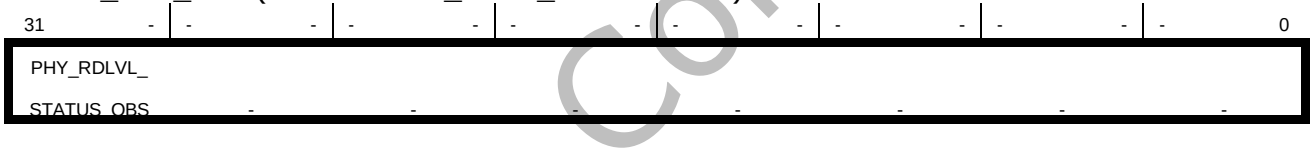
Name	Bits	Default	Range	Description
PHY_RDLVL_RDDQS_DQ_TE_DLY_OBS_	25:16	0x000	0x0-0x3ff	Observation register for read leveling data window trailing edge
PHY_RDLVL_RDDQS_DQ_LE_DLY_OBS_1	9:0	0x000	0x0-0x3ff	Observation register for read leveling data window leading edge

DENALI_PHY_173 (Address PHY_BASE_ADDR + 173)



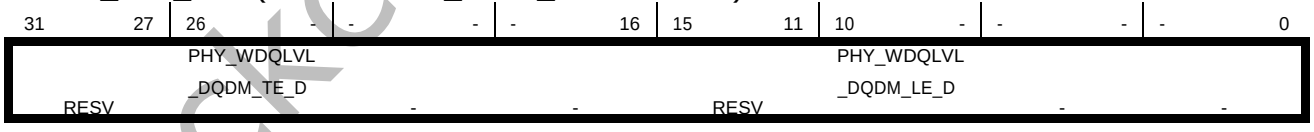
Name	Bits	Default	Range	Description
PHY_RDLVL_RDDQS_DQ_NUM_WINDOWS_OBS_1	1:0	0x0	0x0-0x3	Observation register for read leveling number of windows found

DENALI_PHY_174 (Address PHY_BASE_ADDR + 174)



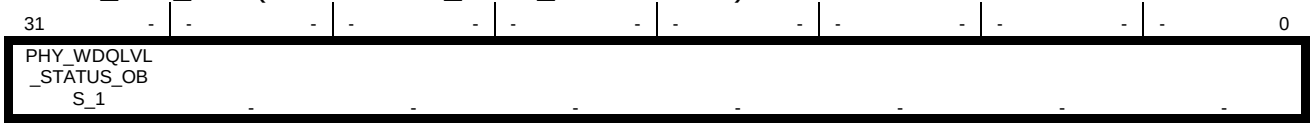
Name	Bits	Default	Range	Description
PHY_RDLVL_STATUS_OBS_1	31:0	0x00000000	0x0-0xffffffff	Observation register for read leveling status for slice 1. READ-

DENALI_PHY_175 (Address PHY_BASE_ADDR + 175)



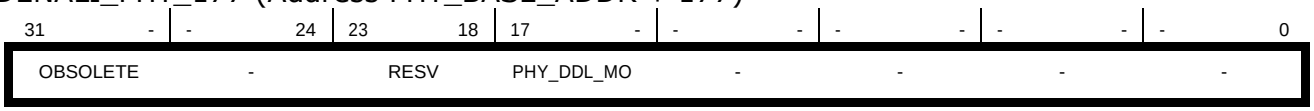
Name	Bits	Default	Range	Description
PHY_WDQLVL_DQDM_TE_DLY_OBS_1	26:16	0x000	0x0-0x7ff	Observation register for write data leveling data window trailing edge
PHY_WDQLVL_DQDM_LE_DLY_OBS_1	10:0	0x000	0x0-0x7ff	Observation register for write data leveling data window leading edge

DENALI_PHY_176 (Address PHY_BASE_ADDR + 176)



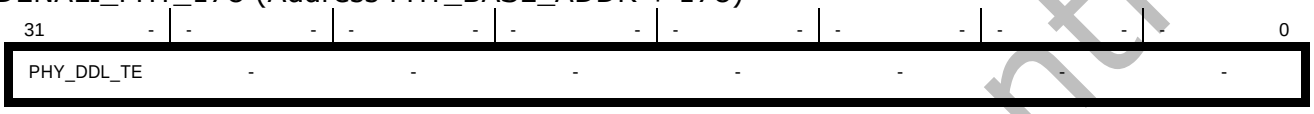
Name	Bits	Default	Range	Description
PHY_WDQLVL_STATUS_OBS_1	31:0	0x00000000	0x0-0xffffffff	Observation register for write data leveling status for slice 1. READ-

DENALI_PHY_177 (Address PHY_BASE_ADDR + 177)



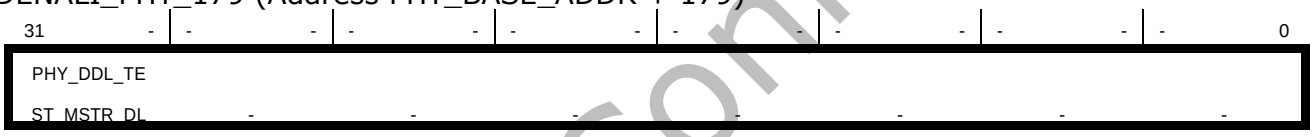
Name	Bits	Default	Range	Description
PHY_DDL_MODE_1	17:0	0x00000	0x0-0x3ffff	DDL mode for slice 1.

DENALI_PHY_178 (Address PHY_BASE_ADDR + 178)



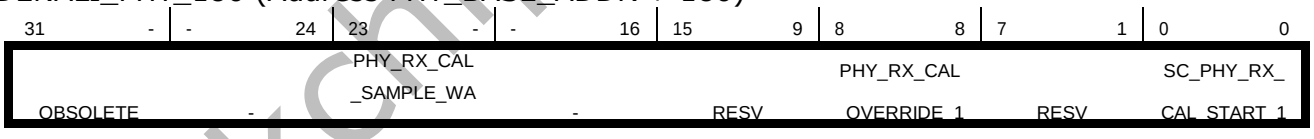
Name	Bits	Default	Range	Description
PHY_DDL_TEST_OBS_1	31:0	0x00000000	0x0-0xffffffff	DDL test observation for slice 1.

DENALI_PHY_179 (Address PHY_BASE_ADDR + 179)



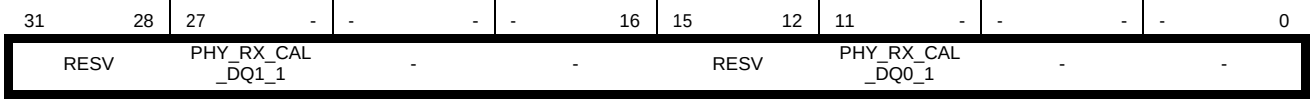
Name	Bits	Default	Range	Description
PHY_DDL_TEST_MSTR_DLY_OBS_1	31:0	0x000000	0x0-0xffffffff	DDL test observation delays for

DENALI_PHY_180 (Address PHY_BASE_ADDR + 180)



Name	Bits	Default	Range	Description
PHY_RX_CAL_SAMPLE_WAIT_1	23:16	0x00	0x0-0xff	RX Calibration state machine wait
PHY_RX_CAL_OVERRIDE_1	8	0x0	0x0-0x1	Manual setting of RX Calibration
SC_PHY_RX_CAL_START_1	0	0x0	0x0-0x1	Manual RX Calibration start for

DENALI_PHY_181 (Address PHY_BASE_ADDR + 181)



Name	Bits	Default	Range	Description

PHY_RX_CAL_DQ1_1	27:16	0x000	0x0-0xfff	RX Calibration codes for DQ1 for slice 1. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits
PHY_RX_CAL_DQ0_1	11:0	0x000	0x0-0xfff	RX Calibration codes for DQ0 for slice 1. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits

DENALI_PHY_182 (Address PHY_BASE_ADDR + 182)

31 28	27 - - - - 16	15 12	11 - - - - 0
RESV	PHY_RX_CAL_DQ3_1	RESV	PHY_RX_CAL_DQ2_1

Name	Bits	Default	Range	Description
PHY_RX_CAL_DQ3_1	27:16	0x000	0x0-0xfff	RX Calibration codes for DQ3 for slice 1. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits
PHY_RX_CAL_DQ2_1	11:0	0x000	0x0-0xfff	RX Calibration codes for DQ2 for slice 1. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits

DENALI_PHY_183 (Address PHY_BASE_ADDR + 183)

31 28	27 - - - - 16	15 12	11 - - - - 0
RESV	PHY_RX_CAL_DQ5_1	RESV	PHY_RX_CAL_DQ4_1

Name	Bits	Default	Range	Description
PHY_RX_CAL_DQ5_1	27:16	0x000	0x0-0xfff	RX Calibration codes for DQ5 for slice 1. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits
PHY_RX_CAL_DQ4_1	11:0	0x000	0x0-0xfff	RX Calibration codes for DQ4 for slice 1. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits

DENALI_PHY_184 (Address PHY_BASE_ADDR + 184)

31 28	27 - - - - 16	15 12	11 - - - - 0
RESV	PHY_RX_CAL_DQ7_1	RESV	PHY_RX_CAL_DQ6_1

Name	Bits	Default	Range	Description
PHY_RX_CAL_DQ7_1	27:16	0x000	0x0-0xfff	RX Calibration codes for DQ7 for slice 1. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits

PHY_RX_CAL_DQ6_1	11:0	0x000	0x0-0xfff	RX Calibration codes for DQ6 for slice 1. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits

DENALI_PHY_185 (Address PHY_BASE_ADDR + 185)

31 28	27 - - - - 16	15 12	11 - - - - 0
RESV	PHY_RX_CAL_DQS_1	RESV	PHY_RX_CAL_DM_1

Name	Bits	Default	Range	Description
PHY_RX_CAL_DQS_1	27:16	0x000	0x0-0xfff	RX Calibration codes for DQS for slice 1. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits
PHY_RX_CAL_DM_1	11:0	0x000	0x0-0xfff	RX Calibration codes for DM for slice 1. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits

DENALI_PHY_186 (Address PHY_BASE_ADDR + 186)

31 27	26 - - - - 16	15 12	11 - - - - 0
RESV	PHY_RX_CAL_OBS_1	RESV	PHY_RX_CAL_FDBK_1

Name	Bits	Default	Range	Description
PHY_RX_CAL_OBS_1	26:16	0x000	0x0-0x7ff	RX Calibration results for slice 1. Bits (7:0) contain calibration results from DQ0-7. Bit (8) contains calibration result from DM. Bit (9)
PHY_RX_CAL_FDBK_1	11:0	0x000	0x0-0xfff	RX Calibration codes for FDBK for slice 1. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits

DENALI_PHY_187 (Address PHY_BASE_ADDR + 187)

31 27	26 - - - - 16	15 11	10 - - - - 0
RESV	PHY_CLK_WR DQ1_SLAVE	RESV	PHY_CLK_WR DQ0_SLAVE

Name	Bits	Default	Range	Description
PHY_CLK_WRDQ1_SLAVE_DELAY_1	26:16	0x000	0x0-0x7ff	Write clock slave delay setting for
PHY_CLK_WRDQ0_SLAVE_DELAY_1	10:0	0x000	0x0-0x7ff	Write clock slave delay setting for

DENALI_PHY_188 (Address PHY_BASE_ADDR + 188)

31 27	26 - - - - 16	15 11	10 - - - - 0

	PHY_CLK_WR				PHY_CLK_WR		
RESV	DQ3_SLAVE	-	-	RESV	DQ2_SLAVE	-	-

Name	Bits	Default	Range	Description
PHY_CLK_WRDQ3_SLAVE_DELAY_1	26:16	0x000	0x0-0x7ff	Write clock slave delay setting for
PHY_CLK_WRDQ2_SLAVE_DELAY_1	10:0	0x000	0x0-0x7ff	Write clock slave delay setting for

DENALI_PHY_189 (Address PHY_BASE_ADDR + 189)

31	27	26	-	-	-	-	16	15	11	10	-	-	-	-	0
		PHY_CLK_WR								PHY_CLK_WR					
RESV		DQ5_SLAVE	-	-	-	-		RESV		DQ4_SLAVE	-	-	-	-	

Name	Bits	Default	Range	Description
PHY_CLK_WRDQ5_SLAVE_DELAY_1	26:16	0x000	0x0-0x7ff	Write clock slave delay setting for
PHY_CLK_WRDQ4_SLAVE_DELAY_1	10:0	0x000	0x0-0x7ff	Write clock slave delay setting for

DENALI_PHY_190 (Address PHY_BASE_ADDR + 190)

31	27	26	-	-	-	-	16	15	11	10	-	-	-	-	0
		PHY_CLK_WR								PHY_CLK_WR					
RESV		DQ7_SLAVE	-	-	-	-		RESV		DQ6_SLAVE	-	-	-	-	

Name	Bits	Default	Range	Description
PHY_CLK_WRDQ7_SLAVE_DELAY_1	26:16	0x000	0x0-0x7ff	Write clock slave delay setting for
PHY_CLK_WRDQ6_SLAVE_DELAY_1	10:0	0x000	0x0-0x7ff	Write clock slave delay setting for

DENALI_PHY_191 (Address PHY_BASE_ADDR + 191)

31	26	25	-	-	-	-	16	15	11	10	-	-	-	-	0
		PHY_CLK_WR								PHY_CLK_WR					
RESV		DQS_SLAVE	-	-	-	-		RESV		DM_SLAVE_D	-	-	-	-	

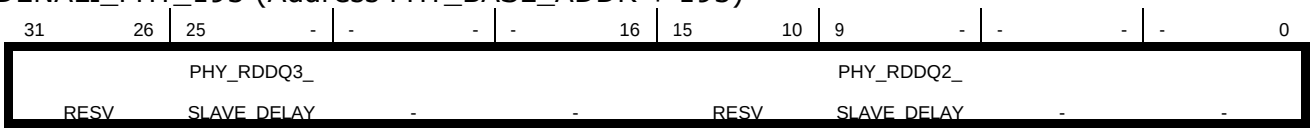
Name	Bits	Default	Range	Description
PHY_CLK_WRDQS_SLAVE_DELAY_1	25:16	0x000	0x0-0x3ff	Write clock slave delay setting for
PHY_CLK_WRDM_SLAVE_DELAY_1	10:0	0x000	0x0-0x7ff	Write clock slave delay setting for

DENALI_PHY_192 (Address PHY_BASE_ADDR + 192)

31	26	25	-	-	-	-	16	15	10	9	-	-	-	-	0
		PHY_RDDQ1_								PHY_RDDQ0_					
RESV		SLAVE_DELAY	-	-	-	-		RESV		SLAVE_DELAY	-	-	-	-	

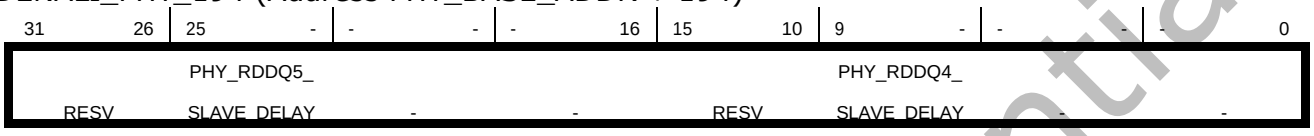
Name	Bits	Default	Range	Description
PHY_RDDQ1_SLAVE_DELAY_1	25:16	0x000	0x0-0x3ff	Read DQ1 slave delay setting for
PHY_RDDQ0_SLAVE_DELAY_1	9:0	0x000	0x0-0x3ff	Read DQ0 slave delay setting for

DENALI_PHY_193 (Address PHY_BASE_ADDR + 193)



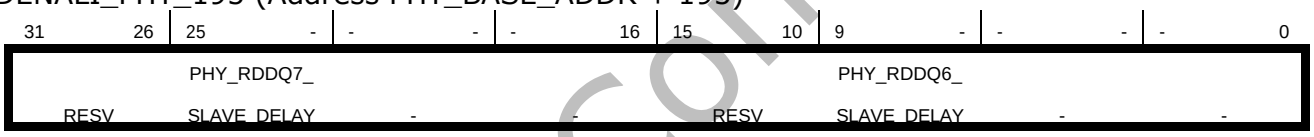
Name	Bits	Default	Range	Description
PHY_RDDQ3_SLAVE_DELAY_1	25:16	0x000	0x0-0x3ff	Read DQ3 slave delay setting for
PHY_RDDQ2_SLAVE_DELAY_1	9:0	0x000	0x0-0x3ff	Read DQ2 slave delay setting for

DENALI_PHY_194 (Address PHY_BASE_ADDR + 194)



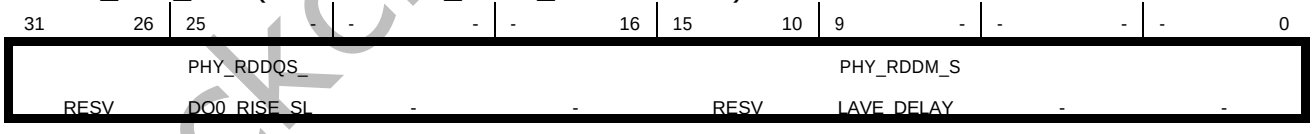
Name	Bits	Default	Range	Description
PHY_RDDQ5_SLAVE_DELAY_1	25:16	0x000	0x0-0x3ff	Read DQ5 slave delay setting for
PHY_RDDQ4_SLAVE_DELAY_1	9:0	0x000	0x0-0x3ff	Read DQ4 slave delay setting for

DENALI_PHY_195 (Address PHY_BASE_ADDR + 195)



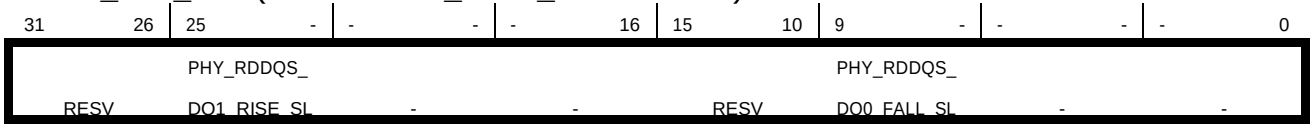
Name	Bits	Default	Range	Description
PHY_RDDQ7_SLAVE_DELAY_1	25:16	0x000	0x0-0x3ff	Read DQ7 slave delay setting for
PHY_RDDQ6_SLAVE_DELAY_1	9:0	0x000	0x0-0x3ff	Read DQ6 slave delay setting for

DENALI_PHY_196 (Address PHY_BASE_ADDR + 196)



Name	Bits	Default	Range	Description
PHY_RDDQS_DQ0_RISE_SLAVE_DELAY_	25:16	0x000	0x0-0x3ff	Rising edge read DQS slave delay
PHY_RDDM_SLAVE_DELAY_1	9:0	0x000	0x0-0x3ff	Read DM/DBI slave delay setting for slice 1. May be used for data

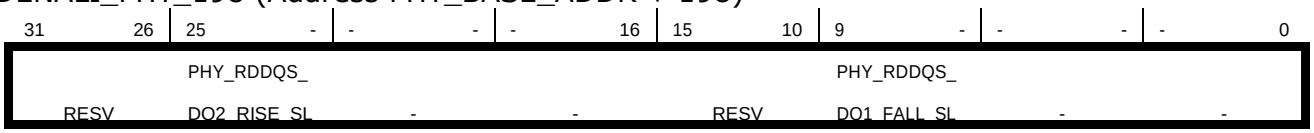
DENALI_PHY_197 (Address PHY_BASE_ADDR + 197)



Name	Bits	Default	Range	Description

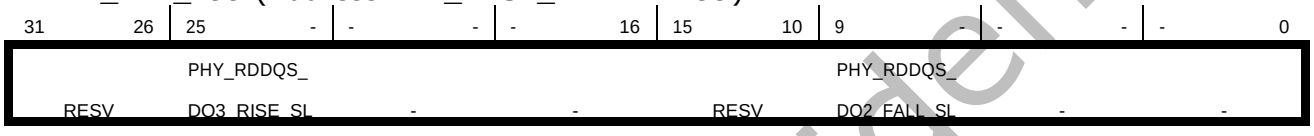
PHY_RDDQS_DQ1_RISE_SLAVE_DELAY_	25:16	0x000	0x0-0x3ff	Rising edge read DQS slave delay
PHY_RDDQS_DQ0_FALL_SLAVE_DELAY_	9:0	0x000	0x0-0x3ff	Falling edge read DQS slave delay

DENALI_PHY_198 (Address PHY_BASE_ADDR + 198)



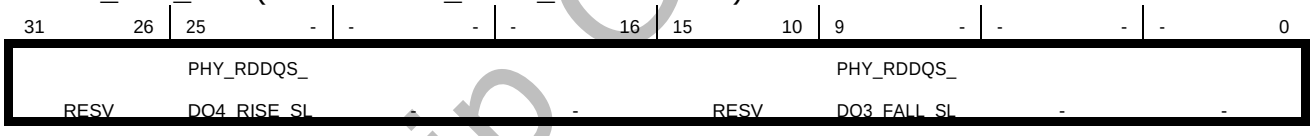
Name	Bits	Default	Range	Description
PHY_RDDQS_DQ2_RISE_SLAVE_DELAY_	25:16	0x000	0x0-0x3ff	Rising edge read DQS slave delay
PHY_RDDQS_DQ1_FALL_SLAVE_DELAY_	9:0	0x000	0x0-0x3ff	Falling edge read DQS slave delay

DENALI_PHY_199 (Address PHY_BASE_ADDR + 199)



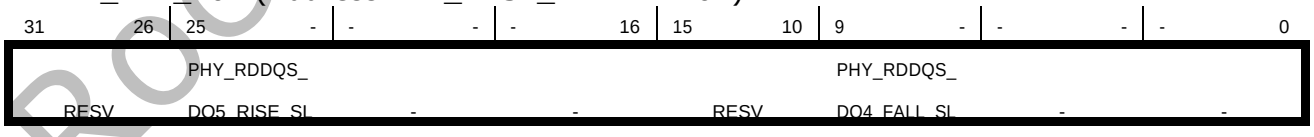
Name	Bits	Default	Range	Description
PHY_RDDQS_DQ3_RISE_SLAVE_DELAY_	25:16	0x000	0x0-0x3ff	Rising edge read DQS slave delay
PHY_RDDQS_DQ2_FALL_SLAVE_DELAY_	9:0	0x000	0x0-0x3ff	Falling edge read DQS slave delay

DENALI_PHY_200 (Address PHY_BASE_ADDR + 200)



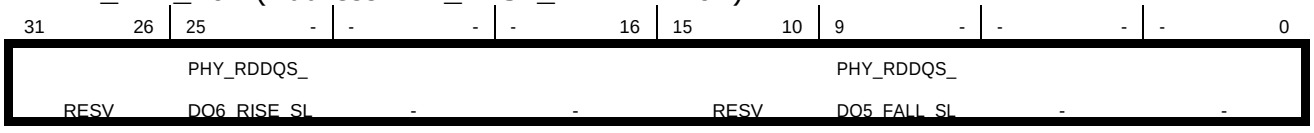
Name	Bits	Default	Range	Description
PHY_RDDQS_DQ4_RISE_SLAVE_DELAY_	25:16	0x000	0x0-0x3ff	Rising edge read DQS slave delay
PHY_RDDQS_DQ3_FALL_SLAVE_DELAY_	9:0	0x000	0x0-0x3ff	Falling edge read DQS slave delay

DENALI_PHY_201 (Address PHY_BASE_ADDR + 201)



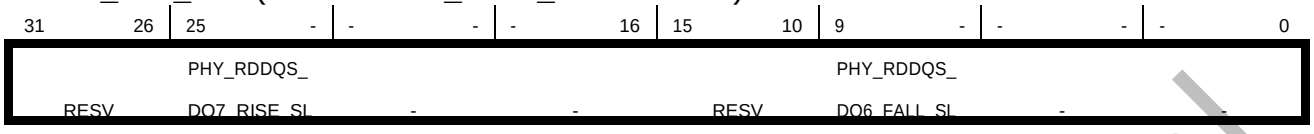
Name	Bits	Default	Range	Description
PHY_RDDQS_DQ5_RISE_SLAVE_DELAY_	25:16	0x000	0x0-0x3ff	Rising edge read DQS slave delay
PHY_RDDQS_DQ4_FALL_SLAVE_DELAY_	9:0	0x000	0x0-0x3ff	Falling edge read DQS slave delay

DENALI_PHY_202 (Address PHY_BASE_ADDR + 202)



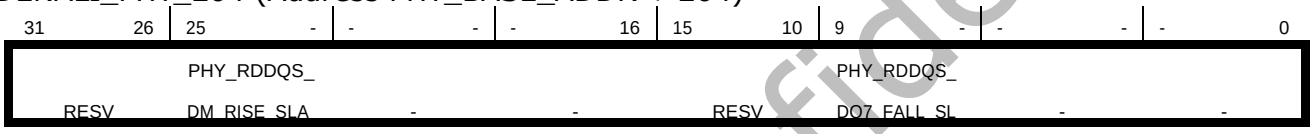
Name	Bits	Default	Range	Description
PHY_RDDQS_DQ6_RISE_SLAVE_DELAY_	25:16	0x000	0x0-0x3ff	Rising edge read DQS slave delay
PHY_RDDQS_DQ5_FALL_SLAVE_DELAY_	9:0	0x000	0x0-0x3ff	Falling edge read DQS slave delay

DENALI_PHY_203 (Address PHY_BASE_ADDR + 203)



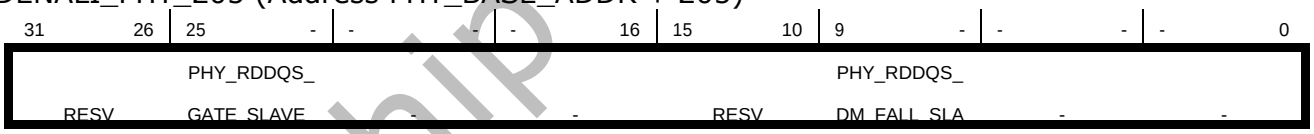
Name	Bits	Default	Range	Description
PHY_RDDQS_DQ7_RISE_SLAVE_DELAY_	25:16	0x000	0x0-0x3ff	Rising edge read DQS slave delay
PHY_RDDQS_DQ6_FALL_SLAVE_DELAY_	9:0	0x000	0x0-0x3ff	Falling edge read DQS slave delay

DENALI_PHY_204 (Address PHY_BASE_ADDR + 204)



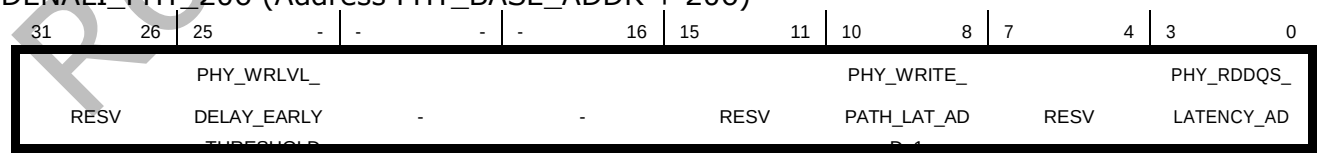
Name	Bits	Default	Range	Description
PHY_RDDQS_DM_RISE_SLAVE_DELAY_1	25:16	0x000	0x0-0x3ff	Rising edge read DQS slave delay
PHY_RDDQS_DQ7_FALL_SLAVE_DELAY_	9:0	0x000	0x0-0x3ff	Falling edge read DQS slave delay

DENALI_PHY_205 (Address PHY_BASE_ADDR + 205)



Name	Bits	Default	Range	Description
PHY_RDDQS_GATE_SLAVE_DELAY_1	25:16	0x000	0x0-0x3ff	Read DQS slave delay setting for
PHY_RDDQS_DM_FALL_SLAVE_DELAY_1	9:0	0x000	0x0-0x3ff	Falling edge read DQS slave delay

DENALI_PHY_206 (Address PHY_BASE_ADDR + 206)



Name	Bits	Default	Range	Description
PHY_WRLVL_DELAY_EARLY_THRESHOLD_1	25:16	0x000	0x0-0x3ff	Write level delay threshold above which will be considered in
PHY_WRITE_PATH_LAT_ADD_1	10:8	0x0	0x0-0x7	Number of cycles to delay the incoming dfi_wrdata_en/dfi_wrdata
PHY_RDDQS_LATENCY_ADJUST_1	3:0	0x0	0x0-0xf	Number of cycles to delay the incoming dfi_rddata_en for read

DENALI_PHY_207 (Address PHY_BASE_ADDR + 207)

31 - 24	23 - 17	16 - 16	15 - 10	9 - 0
OBSOLETE	RESV	PHY_WRLVL_EARLY_FORC	RESV	PHY_WRLVL_DELAY_PERIO

Name	Bits	Default	Range	Description
PHY_WRLVL_EARLY_FORCE_ZERO_1	16	0x0	0x0-0x1	Force the final write level delay value (that meets the early
PHY_WRLVL_DELAY_PERIOD_THRESHOLD_1	9:0	0x000	0x0-0x3ff	Write level delay threshold below which will add a cycle of write path

DENALI_PHY_208 (Address PHY_BASE_ADDR + 208)

31 - 24	23 - 20	19 - 16	15 - 10	9 - 0
OBSOLETE	RESV	PHY_GTLVL_LAT_ADJ_STAR	RESV	PHY_GTLVL_RDDQS_SLV_D

Name	Bits	Default	Range	Description
PHY_GTLVL_LAT_ADJ_START_1	19:16	0x0	0x0-0xf	Initial read DQS gate cycle delay from dfi_rddata_en during gate
PHY_GTLVL_RDDQS_SLV_DLY_START_1	9:0	0x000	0x0-0x3ff	Initial read DQS gate slave delay setting during gate training for slice

DENALI_PHY_209 (Address PHY_BASE_ADDR + 209)

31 26	25 - 16	15 11	10 - 0
RESV	PHY_RDLVL_RDDQS_DQ_S	RESV	PHY_WDQLVL_DQDM_SLV_

Name	Bits	Default	Range	Description
PHY_RDLVL_RDDQS_DQ_SLV_DLY_START_1	25:16	0x000	0x0-0x3ff	Read leveling starting value for the DQS/DQ slave delay settings for
PHY_WDQLVL_DQDM_SLV_DLY_START_1	10:0	0x000	0x0-0x7ff	Initial DQ/DM slave delay setting during write data leveling for slice

DENALI_PHY_210 (Address PHY_BASE_ADDR + 210)

31 - 8	7 2	1 0
OBSOLETE	RESV	RESERVED

Name	Bits	Default	Range	Description
RESERVED	1:0	0x0	0x0-0x3	Reserved for future use. Refer to the regconfig files for the default

DENALI_PHY_211 (Address PHY_BASE_ADDR + 211)

31 - 24	23 - 16	15 - 8	7 - 0
PHY_DQS_OE_TIMING_1	PHY_DQ_TSEL_WR_TIMING	PHY_DQ_TSEL_RD_TIMING	PHY_DQ_OE_TIMING_1

Name	Bits	Default	Range	Description
PHY_DQS_OE_TIMING_1	31:24	0x00	0x0-0xff	Start/end timing values for DQS
PHY_DQ_TSEL_WR_TIMING_1	23:16	0x00	0x0-0xff	Start/end timing values for DQ/DM write based termination enable and
PHY_DQ_TSEL_RD_TIMING_1	15:8	0x00	0x0-0xff	Start/end timing values for DQ/DM read based termination enable and
PHY_DQ_OE_TIMING_1	7:0	0x00	0x0-0xff	Start/end timing values for DQ/DM

DENALI_PHY_212 (Address PHY_BASE_ADDR + 212)

31 - 24	23 - 17	16 - 16	15 - 8	7 - 0
PHY_DQ_IE_TIMING_1	RESV	PHY_PER_CS_TRAINING_EN_1	PHY_DQS_TSEL_WR_TIMING_1	PHY_DQS_TSEL_RD_TIMING_1

Name	Bits	Default	Range	Description
PHY_DQ_IE_TIMING_1	31:24	0x00	0x0-0xff	Start/end timing values for DQ/DM
PHY_PER_CS_TRAINING_EN_1	16	0x0	0x0-0x1	Enables the per-rank training and read/write timing capabilities. Must
PHY_DQS_TSEL_WR_TIMING_1	15:8	0x00	0x0-0xff	Start/end timing values for DQS write based termination enable and
PHY_DQS_TSEL_RD_TIMING_1	7:0	0x00	0x0-0xff	Start/end timing values for DQS read based termination enable and

DENALI_PHY_213 (Address PHY_BASE_ADDR + 213)

31 28	27 24	23 18	17 16	15 10	9 8	7 -	- 0
RESV	PHY_RDDATA_EN_DLY_1	RESV	PHY_IE_MODE_1	RESV	PHY_RDDATA_EN_IE_DLY_1	PHY_DQS_IE_TIMING_1	-

Name	Bits	Default	Range	Description
PHY_RDDATA_EN_DLY_1	27:24	0x0	0x0-0xf	Number of cycles that the dfi_rddata_en signal is early for
PHY_IE_MODE_1	17:16	0x0	0x0-0x3	Input enable mode bits for slice 1. Bit (0) enables the mode where the input enables are always on; set to
PHY_RDDATA_EN_IE_DLY_1	9:8	0x0	0x0-0x3	Number of cycles that the dfi_rddata_en signal is earlier than
PHY_DQS_IE_TIMING_1	7:0	0x00	0x0-0xff	Start/end timing values for DQS

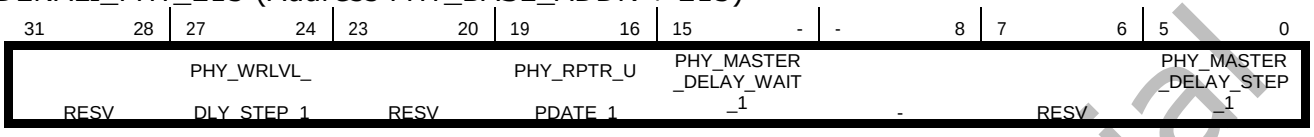
DENALI_PHY_214 (Address PHY_BASE_ADDR + 214)

31 26	25 - 16	15 12	11 8	7 4	3 0
RESV	PHY_MASTER_DELAY_START_1	RESV	PHY_SW_MASTER_MODE_1	RESV	PHY_RDDATA_EN_TSEL_DLY_1

Name	Bits	Default	Range	Description
PHY_MASTER_DELAY_START_1	25:16	0x000	0x0-0x3ff	Start value for master delay line

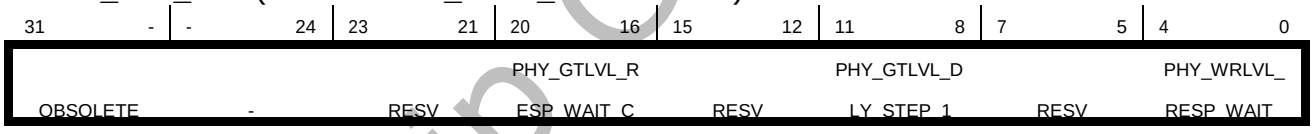
PHY_SW_MASTER_MODE_1	11:8	0x0	0x0-0xf	Master delay line override settings for slice 1. Bit (0) enables software half clock mode. Bit (1) is the software half clock mode value. Bit
PHY_RDDATA_EN_TSEL_DLY_1	3:0	0x0	0x0-0xf	Number of cycles that the dfi_rddata_en signal is earlier than

DENALI_PHY_215 (Address PHY_BASE_ADDR + 215)



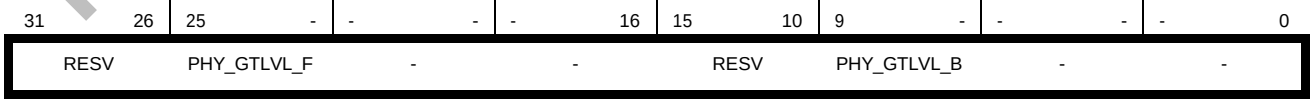
Name	Bits	Default	Range	Description
PHY_WRLVL_DLY_STEP_1	27:24	0x0	0x0-0xf	DQS slave delay step size during
PHY_RPTR_UPDATE_1	19:16	0x0	0x0-0xf	Offset in cycles from the dfi_rddata_en signal to release
PHY_MASTER_DELAY_WAIT_1	15:8	0x00	0x0-0xff	Wait cycles for master delay line locking algorithm for slice 1. Bits (3:0) are the cycle wait count after a calibration clock setting change.
PHY_MASTER_DELAY_STEP_1	5:0	0x00	0x0-0x3f	Incremental step size for master delay line locking algorithm for slice

DENALI_PHY_216 (Address PHY_BASE_ADDR + 216)



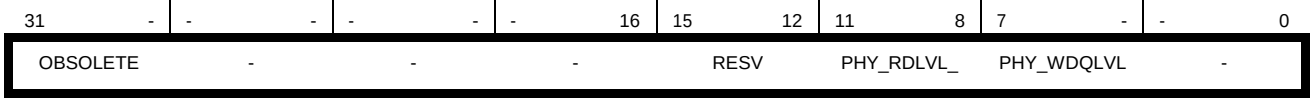
Name	Bits	Default	Range	Description
PHY_GTLVL_RESP_WAIT_CNT_1	20:16	0x00	0x0-0x1f	Number of cycles + 4 to wait between dfi_rddata_en and the sampling of the DQS during gate
PHY_GTLVL_DLY_STEP_1	11:8	0x0	0x0-0xf	DQS slave delay step size during
PHY_WRLVL_RESP_WAIT_CNT_1	4:0	0x00	0x0-0x1f	Number of cycles to wait between dfi_wrlvl_strobe and the sampling

DENALI_PHY_217 (Address PHY_BASE_ADDR + 217)



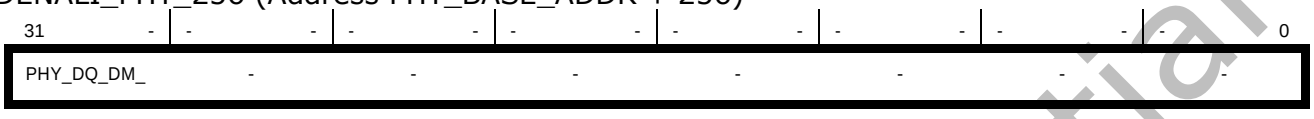
Name	Bits	Default	Range	Description
PHY_GTLVL_FINAL_STEP_1	25:16	0x000	0x0-0x3ff	Final backup step delay used in
PHY_GTLVL_BACK_STEP_1	9:0	0x000	0x0-0x3ff	Interim backup step delay used in

DENALI_PHY_218 (Address PHY_BASE_ADDR + 218)



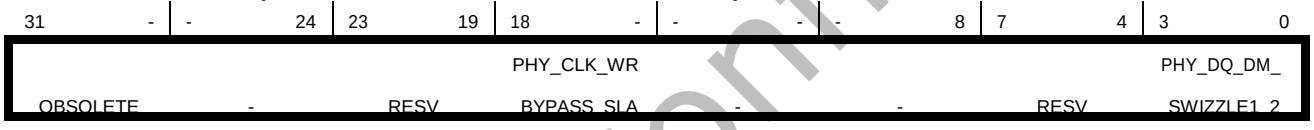
Name	Bits	Default	Range	Description
PHY_RDLVL_DLY_STEP_1	11:8	0x0	0x0-0xf	DQS slave delay step size during
PHY_WDQLVL_DLY_STEP_1	7:0	0x00	0x0-0xff	DQ slave delay step size during

DENALI_PHY_256 (Address PHY_BASE_ADDR + 256)



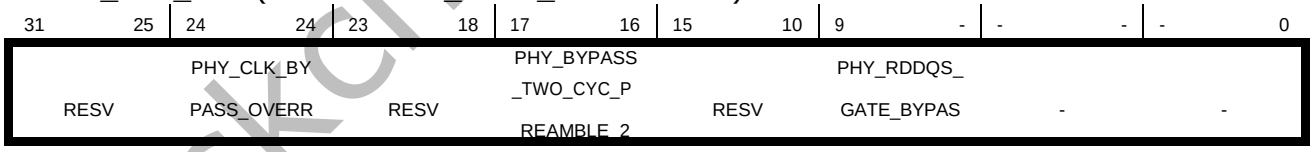
Name	Bits	Default	Range	Description
PHY_DQ_DM_SWIZZLE0_2	31:0	0x00000000	0x0-0xffffffff	DO/DM bit swizzling 0 for slice 2. Bits (3:0) inform the PHY which bit in {DM,DQ} map to DQ0. Bits (7:4) {DM,DQ} map to DQ1, etc.

DENALI_PHY_257 (Address PHY_BASE_ADDR + 257)



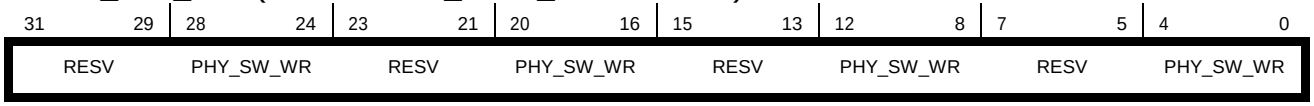
Name	Bits	Default	Range	Description
PHY_CLK_WR_BYPASS_SLAVE_DELAY_2	18:8	0x000	0x0-0x7ff	Write data clock bypass mode
PHY_DQ_DM_SWIZZLE1_2	3:0	0x0	0x0-0xf	DQ/DM bit swizzling 1 for slice 2. Bits (3:0) inform the PHY which bit

DENALI_PHY_258 (Address PHY_BASE_ADDR + 258)



Name	Bits	Default	Range	Description
PHY_CLK_BYPASS_OVERRIDE_2	24	0x0	0x0-0x1	Bypass mode override setting for
PHY_BYPASS_TWO_CYC_PREAMBLE_2	17:16	0x0	0x0-0x3	PHY two_cycle_preamble for
PHY_RDDQS_GATE_BYPASS_SLAVE_DE	9:0	0x000	0x0-0x3ff	Read DQS bypass mode slave

DENALI_PHY_259 (Address PHY_BASE_ADDR + 259)



Name	Bits	Default	Range	Description

PHY_SW_WRDQ3_SHIFT_2	28:24	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for write DQ3 for slice 2. Bit (0) enables override of half_cycle_shift. Bit (1)
PHY_SW_WRDQ2_SHIFT_2	20:16	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for write DQ2 for slice 2. Bit (0) enables override of half_cycle_shift. Bit (1)
PHY_SW_WRDQ1_SHIFT_2	12:8	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for write DQ1 for slice 2. Bit (0) enables override of half_cycle_shift. Bit (1)
PHY_SW_WRDQ0_SHIFT_2	4:0	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for write DQ0 for slice 2. Bit (0) enables override of half_cycle_shift. Bit (1)

DENALI_PHY_260 (Address PHY_BASE_ADDR + 260)

31 29	28 24	23 21	20 16	15 13	12 8	7 5	4 0
RESV	PHY_SW_WR	RESV	PHY_SW_WR	RESV	PHY_SW_WR	RESV	PHY_SW_WR

Name	Bits	Default	Range	Description
PHY_SW_WRDQ7_SHIFT_2	28:24	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for write DQ7 for slice 2. Bit (0) enables override of half_cycle_shift. Bit (1)
PHY_SW_WRDQ6_SHIFT_2	20:16	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for write DQ6 for slice 2. Bit (0) enables override of half_cycle_shift. Bit (1)
PHY_SW_WRDQ5_SHIFT_2	12:8	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for write DQ5 for slice 2. Bit (0) enables override of half_cycle_shift. Bit (1)
PHY_SW_WRDQ4_SHIFT_2	4:0	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for write DQ4 for slice 2. Bit (0) enables override of half_cycle_shift. Bit (1)

DENALI_PHY_261 (Address PHY_BASE_ADDR + 261)

31 -	- 24	23 19	18 16	15 12	11 8	7 5	4 0
OBSOLETE	-	RESV	PHY_DQ_TSE	RESV	PHY_SW_WR	RESV	PHY_SW_WR

Name	Bits	Default	Range	Description

PHY_DQ_TSEL_ENABLE_2	18:16	0x0	0x0-0x7	Operation type tsel enables for DQ/DM signals for slice 2. Bit (0) enables tsel_en during read cycles. Bit (1) enables tsel_en during write
PHY_SW_WRDQS_SHIFT_2	11:8	0x0	0x0-0xf	Manual override of automatic half_cycle_shift/cycle_shift for write DQS for slice 2. Bit (0) enables override of half_cycle_shift. Bit (1)
PHY_SW_WRDM_SHIFT_2	4:0	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for write DM for slice 2. Bit (0) enables override of half_cycle_shift. Bit (1)

DENALI_PHY_262 (Address PHY_BASE_ADDR + 262)

31 27	26 24	23 -	- -	- -	- -	- -	- 0
RESV	PHY_DQS_TS EL_ENABLE_2	PHY_DQ_TSE L_SELECT_2	-	-	-	-	-

Name	Bits	Default	Range	Description
PHY_DQS_TSEL_ENABLE_2	26:24	0x0	0x0-0x7	Operation type tsel enables for DQS signals for slice 2. Bit (0) enables tsel_en during read cycles. Bit (1) enables tsel_en during write
PHY_DQ_TSEL_SELECT_2	23:0	0x000000	0x0-0xffffff	Operation type tsel select values for DQ/DM signals for slice 2. Bits (3:0) are tsel_sel values during read cycles. Bits (7:4) are tsel_sel

DENALI_PHY_263 (Address PHY_BASE_ADDR + 263)

31 26	25 24	23 -	- -	- -	- -	- -	- 0
RESV	PHY_TWO_CY C_PREAMBLE	PHY_DQS_TS EL_SELECT_2	-	-	-	-	-

Name	Bits	Default	Range	Description
PHY_TWO_CYC_PREAMBLE_2	25:24	0x0	0x0-0x3	2 cycle preamble support for slice 2. Bit (0) controls the 2 cycle read preamble. Bit (1) controls the 2
PHY_DQS_TSEL_SELECT_2	23:0	0x000000	0x0-0xffffff	Operation type tsel select values for DQS signals for slice 2. Bits (3:0) are tsel_sel values during read cycles. Bits (7:4) are tsel_sel

DENALI_PHY_264 (Address PHY_BASE_ADDR + 264)

31 25	24 24	23 17	16 16	15 10	9 8	7 1	0 0
RESV	PHY_PER_CS _TRAINING_IN DEX_2	RESV	PHY_PER_CS _TRAINING_M	RESV	PHY_PER_RA NK_CS_MAP_	RESV	PHY_DBI_MO

Name	Bits	Default	Range	Description

PHY_PER_CS_TRAINING_INDEX_2	24	0x0	0x0-0x1	For per-rank training, indicates which ranksparamtersareread/
PHY_PER_CS_TRAINING_MULTICAST_EN_2	16	0x1	0x0-0x1	When set, a register write will update parameters for all ranks at
PHY_PER_RANK_CS_MAP_2	9:8	0x0	0x0-0x3	Per-rank CS map for slice 2.
PHY_DBI_MODE_2	0	0x0	0x0-0x1	DBI mode for slice 2. Bit (0) enables return of DBI read data. Bit

DENALI_PHY_265 (Address PHY_BASE_ADDR + 265)

31 28	27 24	23 20	19 16	15 12	11 8	7 2	1 0
RESV	PHY_LP4_BOOT_RPTR_UP	RESV	PHY_LP4_BOOT_RDDATA_	RESV	PHY_LP4_BOOT_RDDATA_	RESV	PHY_LP4_BOOT_RDDATA_

Name	Bits	Default	Range	Description
PHY_LP4_BOOT_RPTR_UPDATE_2	27:24	0x0	0x0-0xf	For LPDDR4 boot frequency, the offset in cycles from the
PHY_LP4_BOOT_RDDATA_EN_TSEL_DLY_2	19:16	0x0	0x0-0xf	For LPDDR4 boot frequency, the number of cycles that the dfi_rddata_en signal is earlier than
PHY_LP4_BOOT_RDDATA_EN_DLY_2	11:8	0x0	0x0-0xf	For LPDDR4 boot frequency, the number of cycles that the
PHY_LP4_BOOT_RDDATA_EN_IE_DLY_2	1:0	0x0	0x0-0x3	For LPDDR4 boot frequency, the number of cycles that the dfi_rddata_en signal is earlier than

DENALI_PHY_266 (Address PHY_BASE_ADDR + 266)

31 -	- 24	23 17	16 16	15 15	14 8	7 4	3 0
OBSOLETE	-	RESV	PHY_SLICE_PWR_RDC_DIS	RESV	PHY_LPBK_CONTROL_2	RESV	PHY_LP4_BOOT_RDDQS_L

Name	Bits	Default	Range	Description
PHY_SLICE_PWR_RDC_DISABLE_2	16	0x0	0x0-0x1	data slice power reduction disable
PHY_LPBK_CONTROL_2	14:8	0x00	0x0-0x7f	Loopback control bits for slice 2.
PHY_LP4_BOOT_RDDQS_LATENCY_ADJ	3:0	0x0	0x0-0xf	For LPDDR4 boot frequency, the number of cycles to delay the

DENALI_PHY_267 (Address PHY_BASE_ADDR + 267)

31 25	24 24	23 21	20 16	15 10	9 -	- -	- 0
RESV	PHY_SNAP_OBS_REGS_2	RESV	PHY_GATE_ERROR_DELAY_SELECT_2	RESV	PHY_RDDQS_DQ_BYPASS_	-	-

Name	Bits	Default	Range	Description

SC_PHY_SNAP_OBS_REGS_2	24	0x0	0x0-0x1	Initiates a snapshot of the internal observation registers for slice 2.
PHY_GATE_ERROR_DELAY_SELECT_2	20:16	0x00	0x0-0x1f	Number of cycles to wait for the DQS gate to close before flagging
PHY_RDDQS_DQ_BYPASS_SLAVE_DELAY_2	9:0	0x000	0x0-0x3ff	Read DQS data clock bypass mode

DENALI_PHY_268 (Address PHY_BASE_ADDR + 268)

31 25	24 -	- -	- 16	15 10	9 8	7 1	0 0
RESV	PHY_GATE_SMPL1_SLAVE	-	-	RESV	PHY_LPDDR_TYPE_2	RESV	PHY_LPDDR_2

Name	Bits	Default	Range	Description
PHY_GATE_SMPL1_SLAVE_DELAY_2	24:16	0x000	0x0-0x1ff	Number of cycles to delay the read DQS gate signal to generate gate1
PHY_LPDDR_TYPE_2	9:8	0x0	0x0-0x3	Indicates the type of DRAM for slice 2. Clear to 0 for DDR3 or
PHY_LPDDR_2	0	0x0	0x0-0x1	Indicates a cycle of delay for the

DENALI_PHY_269 (Address PHY_BASE_ADDR + 269)

31 -	- 24	23 18	17 16	15 9	8 -	- -	- 0
OBSOLETE	-	RESV	ON_FLY_GATE_ADJUST_E	RESV	PHY_GATE_SMPL2_SLAVE	-	-

Name	Bits	Default	Range	Description
ON_FLY_GATE_ADJUST_EN_2	17:16	0x0	0x0-0x3	Control the on the fly gate
PHY_GATE_SMPL2_SLAVE_DELAY_2	8:0	0x000	0x0-0x1ff	Number of cycles to delay the read DQS gate signal to generate gate2

DENALI_PHY_270 (Address PHY_BASE_ADDR + 270)

31 -	- -	- -	- -	- -	- -	- -	- 0
PHY_GATE_TRACKING_OB	-	-	-	-	-	-	-

Name	Bits	Default	Range	Description
PHY_GATE_TRACKING_OBS_2	31:0	0x00000000	0x0-0xffffffff	Report the on the fly gate

DENALI_PHY_271 (Address PHY_BASE_ADDR + 271)

31 -	- -	- -	- 16	15 10	9 8	7 1	0 0
OBSOLETE	-	-	-	RESV	PHY_LP4_PST_AMBLE_2	RESV	PHY_DFI40_P

Name	Bits	Default	Range	Description
PHY_LP4_PST_AMBLE_2	9:8	0x0	0x0-0x3	Controls the read postamble

PHY_DFI40_POLARITY_2	0	0x0	0x0-0x1	Indicates the dfi_wrdata_cs_n and dfi_rddata_cs_n is low active or

DENALI_PHY_272 (Address PHY_BASE_ADDR + 272)

31 -	-	-	-	-	-	-	-	-	-	0
PHY_LP4_RDL	-	-	-	-	-	-	-			

Name	Bits	Default	Range	Description
PHY_LP4_RDLVL_PATT8_2	31:0	0x00000000	0x0-0xffffffff	LPDDR4 read leveling pattern 8

DENALI_PHY_273 (Address PHY_BASE_ADDR + 273)

31 -	-	-	-	-	-	-	-	-	-	0
PHY_LP4_RDL	-	-	-	-	-	-	-			

Name	Bits	Default	Range	Description
PHY_LP4_RDLVL_PATT9_2	31:0	0x000000	0x0-0xffffffff	LPDDR4 read leveling pattern 9

DENALI_PHY_274 (Address PHY_BASE_ADDR + 274)

31 -	-	-	-	-	-	-	-	-	-	0
PHY_LP4_RDL	-	-	-	-	-	-	-			

Name	Bits	Default	Range	Description
PHY_LP4_RDLVL_PATT10_2	31:0	0x000000	0x0-0xffffffff	LPDDR4 read leveling pattern 10

DENALI_PHY_275 (Address PHY_BASE_ADDR + 275)

31 -	-	-	-	-	-	-	-	-	-	0
PHY_LP4_RDL	-	-	-	-	-	-	-			

Name	Bits	Default	Range	Description
PHY_LP4_RDLVL_PATT11_2	31:0	0x00000000	0x0-0xffffffff	LPDDR4 read leveling pattern 11

DENALI_PHY_276 (Address PHY_BASE_ADDR + 276)

31 27	26 24	23 19	18 16	15 9	8 8	7 3	2 0
RESV	PHY_RDDQ_ENC_OBS_SEL	RESV	PHY_MASTER_DLY_LOCK_OBS_SELECT	RESV	PHY_SW_FIFO_PTR_RST_	RESV	PHY_SLAVE_LOOP_CNT_UP

Name	Bits	Default	Range	Description
PHY_RDDQ_ENC_OBS_SELECT_2	26:24	0x0	0x0-0x7	Select value to map the internal read DQ slave delay encoded settings to the accessible read DQ
PHY_MASTER_DLY_LOCK_OBS_SELECT_2	18:16	0x0	0x0-0x7	Select value to map the internal master delay observation registers

PHY_SW_FIFO_PTR_RST_DISABLE_2	8	0x0	0x0-0x1	Disables automatic reset of the read entry FIFO pointers for slice 2.
PHY_SLAVE_LOOP_CNT_UPDATE_2	2:0	0x0	0x0-0x7	Sets the frequency by which the slave delay encoded value holding

DENALI_PHY_277 (Address PHY_BASE_ADDR + 277)

31 28	27 24	23 20	19 16	15 12	11 8	7 4	3 0
RESV	PHY_FIFO_PTR_OBS_SELE	RESV	PHY_WR_SHIFT_OBS_SEL	RESV	PHY_WR_ENC_OBS_SELECT_2	RESV	PHY_RDDQS_DQ_ENC_OBS

Name	Bits	Default	Range	Description
PHY_FIFO_PTR_OBS_SELECT_2	27:24	0x0	0x0-0xf	Select value to map the internal read entry FIFO read/write pointers to the accessible read entry FIFO
PHY_WR_SHIFT_OBS_SELECT_2	19:16	0x0	0x0-0xf	Select value to map the internal write DQ/DQS automatic cycle/ half_cycle shift settings to the
PHY_WR_ENC_OBS_SELECT_2	11:8	0x0	0x0-0xf	Select value to map the internal write DQ slave delay encoded settings to the accessible write DQ
PHY_RDDQS_DQ_ENC_OBS_SELECT_2	3:0	0x0	0x0-0xf	Select value to map the internal read DQS DQ rise/fall slave delay encoded settings to the accessible

DENALI_PHY_278 (Address PHY_BASE_ADDR + 278)

31 28	27 24	23 22	21 16	15 9	8 8	7 1	0 0
RESV	PHY_WRLVL_UPDT_WAIT	RESV	PHY_WRLVL_CAPTURE_CN	RESV	SC_PHY_LVL_DEBUG_CONT	RESV	PHY_LVL_DEBUG_MODE_2

Name	Bits	Default	Range	Description
PHY_WRLVL_UPDT_WAIT_CNT_2	27:24	0x0	0x0-0xf	Number of cycles to wait after changing DQS slave delay setting
PHY_WRLVL_CAPTURE_CNT_2	21:16	0x00	0x0-0x3f	Number of samples to take at each DQS slave delay setting during
SC_PHY_LVL_DEBUG_CONT_2	8	0x0	0x0-0x1	Allows the leveling state machine to advance (when in debug mode)
PHY_LVL_DEBUG_MODE_2	0	0x0	0x0-0x1	Enables leveling debug mode for

DENALI_PHY_279 (Address PHY_BASE_ADDR + 279)

31 28	27 24	23 22	21 16	15 12	11 8	7 6	5 0
RESV	PHY_RDLVL_UPDT_WAIT	RESV	PHY_RDLVL_CAPTURE_CN	RESV	PHY_GTLVL_UPDT_WAIT_C	RESV	PHY_GTLVL_CAPTURE_CNT

Name	Bits	Default	Range	Description
PHY_RDLVL_UPDT_WAIT_CNT_2	27:24	0x0	0x0-0xf	Number of cycles to wait after changing DQS slave delay setting

PHY_RDLVL_CAPTURE_CNT_2	21:16	0x00	0x0-0x3f	Number of samples to take at each DQS slave delay setting during
PHY_GTLVL_UPDT_WAIT_CNT_2	11:8	0x0	0x0-0xf	Number of cycles + 4 to wait after changing DQS slave delay setting
PHY_GTLVL_CAPTURE_CNT_2	5:0	0x00	0x0-0x3f	Number of samples to take at each DQS slave delay setting during

DENALI_PHY_280 (Address PHY_BASE_ADDR + 280)

31	30	29	24	23	-	-	16	15	13	12	8	7	2	1	0
RESV		PHY_WDQLVL_BURST_CNT_2		PHY_RDLVL_DATA_MASK_		-		RESV		PHY_RDLVL_RDDQS_DQ_		RESV		PHY_RDLVL_	

Name	Bits	Default	Range	Description
PHY_WDQLVL_BURST_CNT_2	29:24	0x00	0x0-0x3f	Defines the write/read burst length in bytes during the write data
PHY_RDLVL_DATA_MASK_2	23:16	0x00	0x0-0xff	Per-bit mask for read leveling for slice 2. If all bits are not used, only
PHY_RDLVL_RDDQS_DQ_OBS_SELECT_2	12:8	0x00	0x0-0x1f	Select value to map an individual DQ data window leading/trailing edge to the leading/trailing edge
PHY_RDLVL_OP_MODE_2	1:0	0x0	0x0-0x3	Read leveling algorithm select for slice 2. Clear to 0 to move linearly from left to right. Set to 1 to start

DENALI_PHY_281 (Address PHY_BASE_ADDR + 281)

31	28	27	24	23	19	18	-	-	-	-	8	7	3	2	0
RESV		PHY_WDQLVL_UPDT_WAIT_		RESV		PHY_WDQLVL_DQDM_SLV_DLY_JUMP_O		-		-		RESV		PHY_WDQLVL_PATT_2	

Name	Bits	Default	Range	Description
PHY_WDQLVL_UPDT_WAIT_CNT_2	27:24	0x0	0x0-0xf	Number of cycles to wait after changing the DQ slave delay
PHY_WDQLVL_DQDM_SLV_DLY_JUMP_OFFSET_2	18:8	0x000	0x0-0x7ff	Defines the write/read burst length in bytes during the write data
PHY_WDQLVL_PATT_2	2:0	0x0	0x0-0x7	Defines the training patterns to be used during the write data leveling sequence for slice 2. Bit (0) corresponds to the LFSR data training pattern. Bit (1) corresponds to the CLK data training pattern. Bit (2) corresponds to user-defined

DENALI_PHY_282 (Address PHY_BASE_ADDR + 282)

31	-	-	24	23	17	16	16	15	12	11	8	7	4	3	0

			SC_PHY_WD		PHY_WDQLVL		PHY_WDQLVL
OBSOLETE	-	RESV	QLVL_CLR_P	RESV	_QTR_DLY_ST	RESV	_DQDM_OBS_

Name	Bits	Default	Range	Description
SC_PHY_WDQLVL_CLR_PREV_RESULTS_2	16	0x0	0x0-0x1	Clears the previous result value to allow a clean slate comparison for future write DQ leveling results for
PHY_WDQLVL_QTR_DLY_STEP_2	11:8	0x0	0x0-0xf	Defines the step granularity for the logic to use once an edge is found. When this occurs, the logic jumps back to the previous invalid value
PHY_WDQLVL_DQDM_OBS_SELECT_2	3:0	0x0	0x0-0xf	Select value to map an individual DQ data window leading/trailing edge to the leading/trailing edge

DENALI_PHY_283 (Address PHY_BASE_ADDR + 283)

31 -	-	-	-	-	- 16	15 9	8	-	-	-	- 0
OBSOLETE	-	-	-	RESV			PHY_WDQLVL_DATADM_MA		-		-

Name	Bits	Default	Range	Description
PHY_WDQLVL_DATADM_MASK_2	8:0	0x000	0x0-0x1ff	Per-bit mask for write data leveling for slice 2. Set to 1 to mask any bit

DENALI_PHY_284 (Address PHY_BASE_ADDR + 284)

31 -	-	-	-	-	-	-	-	-	-	- 0
PHY_USER_P	-	-	-	-	-	-	-			

Name	Bits	Default	Range	Description
PHY_USER_PATT0_2	31:0	0x00000000	0x0-0xffffffff	User-defined pattern to be used during write data leveling for slice 2. This register holds the bytes 3 to 0 written/read from device.

DENALI_PHY_285 (Address PHY_BASE_ADDR + 285)

31 -	-	-	-	-	-	-	-	-	-	- 0
PHY_USER_P	-	-	-	-	-	-	-			

Name	Bits	Default	Range	Description
PHY_USER_PATT1_2	31:0	0x00000000	0x0-0xffffffff	User-defined pattern to be used during write data leveling for slice 2. This register holds the bytes 7 to 4 written/read from device.

DENALI_PHY_286 (Address PHY_BASE_ADDR + 286)

31 -	-	-	-	-	-	-	-	-	-	- 0
PHY_USER_P	-	-	-	-	-	-	-			

Name	Bits	Default	Range	Description
PHY_USER_PATT2_2	31:0	0x00000000	0x0-0xffffffff	User-defined pattern to be used during write data leveling for slice 2. This register holds the bytes 11 to 8 written/read from device.

DENALI_PHY_287 (Address PHY_BASE_ADDR + 287)

31 -	- -	- -	- -	- -	- -	- -	- 0
PHY_USER_P	-	-	-	-	-	-	-

Name	Bits	Default	Range	Description
PHY_USER_PATT3_2	31:0	0x00000000	0x0-0xffffffff	User-defined pattern to be used during write data leveling for slice 2. This register holds the bytes 15 to 12 written/read from device.

DENALI_PHY_288 (Address PHY_BASE_ADDR + 288)

31 30	29 24	23 17	16 16	15 -	- -	- -	- 0
RESV	SC_PHY_MANUAL_CLEAR_2	RESV	PHY_CALVL_VREF_DRIVING	PHY_USER_PATT4_2	-	-	-

Name	Bits	Default	Range	Description
SC_PHY_MANUAL_CLEAR_2	29:24	0x00	0x0-0x3f	Manual reset/clear of internal logic for slice 2. Bit (0) initiates manual setup of the read DQS gate. Bit (1) is reset of read entry FIFO pointers. Bit (2) is reset of master delay min/ max lock values. Bit (3) is manual reset of master delay unlock
PHY_CALVL_VREF_DRIVING_SLICE_2	16	0x0	0x0-0x1	Indicates if slice 2 is used to drive the VREF value to the device
PHY_USER_PATT4_2	15:0	0x0000	0x0-0xffff	User-defined pattern to be used during write data leveling for slice 2. This register holds the DM bit for

DENALI_PHY_289 (Address PHY_BASE_ADDR + 289)

31 -	- -	- -	- -	- -	- 8	7 -	- 0
OBSOLETE	-	-	-	-	PHY_FIFO_PT		-

Name	Bits	Default	Range	Description
PHY_FIFO_PTR_OBS_2	7:0	0x00	0x0-0xff	Observation register for read entry FIFO pointers for slice 2. READ-

DENALI_PHY_290 (Address PHY_BASE_ADDR + 290)

31 -	- -	- -	- -	- -	- -	- -	- 0
PHY_LPBK_R	-	-	-	-	-	-	-

Name	Bits	Default	Range	Description

PHY_LPBK_RESULT_OBS_2	31:0	0x00000000	0x0-0xffffffff	Observation register containing loopback status/results for slice 2.

DENALI_PHY_291 (Address PHY_BASE_ADDR + 291)

31 - 26	25 - 16	15 - 0
RESV	PHY_MASTER_DLY_LOCK_OBS_2	PHY_LPBK_ERROR_COUN

Name	Bits	Default	Range	Description
PHY_MASTER_DLY_LOCK_OBS_2	25:16	0x000	0x0-0x3ff	Observation register for master delay results for slice 2. READ-
PHY_LPBK_ERROR_COUNT_OBS_2	15:0	0x0000	0x0-0xffff	Observation register containing total number of loopback error data

DENALI_PHY_292 (Address PHY_BASE_ADDR + 292)

31 - 24	23 - 16	15 - 15	14 - 8	7 - 6	5 - 0
PHY_RDDQS_DQ_FALL_ADD	PHY_RDDQS_DQ_RISE_AD	RESV	PHY_RDDQS_BASE_SLV_DL	RESV	PHY_RDDQ_SLV_DLY_ENC_

Name	Bits	Default	Range	Description
PHY_RDDQS_DQ_FALL_ADDER_SLV_DL	31:24	0x00	0x0-0xff	Observation register for read DQS DQ falling edge adder slave delay
PHY_RDDQS_DQ_RISE_ADDER_SLV_DL	23:16	0x00	0x0-0xff	Observation register for read DQS DQ rising edge adder slave delay
PHY_RDDQS_BASE_SLV_DLY_ENC_OBS_2	14:8	0x00	0x0-0x7f	Observation register for read DQS base slave delay encoded value for
PHY_RDDQ_SLV_DLY_ENC_OBS_2	5:0	0x00	0x0-0x3f	Observation register for read DQ slave delay encoded values for

DENALI_PHY_293 (Address PHY_BASE_ADDR + 293)

31 - 24	23 - 23	22 - 16	15 - 10	9 - 0
PHY_WRDQ_BASE_SLV_DL	RESV	PHY_WRDQS_BASE_SLV_DLY_ENC_OBS	RESV	PHY_RDDQS_GATE_SLV_DL

Name	Bits	Default	Range	Description
PHY_WRDQ_BASE_SLV_DLY_ENC_OBS_2	31:24	0x00	0x0-0xff	Observation register for write DQ base slave delay encoded value for
PHY_WRDQS_BASE_SLV_DLY_ENC_OBS_2	22:16	0x00	0x0-0x7f	Observation register for write DQS base slave delay encoded value for
PHY_RDDQS_GATE_SLV_DLY_ENC_OBS_2	9:0	0x000	0x0-0x3ff	Observation register for read DQS gate slave delay encoded value for

DENALI_PHY_294 (Address PHY_BASE_ADDR + 294)

31 - 26	25 - 16	15 - 11	10 - 8	7 - 0
RESV	PHY_WRLVL_HARD0_DELA	RESV	PHY_WR_SHIFT_OBS_2	PHY_WR_ADDER_SLV_DLY

Name	Bits	Default	Range	Description
PHY_WRLVL_HARD0_DELAY_OBS_2	25:16	0x000	0x0-0x3ff	Observation register for write leveling last hard 0 DQS slave
PHY_WR_SHIFT_OBS_2	10:8	0x0	0x0-0x7	Observation register for automatic half cycle and cycle shift values for
PHY_WR_ADDER_SLV_DLY_ENC_OBS_2	7:0	0x00	0x0-0xff	Observation register for write adder slave delay encoded value for slice

DENALI_PHY_295 (Address PHY_BASE_ADDR + 295)

31 - 16	15 10	9 - 0
OBSOLETE	RESV	PHY_WRLVL_HARD1_DELA

Name	Bits	Default	Range	Description
PHY_WRLVL_HARD1_DELAY_OBS_2	9:0	0x000	0x0-0x3ff	Observation register for write leveling first hard 1 DQS slave

DENALI_PHY_296 (Address PHY_BASE_ADDR + 296)

31 - 24	23 17	16 - 0
OBSOLETE	RESV	PHY_WRLVL_STATUS_OBS

Name	Bits	Default	Range	Description
PHY_WRLVL_STATUS_OBS_2	16:0	0x00000	0x0-0x1ffff	Observation register for write leveling status for slice 2. READ-

DENALI_PHY_297 (Address PHY_BASE_ADDR + 297)

31 25	24 - 16	15 9	8 - 0
RESV	PHY_GATE_SMPL2_SLV_DL	RESV	PHY_GATE_SMPL1_SLV_DL

Name	Bits	Default	Range	Description
PHY_GATE_SMPL2_SLV_DLY_ENC_OBS_2	24:16	0x000	0x0-0x1ff	Observation register for gate sample1 slave delay encoded
PHY_GATE_SMPL1_SLV_DLY_ENC_OBS_2	8:0	0x000	0x0-0x1ff	Observation register for gate sample1 slave delay encoded

DENALI_PHY_298 (Address PHY_BASE_ADDR + 298)

31 30	29 - 16	15 - 0
RESV	PHY_GTLVL_HARD0_DELAY	PHY_WRLVL_ERROR_OBS

Name	Bits	Default	Range	Description
PHY_GTLVL_HARD0_DELAY_OBS_2	29:16	0x0000	0x0-0x3fff	Observation register for gate training first hard 0 DQS slave

PHY_WRLVL_ERROR_OBS_2	15:0	0x0000	0x0-0xffff	Observation register for write leveling error status for slice 2.

DENALI_PHY_299 (Address PHY_BASE_ADDR + 299)

31 28	27 - - - - 16	15 14	13 - - - - 0
RESV	PHY_GTLVL_STATUS_OBS_2	RESV	PHY_GTLVL_HARD1_DELAY

Name	Bits	Default	Range	Description
PHY_GTLVL_STATUS_OBS_2	27:16	0x000	0x0-0xfff	Observation register for gate training status for slice 2. READ-
PHY_GTLVL_HARD1_DELAY_OBS_2	13:0	0x0000	0x0-0x3fff	Observation register for gate training last hard 1 DQS slave

DENALI_PHY_300 (Address PHY_BASE_ADDR + 300)

31 26	25 - - - - 16	15 10	9 - - - - 0
RESV	PHY_RDLVL_RDDQS_DQ_TE	RESV	PHY_RDLVL_RDDQS_DQ_L

Name	Bits	Default	Range	Description
PHY_RDLVL_RDDQS_DQ_TE_DLY_OBS_	25:16	0x000	0x0-0x3ff	Observation register for read leveling data window trailing edge
PHY_RDLVL_RDDQS_DQ_LE_DLY_OBS_2	9:0	0x000	0x0-0x3ff	Observation register for read leveling data window leading edge

DENALI_PHY_301 (Address PHY_BASE_ADDR + 301)

31 - - - - - - - - 8	7 2	1 0
OBSOLETE	RESV	PHY_RDLVL_RDDQS_DQ_N

Name	Bits	Default	Range	Description
PHY_RDLVL_RDDQS_DQ_NUM_WINDOWS_OBS_2	1:0	0x0	0x0-0x3	Observation register for read leveling number of windows found

DENALI_PHY_302 (Address PHY_BASE_ADDR + 302)

31 - - - - - - - - - - - - - - - -	0
PHY_RDLVL_STATUS_OBS	

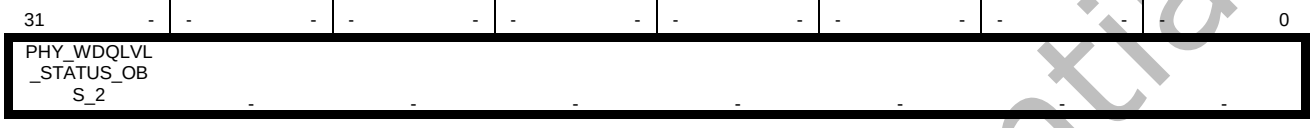
Name	Bits	Default	Range	Description
PHY_RDLVL_STATUS_OBS_2	31:0	0x00000000	0x0-0xffffffff	Observation register for read leveling status for slice 2. READ-

DENALI_PHY_303 (Address PHY_BASE_ADDR + 303)

31 27	26 - - - - 16	15 11	10 - - - - 0

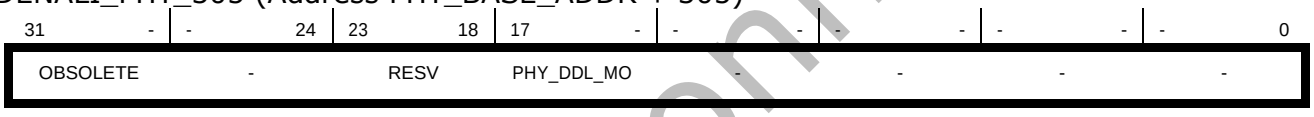
Name	Bits	Default	Range	Description
PHY_WDQLVL_DQDM_TE_DLY_OBS_2	26:16	0x000	0x0-0x7ff	Observation register for write data leveling data window trailing edge
PHY_WDQLVL_DQDM_LE_DLY_OBS_2	10:0	0x000	0x0-0x7ff	Observation register for write data leveling data window leading edge

DENALI_PHY_304 (Address PHY_BASE_ADDR + 304)



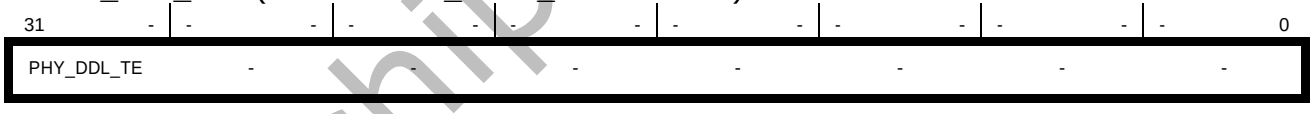
Name	Bits	Default	Range	Description
PHY_WDQLVL_STATUS_OBS_2	31:0	0x00000000	0x0-0xffffffff	Observation register for write data leveling status for slice 2. READ-

DENALI_PHY_305 (Address PHY_BASE_ADDR + 305)



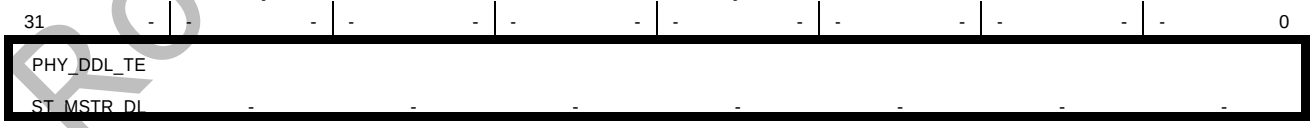
Name	Bits	Default	Range	Description
PHY_DDL_MODE_2	17:0	0x00000	0x0-0x3ffff	DDL mode for slice 2.

DENALI_PHY_306 (Address PHY_BASE_ADDR + 306)



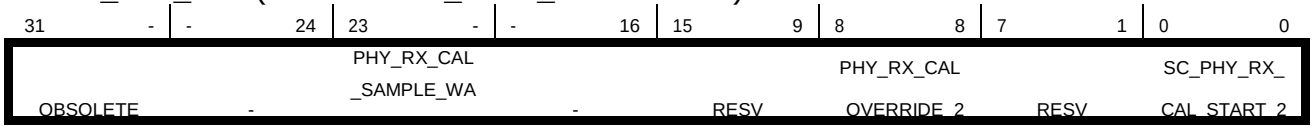
Name	Bits	Default	Range	Description
PHY_DDL_TEST_OBS_2	31:0	0x00000000	0x0-0xffffffff	DDL test observation for slice 2.

DENALI_PHY_307 (Address PHY_BASE_ADDR + 307)



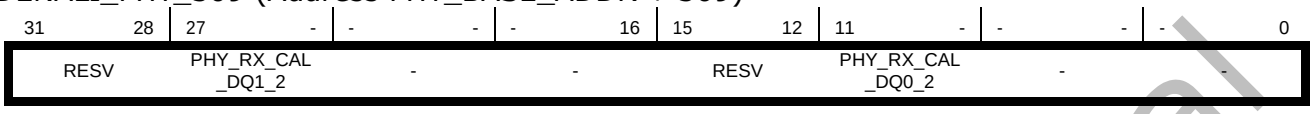
Name	Bits	Default	Range	Description
PHY_DDL_TEST_MSTR_DLY_OBS_2	31:0	0x000000	0x0-0xffffffff	DDL test observation delays for

DENALI_PHY_308 (Address PHY_BASE_ADDR + 308)



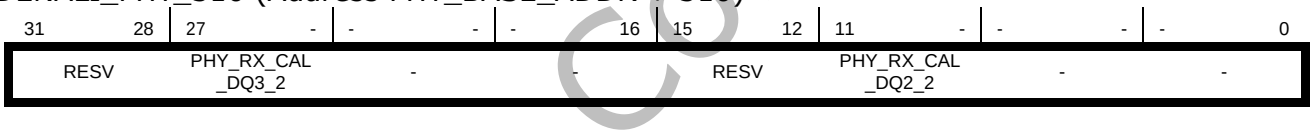
Name	Bits	Default	Range	Description
PHY_RX_CAL_SAMPLE_WAIT_2	23:16	0x00	0x0-0xff	RX Calibration state machine wait
PHY_RX_CAL_OVERRIDE_2	8	0x0	0x0-0x1	Manual setting of RX Calibration
SC_PHY_RX_CAL_START_2	0	0x0	0x0-0x1	Manual RX Calibration start for

DENALI_PHY_309 (Address PHY_BASE_ADDR + 309)



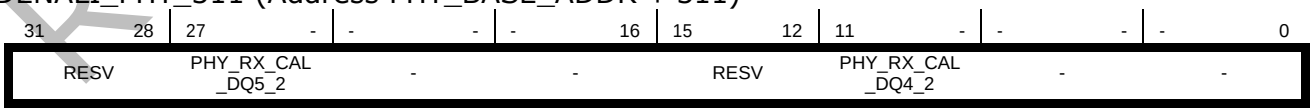
Name	Bits	Default	Range	Description
PHY_RX_CAL_DQ1_2	27:16	0x000	0x0-0xfff	RX Calibration codes for DQ1 for slice 2. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits
PHY_RX_CAL_DQ0_2	11:0	0x000	0x0-0xfff	RX Calibration codes for DQ0 for slice 2. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits

DENALI_PHY_310 (Address PHY_BASE_ADDR + 310)



Name	Bits	Default	Range	Description
PHY_RX_CAL_DQ3_2	27:16	0x000	0x0-0xfff	RX Calibration codes for DQ3 for slice 2. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits
PHY_RX_CAL_DQ2_2	11:0	0x000	0x0-0xfff	RX Calibration codes for DQ2 for slice 2. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits

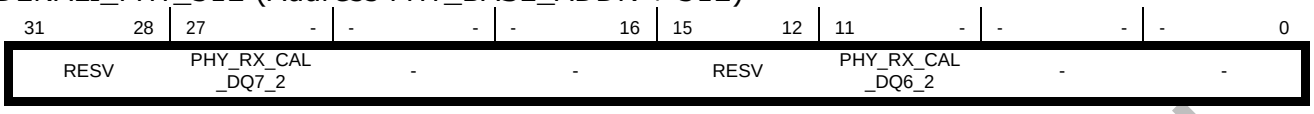
DENALI_PHY_311 (Address PHY_BASE_ADDR + 311)



Name	Bits	Default	Range	Description
PHY_RX_CAL_DQ5_2	27:16	0x000	0x0-0xfff	RX Calibration codes for DQ5 for slice 2. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits

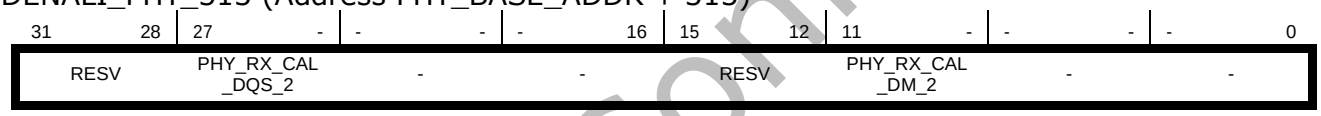
PHY_RX_CAL_DQ4_2	11:0	0x000	0x0-0xfff	RX Calibration codes for DQ4 for slice 2. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits

DENALI_PHY_312 (Address PHY_BASE_ADDR + 312)



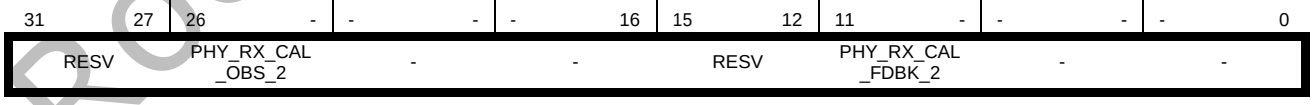
Name	Bits	Default	Range	Description
PHY_RX_CAL_DQ7_2	27:16	0x000	0x0-0xfff	RX Calibration codes for DQ7 for slice 2. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits
PHY_RX_CAL_DQ6_2	11:0	0x000	0x0-0xfff	RX Calibration codes for DQ6 for slice 2. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits

DENALI_PHY_313 (Address PHY_BASE_ADDR + 313)



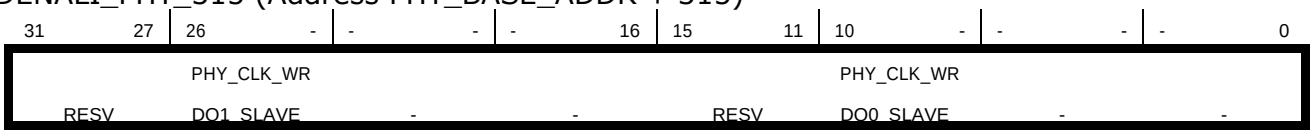
Name	Bits	Default	Range	Description
PHY_RX_CAL_DQS_2	27:16	0x000	0x0-0xfff	RX Calibration codes for DQS for slice 2. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits
PHY_RX_CAL_DM_2	11:0	0x000	0x0-0xfff	RX Calibration codes for DM for slice 2. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits

DENALI_PHY_314 (Address PHY_BASE_ADDR + 314)



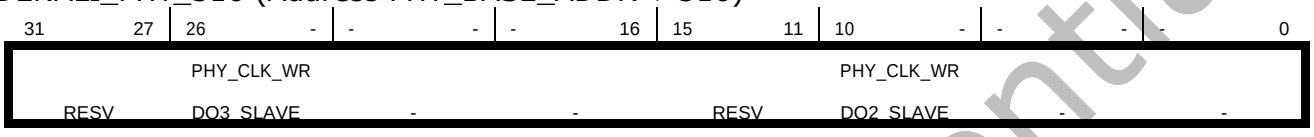
Name	Bits	Default	Range	Description
PHY_RX_CAL_OBS_2	26:16	0x000	0x0-0x7ff	RX Calibration results for slice 2. Bits (7:0) contain calibration results from DQ0-7. Bit (8) contains calibration result from DM. Bit (9)
PHY_RX_CAL_FDBK_2	11:0	0x000	0x0-0xfff	RX Calibration codes for FDBK for slice 2. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits

DENALI_PHY_315 (Address PHY_BASE_ADDR + 315)



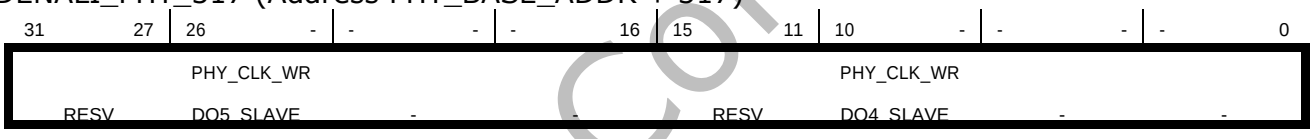
Name	Bits	Default	Range	Description
PHY_CLK_WRDQ1_SLAVE_DELAY_2	26:16	0x000	0x0-0x7ff	Write clock slave delay setting for
PHY_CLK_WRDQ0_SLAVE_DELAY_2	10:0	0x000	0x0-0x7ff	Write clock slave delay setting for

DENALI_PHY_316 (Address PHY_BASE_ADDR + 316)



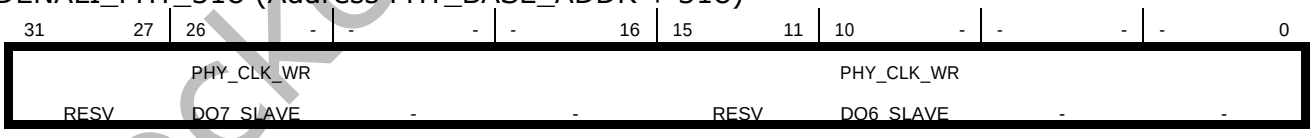
Name	Bits	Default	Range	Description
PHY_CLK_WRDQ3_SLAVE_DELAY_2	26:16	0x000	0x0-0x7ff	Write clock slave delay setting for
PHY_CLK_WRDQ2_SLAVE_DELAY_2	10:0	0x000	0x0-0x7ff	Write clock slave delay setting for

DENALI_PHY_317 (Address PHY_BASE_ADDR + 317)



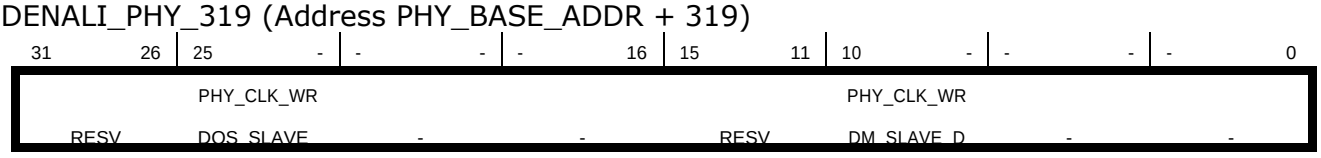
Name	Bits	Default	Range	Description
PHY_CLK_WRDQ5_SLAVE_DELAY_2	26:16	0x000	0x0-0x7ff	Write clock slave delay setting for
PHY_CLK_WRDQ4_SLAVE_DELAY_2	10:0	0x000	0x0-0x7ff	Write clock slave delay setting for

DENALI_PHY_318 (Address PHY_BASE_ADDR + 318)



Name	Bits	Default	Range	Description
PHY_CLK_WRDQ7_SLAVE_DELAY_2	26:16	0x000	0x0-0x7ff	Write clock slave delay setting for
PHY_CLK_WRDQ6_SLAVE_DELAY_2	10:0	0x000	0x0-0x7ff	Write clock slave delay setting for

DENALI_PHY_319 (Address PHY_BASE_ADDR + 319)



Name	Bits	Default	Range	Description

PHY_CLK_WRDQS_SLAVE_DELAY_2	25:16	0x000	0x0-0x3ff	Write clock slave delay setting for
PHY_CLK_WRDM_SLAVE_DELAY_2	10:0	0x000	0x0-0x7ff	Write clock slave delay setting for

DENALI_PHY_320 (Address PHY_BASE_ADDR + 320)

31	26	25	-	-	-	-	16	15	10	9	-	-	-	-	0
		PHY_RDDQ1_								PHY_RDDQ0_					
RESV		SLAVE_DELAY		-		-		RESV		SLAVE_DELAY		-		-	

Name	Bits	Default	Range	Description
PHY_RDDQ1_SLAVE_DELAY_2	25:16	0x000	0x0-0x3ff	Read DQ1 slave delay setting for
PHY_RDDQ0_SLAVE_DELAY_2	9:0	0x000	0x0-0x3ff	Read DQ0 slave delay setting for

DENALI_PHY_321 (Address PHY_BASE_ADDR + 321)

31	26	25	-	-	-	-	16	15	10	9	-	-	-	-	0
		PHY_RDDQ3_								PHY_RDDQ2_					
RESV		SLAVE_DELAY		-		-		RESV		SLAVE_DELAY		-		-	

Name	Bits	Default	Range	Description
PHY_RDDQ3_SLAVE_DELAY_2	25:16	0x000	0x0-0x3ff	Read DQ3 slave delay setting for
PHY_RDDQ2_SLAVE_DELAY_2	9:0	0x000	0x0-0x3ff	Read DQ2 slave delay setting for

DENALI_PHY_322 (Address PHY_BASE_ADDR + 322)

31	26	25	-	-	-	-	16	15	10	9	-	-	-	-	0
		PHY_RDDQ5_								PHY_RDDQ4_					
RESV		SLAVE_DELAY		-		-		RESV		SLAVE_DELAY		-		-	

Name	Bits	Default	Range	Description
PHY_RDDQ5_SLAVE_DELAY_2	25:16	0x000	0x0-0x3ff	Read DQ5 slave delay setting for
PHY_RDDQ4_SLAVE_DELAY_2	9:0	0x000	0x0-0x3ff	Read DQ4 slave delay setting for

DENALI_PHY_323 (Address PHY_BASE_ADDR + 323)

31	26	25	-	-	-	-	16	15	10	9	-	-	-	-	0
		PHY_RDDQ7_								PHY_RDDQ6_					
RESV		SLAVE_DELAY		-		-		RESV		SLAVE_DELAY		-		-	

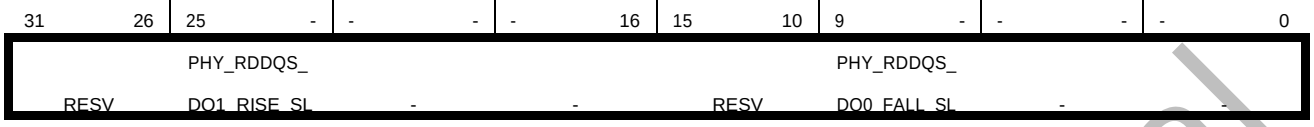
Name	Bits	Default	Range	Description
PHY_RDDQ7_SLAVE_DELAY_2	25:16	0x000	0x0-0x3ff	Read DQ7 slave delay setting for
PHY_RDDQ6_SLAVE_DELAY_2	9:0	0x000	0x0-0x3ff	Read DQ6 slave delay setting for

DENALI_PHY_324 (Address PHY_BASE_ADDR + 324)

31	26	25	-	-	-	-	16	15	10	9	-	-	-	-	0
		PHY_RDDQS_								PHY_RDDM_S					
RESV		DQ0_RISE_SL		-		-		RESV		LAVE_DELAY		-		-	

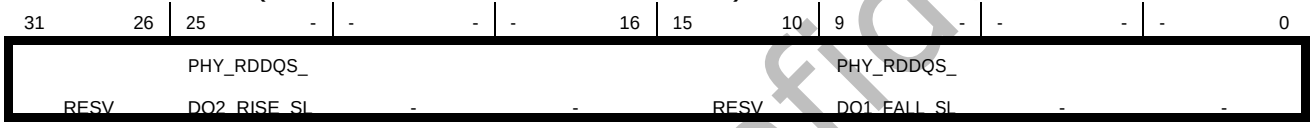
Name	Bits	Default	Range	Description
PHY_RDDQS_DQ0_RISE_SLAVE_DELAY_	25:16	0x000	0x0-0x3ff	Rising edge read DQS slave delay
PHY_RDDM_SLAVE_DELAY_2	9:0	0x000	0x0-0x3ff	Read DM/DBI slave delay setting for slice 2. May be used for data

DENALI_PHY_325 (Address PHY_BASE_ADDR + 325)



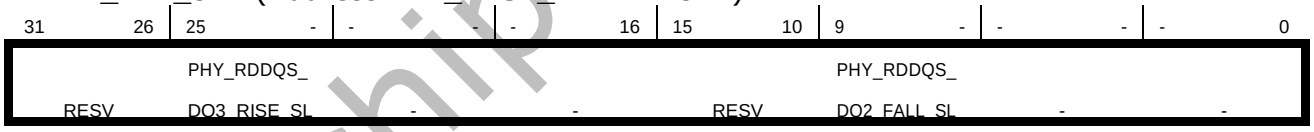
Name	Bits	Default	Range	Description
PHY_RDDQS_DQ1_RISE_SLAVE_DELAY_	25:16	0x000	0x0-0x3ff	Rising edge read DQS slave delay
PHY_RDDQS_DQ0_FALL_SLAVE_DELAY_	9:0	0x000	0x0-0x3ff	Falling edge read DQS slave delay

DENALI_PHY_326 (Address PHY_BASE_ADDR + 326)



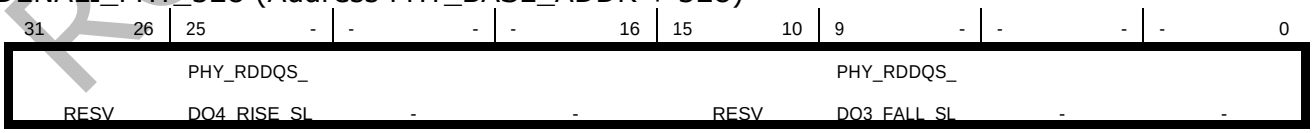
Name	Bits	Default	Range	Description
PHY_RDDQS_DQ2_RISE_SLAVE_DELAY_	25:16	0x000	0x0-0x3ff	Rising edge read DQS slave delay
PHY_RDDQS_DQ1_FALL_SLAVE_DELAY_	9:0	0x000	0x0-0x3ff	Falling edge read DQS slave delay

DENALI_PHY_327 (Address PHY_BASE_ADDR + 327)



Name	Bits	Default	Range	Description
PHY_RDDQS_DQ3_RISE_SLAVE_DELAY_	25:16	0x000	0x0-0x3ff	Rising edge read DQS slave delay
PHY_RDDQS_DQ2_FALL_SLAVE_DELAY_	9:0	0x000	0x0-0x3ff	Falling edge read DQS slave delay

DENALI_PHY_328 (Address PHY_BASE_ADDR + 328)



Name	Bits	Default	Range	Description
PHY_RDDQS_DQ4_RISE_SLAVE_DELAY_	25:16	0x000	0x0-0x3ff	Rising edge read DQS slave delay
PHY_RDDQS_DQ3_FALL_SLAVE_DELAY_	9:0	0x000	0x0-0x3ff	Falling edge read DQS slave delay

DENALI_PHY_329 (Address PHY_BASE_ADDR + 329)

31	26	25	-	-	-	-	16	15	10	9	-	-	-	-	0
RESV		PHY_RDDQS_DQ5_RISE_SL		-		-		RESV		PHY_RDDQS_DQ4_FALL_SL		-		-	

Name	Bits	Default	Range	Description
PHY_RDDQS_DQ5_RISE_SLAVE_DELAY_	25:16	0x000	0x0-0x3ff	Rising edge read DQS slave delay
PHY_RDDQS_DQ4_FALL_SLAVE_DELAY_	9:0	0x000	0x0-0x3ff	Falling edge read DQS slave delay

DENALI_PHY_330 (Address PHY_BASE_ADDR + 330)

31	26	25	-	-	-	-	16	15	10	9	-	-	-	-	0
RESV		PHY_RDDQS_DQ6_RISE_SL		-		-		RESV		PHY_RDDQS_DQ5_FALL_SL		-		-	

Name	Bits	Default	Range	Description
PHY_RDDQS_DQ6_RISE_SLAVE_DELAY_	25:16	0x000	0x0-0x3ff	Rising edge read DQS slave delay
PHY_RDDQS_DQ5_FALL_SLAVE_DELAY_	9:0	0x000	0x0-0x3ff	Falling edge read DQS slave delay

DENALI_PHY_331 (Address PHY_BASE_ADDR + 331)

31	26	25	-	-	-	-	16	15	10	9	-	-	-	-	0
RESV		PHY_RDDQS_DQ7_RISE_SL		-		-		RESV		PHY_RDDQS_DQ6_FALL_SL		-		-	

Name	Bits	Default	Range	Description
PHY_RDDQS_DQ7_RISE_SLAVE_DELAY_	25:16	0x000	0x0-0x3ff	Rising edge read DQS slave delay
PHY_RDDQS_DQ6_FALL_SLAVE_DELAY_	9:0	0x000	0x0-0x3ff	Falling edge read DQS slave delay

DENALI_PHY_332 (Address PHY_BASE_ADDR + 332)

31	26	25	-	-	-	-	16	15	10	9	-	-	-	-	0
RESV		PHY_RDDQS_DM_RISE_SLA		-		-		RESV		PHY_RDDQS_DQ7_FALL_SL		-		-	

Name	Bits	Default	Range	Description
PHY_RDDQS_DM_RISE_SLAVE_DELAY_2	25:16	0x000	0x0-0x3ff	Rising edge read DQS slave delay
PHY_RDDQS_DQ7_FALL_SLAVE_DELAY_	9:0	0x000	0x0-0x3ff	Falling edge read DQS slave delay

DENALI_PHY_333 (Address PHY_BASE_ADDR + 333)

31	26	25	-	-	-	-	16	15	10	9	-	-	-	-	0
RESV		PHY_RDDQS_GATE_SLAVE		-		-		RESV		PHY_RDDQS_DM_FALL_SLA		-		-	

Name	Bits	Default	Range	Description
PHY_RDDQS_GATE_SLAVE_DELAY_2	25:16	0x000	0x0-0x3ff	Read DQS slave delay setting for
PHY_RDDQS_DM_FALL_SLAVE_DELAY_2	9:0	0x000	0x0-0x3ff	Falling edge read DQS slave delay

DENALI_PHY_334 (Address PHY_BASE_ADDR + 334)

31 26	25 - 16	15 11	10 8	7 4	3 0
RESV	PHY_WRLVL_DELAY_EARLY_THRESHOLD_2	RESV	PHY_WRITE_PATH_LAT_ADD_2	RESV	PHY_RDDQS_LATENCY_ADJUST_2

Name	Bits	Default	Range	Description
PHY_WRLVL_DELAY_EARLY_THRESHOLD_2	25:16	0x000	0x0-0x3ff	Write level delay threshold above which will be considered in
PHY_WRITE_PATH_LAT_ADD_2	10:8	0x0	0x0-0x7	Number of cycles to delay the incoming dfi_wrdata_en/dfi_wrdata
PHY_RDDQS_LATENCY_ADJUST_2	3:0	0x0	0x0-0xf	Number of cycles to delay the incoming dfi_rddata_en for read

DENALI_PHY_335 (Address PHY_BASE_ADDR + 335)

31 24	23 17	16 16	15 10	9 0
OBSOLETE	RESV	PHY_WRLVL_EARLY_FORCE_ZERO_2	RESV	PHY_WRLVL_DELAY_PERIOD_THRESHOLD_2

Name	Bits	Default	Range	Description
PHY_WRLVL_EARLY_FORCE_ZERO_2	16	0x0	0x0-0x1	Force the final write level delay value (that meets the early
PHY_WRLVL_DELAY_PERIOD_THRESHOLD_2	9:0	0x000	0x0-0x3ff	Write level delay threshold below which will add a cycle of write path

DENALI_PHY_336 (Address PHY_BASE_ADDR + 336)

31 24	23 20	19 16	15 10	9 0
OBSOLETE	RESV	PHY_GTLVL_LAT_ADJ_START_2	RESV	PHY_GTLVL_RDDQS_SLV_DLY_START_2

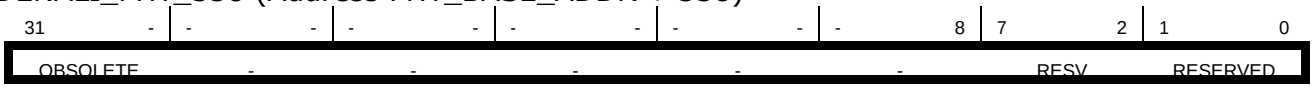
Name	Bits	Default	Range	Description
PHY_GTLVL_LAT_ADJ_START_2	19:16	0x0	0x0-0xf	Initial read DQS gate cycle delay from dfi_rddata_en during gate
PHY_GTLVL_RDDQS_SLV_DLY_START_2	9:0	0x000	0x0-0x3ff	Initial read DQS gate slave delay setting during gate training for slice

DENALI_PHY_337 (Address PHY_BASE_ADDR + 337)

31 26	25 - 16	15 11	10 - 0
RESV	PHY_RDLVL_RDDQS_DQ_SLV_DLY_START_2	RESV	PHY_WDQLVL_DQDM_SLV_DLY_START_2

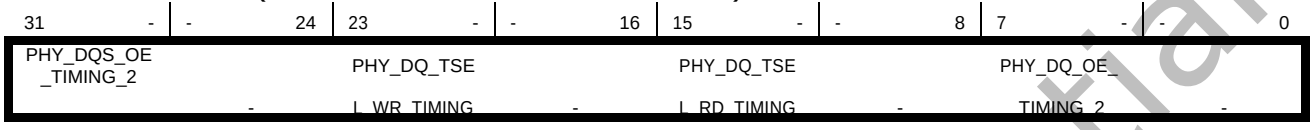
Name	Bits	Default	Range	Description
PHY_RDLVL_RDDQS_DQ_SLV_DLY_START_2	25:16	0x000	0x0-0x3ff	Read leveling starting value for the DQS/DQ slave delay settings for
PHY_WDQLVL_DQDM_SLV_DLY_START_2	10:0	0x000	0x0-0x7ff	Initial DQ/DM slave delay setting during write data leveling for slice

DENALI_PHY_338 (Address PHY_BASE_ADDR + 338)



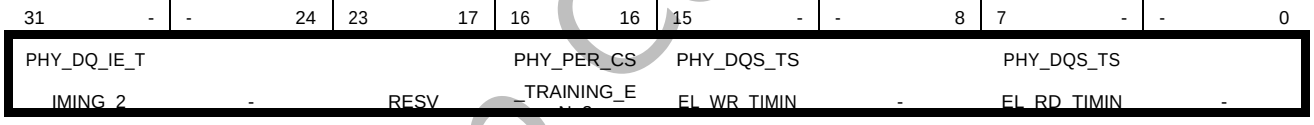
Name	Bits	Default	Range	Description
RESERVED	1:0	0x0	0x0-0x3	Reserved for future use. Refer to the regconfig files for the default

DENALI_PHY_339 (Address PHY_BASE_ADDR + 339)



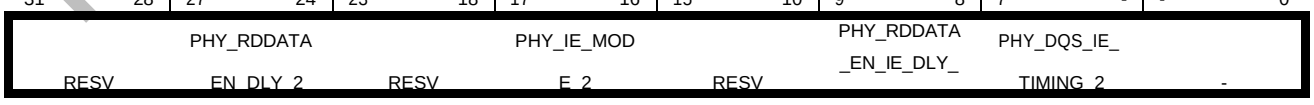
Name	Bits	Default	Range	Description
PHY_DQS_OE_TIMING_2	31:24	0x00	0x0-0xff	Start/end timing values for DQS
PHY_DQ_TSEL_WR_TIMING_2	23:16	0x00	0x0-0xff	Start/end timing values for DQ/DM write based termination enable and
PHY_DQ_TSEL_RD_TIMING_2	15:8	0x00	0x0-0xff	Start/end timing values for DQ/DM read based termination enable and
PHY_DQ_OE_TIMING_2	7:0	0x00	0x0-0xff	Start/end timing values for DQ/DM

DENALI_PHY_340 (Address PHY_BASE_ADDR + 340)



Name	Bits	Default	Range	Description
PHY_DQ_IE_TIMING_2	31:24	0x00	0x0-0xff	Start/end timing values for DQ/DM
PHY_PER_CS_TRAINING_EN_2	16	0x0	0x0-0x1	Enables the per-rank training and read/write timing capabilities. Must
PHY_DQS_TSEL_WR_TIMING_2	15:8	0x00	0x0-0xff	Start/end timing values for DQS write based termination enable and
PHY_DQS_TSEL_RD_TIMING_2	7:0	0x00	0x0-0xff	Start/end timing values for DQS read based termination enable and

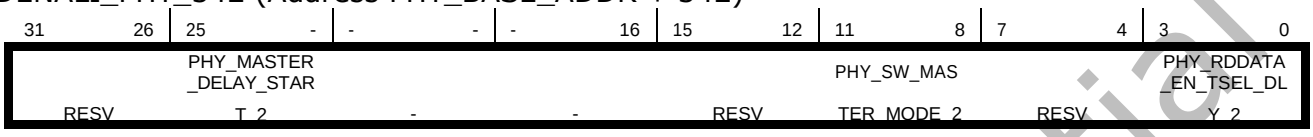
DENALI_PHY_341 (Address PHY_BASE_ADDR + 341)



Name	Bits	Default	Range	Description
PHY_RDDATA_EN_DLY_2	27:24	0x0	0x0-0xf	Number of cycles that the dfi_rddata_en signal is early for

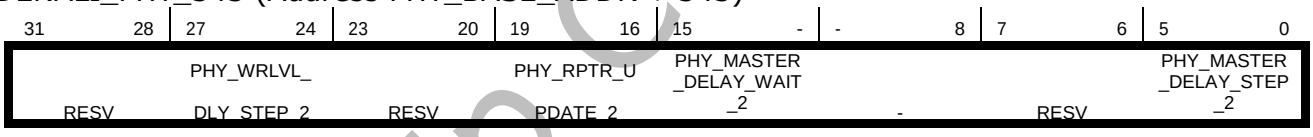
PHY_IE_MODE_2	17:16	0x0	0x0-0x3	Input enable mode bits for slice 2. Bit (0) enables the mode where the input enables are always on; set to
PHY_RDDATA_EN_IE_DLY_2	9:8	0x0	0x0-0x3	Number of cycles that the dfi_rddata_en signal is earlier than
PHY_DQS_IE_TIMING_2	7:0	0x00	0x0-0xff	Start/end timing values for DQS

DENALI_PHY_342 (Address PHY_BASE_ADDR + 342)



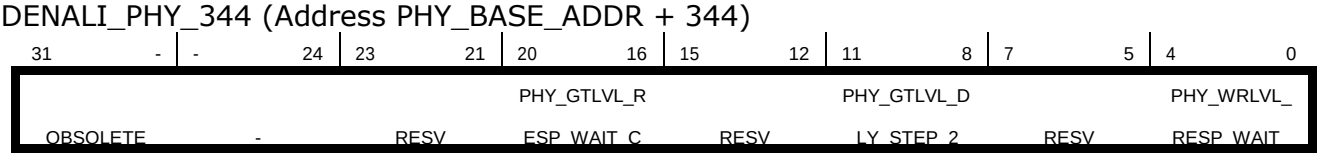
Name	Bits	Default	Range	Description
PHY_MASTER_DELAY_START_2	25:16	0x000	0x0-0x3ff	Start value for master delay line
PHY_SW_MASTER_MODE_2	11:8	0x0	0x0-0xf	Master delay line override settings for slice 2. Bit (0) enables software half clock mode. Bit (1) is the software half clock mode value. Bit
PHY_RDDATA_EN_TSEL_DLY_2	3:0	0x0	0x0-0xf	Number of cycles that the dfi_rddata_en signal is earlier than

DENALI_PHY_343 (Address PHY_BASE_ADDR + 343)



Name	Bits	Default	Range	Description
PHY_WRLVL_DLY_STEP_2	27:24	0x0	0x0-0xf	DQS slave delay step size during
PHY_RPTR_UPDATE_2	19:16	0x0	0x0-0xf	Offset in cycles from the dfi_rddata_en signal to release
PHY_MASTER_DELAY_WAIT_2	15:8	0x00	0x0-0xff	Wait cycles for master delay line locking algorithm for slice 2. Bits (3:0) are the cycle wait count after a calibration clock setting change.
PHY_MASTER_DELAY_STEP_2	5:0	0x00	0x0-0x3f	Incremental step size for master delay line locking algorithm for slice

DENALI_PHY_344 (Address PHY_BASE_ADDR + 344)



Name	Bits	Default	Range	Description

PHY_GTLVL_RESP_WAIT_CNT_2	20:16	0x00	0x0-0x1f	Number of cycles + 4 to wait between dfi_rddata_en and the sampling of the DQS during gate
PHY_GTLVL_DLY_STEP_2	11:8	0x0	0x0-0xf	DQS slave delay step size during
PHY_WRLVL_RESP_WAIT_CNT_2	4:0	0x00	0x0-0x1f	Number of cycles to wait between dfi_wrlvl_strobe and the sampling

DENALI_PHY_345 (Address PHY_BASE_ADDR + 345)

31 26	25 - - - - 16	15 10	9 - - - - 0
RESV	PHY_GTLVL_F - -	RESV	PHY_GTLVL_B - -

Name	Bits	Default	Range	Description
PHY_GTLVL_FINAL_STEP_2	25:16	0x000	0x0-0x3ff	Final backup step delay used in
PHY_GTLVL_BACK_STEP_2	9:0	0x000	0x0-0x3ff	Interim backup step delay used in

DENALI_PHY_346 (Address PHY_BASE_ADDR + 346)

31 - - - - - - 16	15 12	11 8	7 - - 0
OBSOLETE - - -	RESV	PHY_RDLVL_	PHY_WDQLVL -

Name	Bits	Default	Range	Description
PHY_RDLVL_DLY_STEP_2	11:8	0x0	0x0-0xf	DQS slave delay step size during
PHY_WDQLVL_DLY_STEP_2	7:0	0x00	0x0-0xff	DQ slave delay step size during

DENALI_PHY_384 (Address PHY_BASE_ADDR + 384)

31 - - - - - - - - - - - - - - - - 0
PHY_DQ_DM_ - - - - - - -

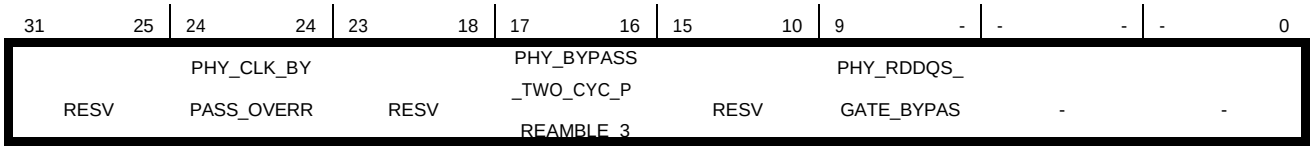
Name	Bits	Default	Range	Description
PHY_DQ_DM_SWIZZLE0_3	31:0	0x00000000	0x0-0xffffffff	DQ/DM bit swizzling 0 for slice 3. Bits (3:0) inform the PHY which bit in {DM,DQ} map to DQ0, Bits (7:4) {DM,DQ} map to DQ1, etc.

DENALI_PHY_385 (Address PHY_BASE_ADDR + 385)

31 - - 24	23 19	18 - - - - 8	7 4	3 0
		PHY_CLK_WR		PHY_DQ_DM_
OBSOLETE -	RESV	BYPASS_SLA - -	RESV	SWIZZLE1_3

Name	Bits	Default	Range	Description
PHY_CLK_WR_BYPASS_SLAVE_DELAY_3	18:8	0x000	0x0-0x7ff	Write data clock bypass mode
PHY_DQ_DM_SWIZZLE1_3	3:0	0x0	0x0-0xf	DQ/DM bit swizzling 1 for slice 3. Bits (3:0) inform the PHY which bit

DENALI_PHY_386 (Address PHY_BASE_ADDR + 386)

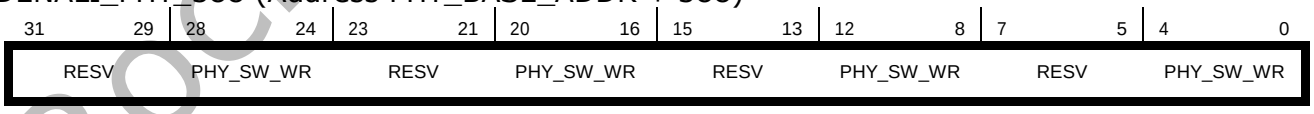


Name	Bits	Default	Range	Description
PHY_CLK_BYPASS_OVERRIDE_3	24	0x0	0x0-0x1	Bypass mode override setting for
PHY_BYPASS_TWO_CYC_PREAMBLE_3	17:16	0x0	0x0-0x3	PHY two_cycle_preamble for
PHY_RDDQS_GATE_BYPASS_SLAVE_DE	9:0	0x000	0x0-0x3ff	Read DQS bypass mode slave

DENALI_PHY_387 (Address PHY_BASE_ADDR + 387)

Name	Bits	Default	Range	Description
PHY_SW_WRDQ3_SHIFT_3	28:24	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for write DQ3 for slice 3. Bit (0) enables override of half_cycle_shift. Bit (1)
PHY_SW_WRDQ2_SHIFT_3	20:16	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for write DQ2 for slice 3. Bit (0) enables override of half_cycle_shift. Bit (1)
PHY_SW_WRDQ1_SHIFT_3	12:8	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for write DQ1 for slice 3. Bit (0) enables override of half_cycle_shift. Bit (1)
PHY_SW_WRDQ0_SHIFT_3	4:0	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for write DQ0 for slice 3. Bit (0) enables override of half_cycle_shift. Bit (1)

DENALI_PHY_388 (Address PHY_BASE_ADDR + 388)



Name	Bits	Default	Range	Description
PHY_SW_WRDQ7_SHIFT_3	28:24	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for write DQ7 for slice 3. Bit (0) enables override of half_cycle_shift. Bit (1)
PHY_SW_WRDQ6_SHIFT_3	20:16	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for write DQ6 for slice 3. Bit (0) enables override of half_cycle_shift. Bit (1)

PHY_SW_WRDQ5_SHIFT_3	12:8	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for write DQ5 for slice 3. Bit (0) enables override of half_cycle_shift. Bit (1)
PHY_SW_WRDQ4_SHIFT_3	4:0	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for write DQ4 for slice 3. Bit (0) enables override of half_cycle_shift. Bit (1)

DENALI_PHY_389 (Address PHY_BASE_ADDR + 389)

31 -	- 24	23 19	18 16	15 12	11 8	7 5	4 0
OBSOLETE -		RESV	PHY_DQ_TSE	RESV	PHY_SW_WR	RESV	PHY_SW_WR

Name	Bits	Default	Range	Description
PHY_DQ_TSEL_ENABLE_3	18:16	0x0	0x0-0x7	Operation type tsel enables for DQ/DM signals for slice 3. Bit (0) enables tsel_en during read cycles. Bit (1) enables tsel_en during write
PHY_SW_WRDQS_SHIFT_3	11:8	0x0	0x0-0xf	Manual override of automatic half_cycle_shift/cycle_shift for write DQS for slice 3. Bit (0) enables override of half_cycle_shift. Bit (1)
PHY_SW_WRDM_SHIFT_3	4:0	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for write DM for slice 3. Bit (0) enables override of half_cycle_shift. Bit (1)

DENALI_PHY_390 (Address PHY_BASE_ADDR + 390)

31 27	26 24	23 -	- -	- -	- -	- -	- 0
RESV	PHY_DQS_TS	PHY_DQ_TSE	-	-	-	-	-

Name	Bits	Default	Range	Description
PHY_DQS_TSEL_ENABLE_3	26:24	0x0	0x0-0x7	Operation type tsel enables for DQS signals for slice 3. Bit (0) enables tsel_en during read cycles. Bit (1) enables tsel_en during write
PHY_DQ_TSEL_SELECT_3	23:0	0x000000	0x0-0xffffff	Operation type tsel select values for DQ/DM signals for slice 3. Bits (3:0) are tsel_sel values during read cycles. Bits (7:4) are tsel_sel

DENALI_PHY_391 (Address PHY_BASE_ADDR + 391)

31 26	25 24	23 -	- -	- -	- -	- -	- 0
RESV	PHY_TWO_CYC_PREAMBLE	PHY_DQS_TSEL_SELECT_3	-	-	-	-	-

Name	Bits	Default	Range	Description

PHY_TWO_CYC_PREAMBLE_3	25:24	0x0	0x0-0x3	2 cycle preamble support for slice 3. Bit (0) controls the 2 cycle read preamble. Bit (1) controls the 2
PHY_DQS_TSEL_SELECT_3	23:0	0x000000	0x0-0xffffff	Operation type tsel select values for DQS signals for slice 3. Bits (3:0) are tsel_sel values during read cycles. Bits (7:4) are tsel_sel

DENALI_PHY_392 (Address PHY_BASE_ADDR + 392)

31 25	24 24	23 17	16 16	15 10	9 8	7 1	0 0
RESV	PHY_PER_CS_TRAINING_INDEX_3	RESV	PHY_PER_CS_TRAINING_M	RESV	PHY_PER_RANK_CS_MAP_	RESV	PHY_DBI_MO

Name	Bits	Default	Range	Description
PHY_PER_CS_TRAINING_INDEX_3	24	0x0	0x0-0x1	For per-rank training, indicates which ranksparamtersareread/
PHY_PER_CS_TRAINING_MULTICAST_EN_3	16	0x1	0x0-0x1	When set, a register write will update parameters for all ranks at
PHY_PER_RANK_CS_MAP_3	9:8	0x0	0x0-0x3	Per-rank CS map for slice 3.
PHY_DBI_MODE_3	0	0x0	0x0-0x1	DBI mode for slice 3. Bit (0) enables return of DBI read data. Bit

DENALI_PHY_393 (Address PHY_BASE_ADDR + 393)

31 28	27 24	23 20	19 16	15 12	11 8	7 2	1 0
RESV	PHY_LP4_BOOT_RPTR_UP	RESV	PHY_LP4_BOOT_RDDATA_	RESV	PHY_LP4_BOOT_RDDATA_	RESV	PHY_LP4_BOOT_RDDATA_

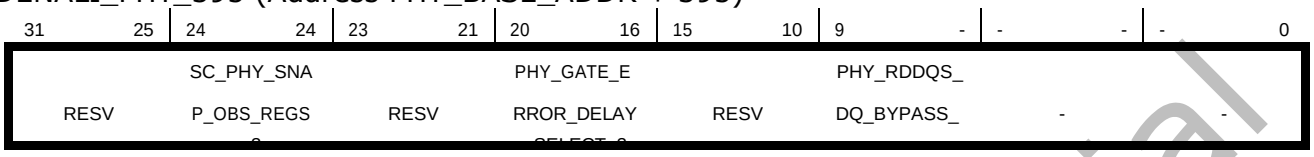
Name	Bits	Default	Range	Description
PHY_LP4_BOOT_RPTR_UPDATE_3	27:24	0x0	0x0-0xf	For LPDDR4 boot frequency, the offset in cycles from the
PHY_LP4_BOOT_RDDATA_EN_TSEL_DLY_3	19:16	0x0	0x0-0xf	For LPDDR4 boot frequency, the number of cycles that the dfi_rddata_en signal is earlier than
PHY_LP4_BOOT_RDDATA_EN_DLY_3	11:8	0x0	0x0-0xf	For LPDDR4 boot frequency, the number of cycles that the
PHY_LP4_BOOT_RDDATA_EN_IE_DLY_3	1:0	0x0	0x0-0x3	For LPDDR4 boot frequency, the number of cycles that the dfi_rddata_en signal is earlier than

DENALI_PHY_394 (Address PHY_BASE_ADDR + 394)

31 -	- 24	23 17	16 16	15 15	14 8	7 4	3 0
OBSOLETE	-	RESV	PHY_SLICE_PWR_RDC_DIS	RESV	PHY_LPBK_C	RESV	PHY_LP4_BOOT_RDDQS_L

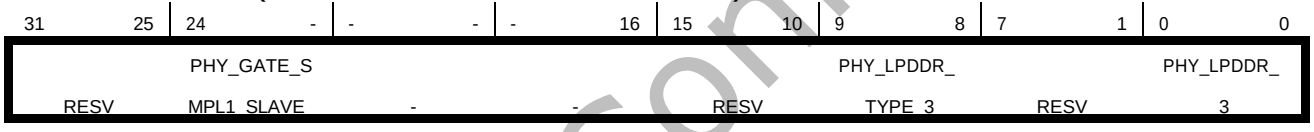
Name	Bits	Default	Range	Description
PHY_SLICE_PWR_RDC_DISABLE_3	16	0x0	0x0-0x1	data slice power reduction disable
PHY_LPBK_CONTROL_3	14:8	0x00	0x0-0x7f	Loopback control bits for slice 3.
PHY_LP4_BOOT_RDDQS_LATENCY_ADJ	3:0	0x0	0x0-0xf	For LPDDR4 boot frequency, the number of cycles to delay the

DENALI_PHY_395 (Address PHY_BASE_ADDR + 395)



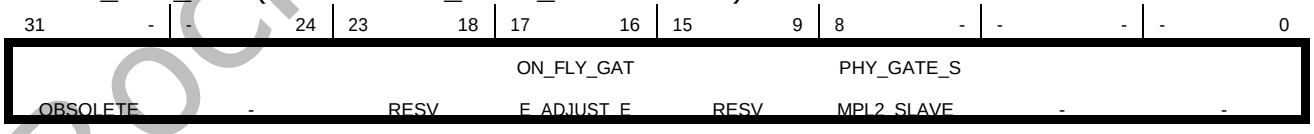
Name	Bits	Default	Range	Description
SC_PHY_SNAP_OBS_REGS_3	24	0x0	0x0-0x1	Initiates a snapshot of the internal observation registers for slice 3.
PHY_GATE_ERROR_DELAY_SELECT_3	20:16	0x00	0x0-0x1f	Number of cycles to wait for the DQS gate to close before flagging
PHY_RDDQS_DQ_BYPASS_SLAVE_DELAY_3	9:0	0x000	0x0-0x3ff	Read DQS data clock bypass mode

DENALI_PHY_396 (Address PHY_BASE_ADDR + 396)



Name	Bits	Default	Range	Description
PHY_GATE_SMPL1_SLAVE_DELAY_3	24:16	0x000	0x0-0x1ff	Number of cycles to delay the read DQS gate signal to generate gate1
PHY_LPDDR_TYPE_3	9:8	0x0	0x0-0x3	Indicates the type of DRAM for slice 3. Clear to 0 for DDR3 or
PHY_LPDDR_3	0	0x0	0x0-0x1	Indicates a cycle of delay for the

DENALI_PHY_397 (Address PHY_BASE_ADDR + 397)

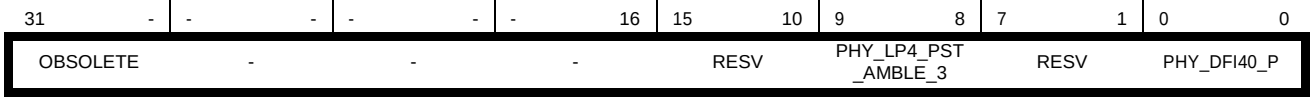


Name	Bits	Default	Range	Description
ON_FLY_GATE_ADJUST_EN_3	17:16	0x0	0x0-0x3	Control the on the fly gate
PHY_GATE_SMPL2_SLAVE_DELAY_3	8:0	0x000	0x0-0x1ff	Number of cycles to delay the read DQS gate signal to generate gate2

DENALI_PHY_398 (Address PHY_BASE_ADDR + 398)

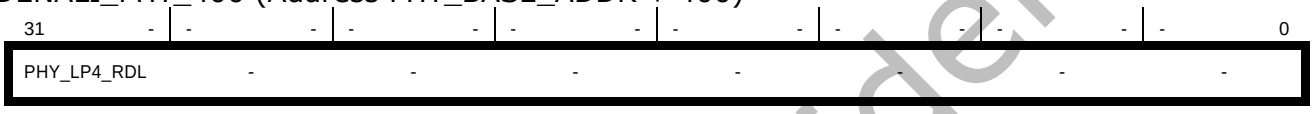
Name	Bits	Default	Range	Description
PHY_GATE_TRACKING_OBS_3	31:0	0x00000000	0x0-0xffffffff	Report the on the fly gate

DENALI_PHY_399 (Address PHY_BASE_ADDR + 399)



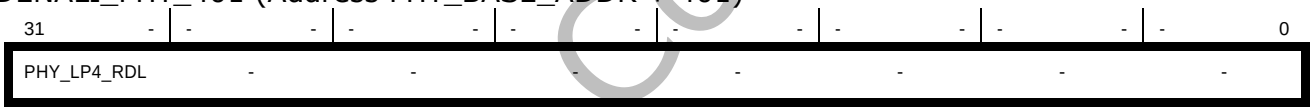
Name	Bits	Default	Range	Description
PHY_LP4_PST_AMBLE_3	9:8	0x0	0x0-0x3	Controls the read postamble
PHY_DFI40_POLARITY_3	0	0x0	0x0-0x1	Indicates the dfi_wrdata_cs_n and dfi_rddata_cs_n is low active or

DENALI_PHY_400 (Address PHY_BASE_ADDR + 400)



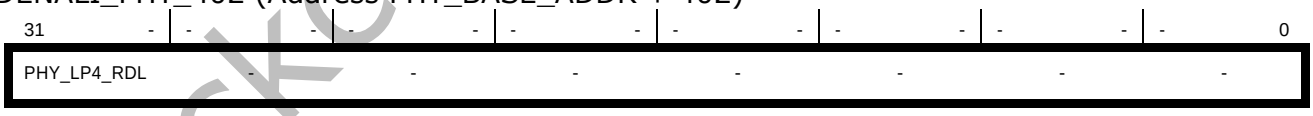
Name	Bits	Default	Range	Description
PHY_LP4_RDLVL_PATT8_3	31:0	0x00000000	0x0-0xffffffff	LPDDR4 read leveling pattern 8

DENALI_PHY_401 (Address PHY_BASE_ADDR + 401)



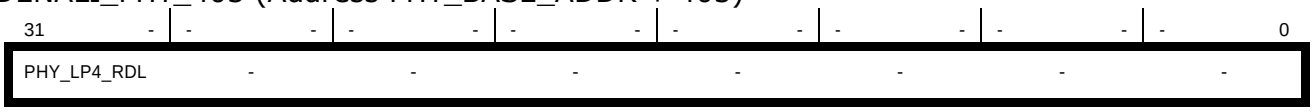
Name	Bits	Default	Range	Description
PHY_LP4_RDLVL_PATT9_3	31:0	0x000000	0x0-0xffffffff	LPDDR4 read leveling pattern 9

DENALI_PHY_402 (Address PHY_BASE_ADDR + 402)



Name	Bits	Default	Range	Description
PHY_LP4_RDLVL_PATT10_3	31:0	0x000000	0x0-0xffffffff	LPDDR4 read leveling pattern 10

DENALI_PHY_403 (Address PHY_BASE_ADDR + 403)



Name	Bits	Default	Range	Description
PHY_LP4_RDLVL_PATT11_3	31:0	0x00000000	0x0-0xffffffff	LPDDR4 read leveling pattern 11

DENALI_PHY_404 (Address PHY_BASE_ADDR + 404)

31 27	26 24	23 19	18 16	15 9	8 8	7 3	2 0
RESV	PHY_RDDQ_ENC_OBS_SEL	RESV	PHY_MASTER_DLY_LOCK_OBS_SELECT	RESV	PHY_SW_FIFO_PTR_RST_	RESV	PHY_SLAVE_LOOP_CNT_UP

Name	Bits	Default	Range	Description
PHY_RDDQ_ENC_OBS_SELECT_3	26:24	0x0	0x0-0x7	Select value to map the internal read DQ slave delay encoded settings to the accessible read DQ
PHY_MASTER_DLY_LOCK_OBS_SELECT_3	18:16	0x0	0x0-0x7	Select value to map the internal master delay observation registers
PHY_SW_FIFO_PTR_RST_DISABLE_3	8	0x0	0x0-0x1	Disables automatic reset of the read entry FIFO pointers for slice 3.
PHY_SLAVE_LOOP_CNT_UPDATE_3	2:0	0x0	0x0-0x7	Sets the frequency by which the slave delay encoded value holding

DENALI_PHY_405 (Address PHY_BASE_ADDR + 405)

31 28	27 24	23 20	19 16	15 12	11 8	7 4	3 0
RESV	PHY_FIFO_PTR_OBS_SELE	RESV	PHY_WR_SHIFT_OBS_SEL	RESV	PHY_WR_ENC_OBS_SELECT_3	RESV	PHY_RDDQS_DQ_ENC_OBS

Name	Bits	Default	Range	Description
PHY_FIFO_PTR_OBS_SELECT_3	27:24	0x0	0x0-0xf	Select value to map the internal read entry FIFO read/write pointers to the accessible read entry FIFO
PHY_WR_SHIFT_OBS_SELECT_3	19:16	0x0	0x0-0xf	Select value to map the internal write DQ/DQS automatic cycle/ half_cycle shift settings to the
PHY_WR_ENC_OBS_SELECT_3	11:8	0x0	0x0-0xf	Select value to map the internal write DQ slave delay encoded settings to the accessible write DQ
PHY_RDDQS_DQ_ENC_OBS_SELECT_3	3:0	0x0	0x0-0xf	Select value to map the internal read DQS DQ rise/fall slave delay encoded settings to the accessible

DENALI_PHY_406 (Address PHY_BASE_ADDR + 406)

31 28	27 24	23 22	21 16	15 9	8 8	7 1	0 0
RESV	PHY_WRLVL_UPDT_WAIT	RESV	PHY_WRLVL_CAPTURE_CN	RESV	SC_PHY_LVL_DEBUG_CONT	RESV	PHY_LVL_DEBUG_MODE_3

Name	Bits	Default	Range	Description
PHY_WRLVL_UPDT_WAIT_CNT_3	27:24	0x0	0x0-0xf	Number of cycles to wait after changing DQS slave delay setting
PHY_WRLVL_CAPTURE_CNT_3	21:16	0x00	0x0-0x3f	Number of samples to take at each DQS slave delay setting during
SC_PHY_LVL_DEBUG_CONT_3	8	0x0	0x0-0x1	Allows the leveling state machine to advance (when in debug mode)

PHY_LVL_DEBUG_MODE_3	0	0x0	0x0-0x1	Enables leveling debug mode for

DENALI_PHY_407 (Address PHY_BASE_ADDR + 407)

31 28	27 24	23 22	21 16	15 12	11 8	7 6	5 0
RESV	PHY_RDLVL_UPDT_WAIT	RESV	PHY_RDLVL_CAPTURE_CN	RESV	PHY_GTLVL_UPDT_WAIT_C	RESV	PHY_GTLVL_CAPTURE_CNT

Name	Bits	Default	Range	Description
PHY_RDLVL_UPDT_WAIT_CNT_3	27:24	0x0	0x0-0xf	Number of cycles to wait after changing DQS slave delay setting
PHY_RDLVL_CAPTURE_CNT_3	21:16	0x00	0x0-0x3f	Number of samples to take at each DQS slave delay setting during
PHY_GTLVL_UPDT_WAIT_CNT_3	11:8	0x0	0x0-0xf	Number of cycles + 4 to wait after changing DQS slave delay setting
PHY_GTLVL_CAPTURE_CNT_3	5:0	0x00	0x0-0x3f	Number of samples to take at each DQS slave delay setting during

DENALI_PHY_408 (Address PHY_BASE_ADDR + 408)

31 30	29 24	23 -	- 16	15 13	12 8	7 2	1 0
RESV	PHY_WDQLVL_BURST_CNT_3	PHY_RDLVL_DATA_MASK_	-	RESV	PHY_RDLVL_RDDQS_DQ_	RESV	PHY_RDLVL_

Name	Bits	Default	Range	Description
PHY_WDQLVL_BURST_CNT_3	29:24	0x00	0x0-0x3f	Defines the write/read burst length in bytes during the write data
PHY_RDLVL_DATA_MASK_3	23:16	0x00	0x0-0xff	Per-bit mask for read leveling for slice 3. If all bits are not used, only
PHY_RDLVL_RDDQS_DQ_OBS_SELECT_3	12:8	0x00	0x0-0x1f	Select value to map an individual DQ data window leading/trailing edge to the leading/trailing edge
PHY_RDLVL_OP_MODE_3	1:0	0x0	0x0-0x3	Read leveling algorithm select for slice 3. Clear to 0 to move linearly from left to right. Set to 1 to start

DENALI_PHY_409 (Address PHY_BASE_ADDR + 409)

31 28	27 24	23 19	18 -	- -	- 8	7 3	2 0
RESV	PHY_WDQLVL_UPDT_WAIT_	RESV	PHY_WDQLVL_DQDM_SLV_DLY_JUMP_O	-	-	RESV	PHY_WDQLVL_PATT_3

Name	Bits	Default	Range	Description
PHY_WDQLVL_UPDT_WAIT_CNT_3	27:24	0x0	0x0-0xf	Number of cycles to wait after changing the DQ slave delay
PHY_WDQLVL_DQDM_SLV_DLY_JUMP_OFFSET_3	18:8	0x000	0x0-0x7ff	Defines the write/read burst length in bytes during the write data

PHY_WDQLVL_PATT_3	2:0	0x0	0x0-0x7	Defines the training patterns to be used during the write data leveling sequence for slice 3. Bit (0) corresponds to the LFSR data training pattern. Bit (1) corresponds to the CLK data training pattern. Bit (2) corresponds to user-defined

DENALI_PHY_410 (Address PHY_BASE_ADDR + 410)

31 - 24	23 - 17	16 - 16	15 - 12	11 - 8	7 - 4	3 - 0
OBSOLETE	RESV	SC_PHY_WDQLVL_CLR_P	RESV	PHY_WDQLVL_QTR_DLY_ST	RESV	PHY_WDQLVL_DQDM_OBS_

Name	Bits	Default	Range	Description
SC_PHY_WDQLVL_CLR_PREV_RESULTS_3	16	0x0	0x0-0x1	Clears the previous result value to allow a clean slate comparison for future write DQ leveling results for
PHY_WDQLVL_QTR_DLY_STEP_3	11:8	0x0	0x0-0xf	Defines the step granularity for the logic to use once an edge is found. When this occurs, the logic jumps back to the previous invalid value
PHY_WDQLVL_DQDM_OBS_SELECT_3	3:0	0x0	0x0-0xf	Select value to map an individual DQ data window leading/trailing edge to the leading/trailing edge

DENALI_PHY_411 (Address PHY_BASE_ADDR + 411)

31 - 16	15 - 9	8 - 8	7 - 0
OBSOLETE	RESV	PHY_WDQLVL_DATADM_MA	-

Name	Bits	Default	Range	Description
PHY_WDQLVL_DATADM_MASK_3	8:0	0x000	0x0-0x1ff	Per-bit mask for write data leveling for slice 3. Set to 1 to mask any bit

DENALI_PHY_412 (Address PHY_BASE_ADDR + 412)

31 - 0
PHY_USER_P -

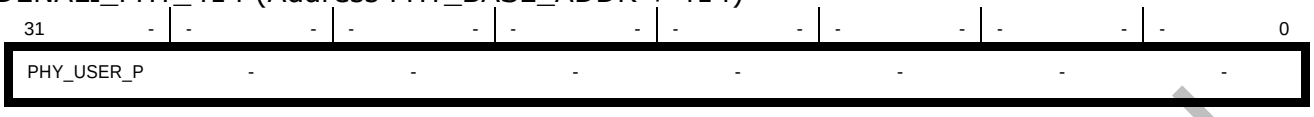
Name	Bits	Default	Range	Description
PHY_USER_PATT0_3	31:0	0x00000000	0x0-0xffffffff	User-defined pattern to be used during write data leveling for slice 3. This register holds the bytes 3 to 0 written/read from device.

DENALI_PHY_413 (Address PHY_BASE_ADDR + 413)

31 - 0
PHY_USER_P -

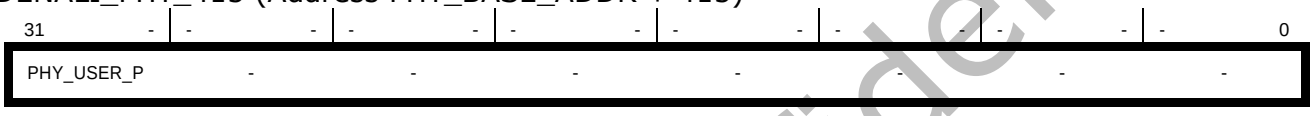
Name	Bits	Default	Range	Description
PHY_USER_PATT1_3	31:0	0x00000000	0x0-0xffffffff	User-defined pattern to be used during write data leveling for slice 3. This register holds the bytes 7 to 4 written/read from device.

DENALI_PHY_414 (Address PHY_BASE_ADDR + 414)



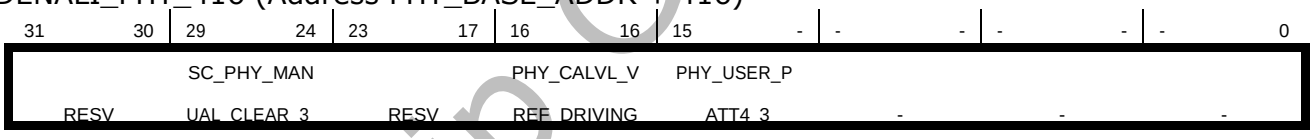
Name	Bits	Default	Range	Description
PHY_USER_PATT2_3	31:0	0x00000000	0x0-0xffffffff	User-defined pattern to be used during write data leveling for slice 3. This register holds the bytes 11 to 8 written/read from device.

DENALI_PHY_415 (Address PHY_BASE_ADDR + 415)



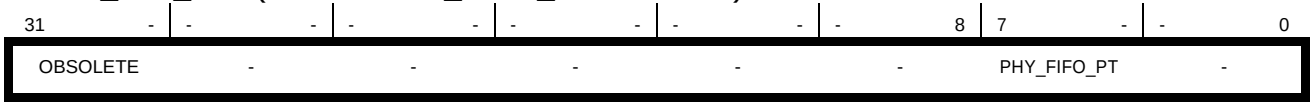
Name	Bits	Default	Range	Description
PHY_USER_PATT3_3	31:0	0x00000000	0x0-0xffffffff	User-defined pattern to be used during write data leveling for slice 3. This register holds the bytes 15 to 12 written/read from device.

DENALI_PHY_416 (Address PHY_BASE_ADDR + 416)



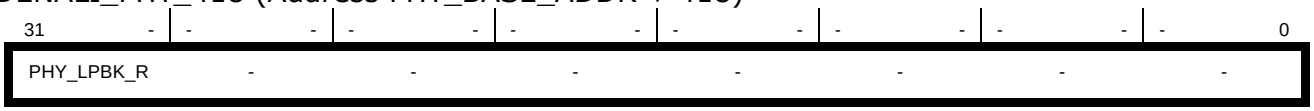
Name	Bits	Default	Range	Description
SC_PHY_MANUAL_CLEAR_3	29:24	0x00	0x0-0x3f	Manual reset/clear of internal logic for slice 3. Bit (0) initiates manual setup of the read DQS gate. Bit (1) is reset of read entry FIFO pointers. Bit (2) is reset of master delay min/ max lock values. Bit (3) is manual reset of master delay unlock
PHY_CALVL_VREF_DRIVING_SLICE_3	16	0x0	0x0-0x1	Indicates if slice 3 is used to drive the VREF value to the device
PHY_USER_PATT4_3	15:0	0x0000	0x0-0xffff	User-defined pattern to be used during write data leveling for slice 3. This register holds the DM bit for

DENALI_PHY_417 (Address PHY_BASE_ADDR + 417)



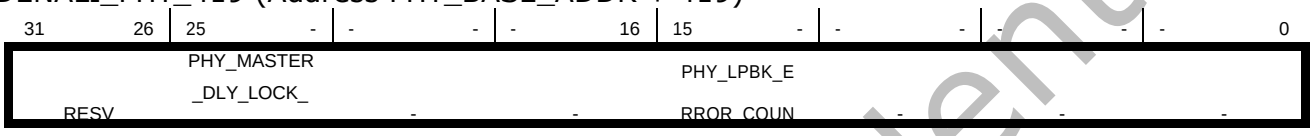
Name	Bits	Default	Range	Description
PHY_FIFO_PTR_OBS_3	7:0	0x00	0x0-0xff	Observation register for read entry FIFO pointers for slice 3. READ-

DENALI_PHY_418 (Address PHY_BASE_ADDR + 418)



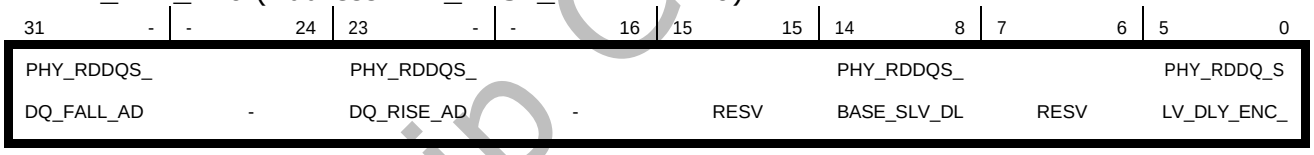
Name	Bits	Default	Range	Description
PHY_LPBK_RESULT_OBS_3	31:0	0x00000000	0x0-0xffffffff	Observation register containing loopback status/results for slice 3.

DENALI_PHY_419 (Address PHY_BASE_ADDR + 419)



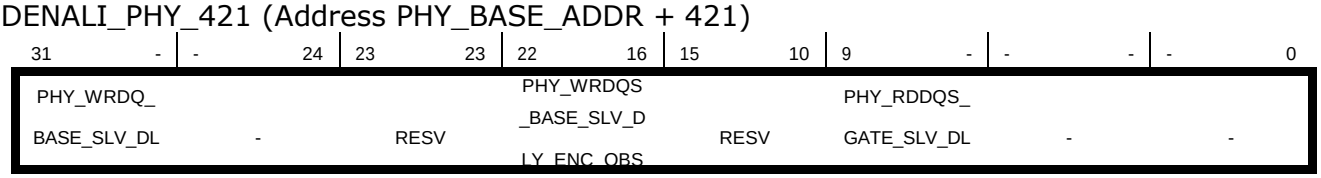
Name	Bits	Default	Range	Description
PHY_MASTER_DLY_LOCK_OBS_3	25:16	0x000	0x0-0x3ff	Observation register for master delay results for slice 3. READ-
PHY_LPBK_ERROR_COUNT_OBS_3	15:0	0x0000	0x0-0xffff	Observation register containing total number of loopback error data

DENALI_PHY_420 (Address PHY_BASE_ADDR + 420)



Name	Bits	Default	Range	Description
PHY_RDDQS_DQ_FALL_ADDER_SLV_DL	31:24	0x00	0x0-0xff	Observation register for read DQS DQ falling edge adder slave delay
PHY_RDDQS_DQ_RISE_ADDER_SLV_DL	23:16	0x00	0x0-0xff	Observation register for read DQS DQ rising edge adder slave delay
PHY_RDDQS_BASE_SLV_DLY_ENC_OBS_3	14:8	0x00	0x0-0x7f	Observation register for read DQS base slave delay encoded value for
PHY_RDDQ_SLV_DLY_ENC_OBS_3	5:0	0x00	0x0-0x3f	Observation register for read DQ slave delay encoded values for

DENALI_PHY_421 (Address PHY_BASE_ADDR + 421)



Name	Bits	Default	Range	Description

PHY_WRDQ_BASE_SLV_DLY_ENC_OBS_3	31:24	0x00	0x0-0xff	Observation register for write DQ base slave delay encoded value for
PHY_WRDQS_BASE_SLV_DLY_ENC_OBS_3	22:16	0x00	0x0-0x7f	Observation register for write DQS base slave delay encoded value for
PHY_RDDQS_GATE_SLV_DLY_ENC_OBS_3	9:0	0x000	0x0-0x3ff	Observation register for read DQS gate slave delay encoded value for

DENALI_PHY_422 (Address PHY_BASE_ADDR + 422)

31 26	25 - - - - 16	15 11	10 8	7 - - 0
RESV	PHY_WRLVL_HARD0_DELA	RESV	PHY_WR_SHIFT_OBS_3	PHY_WR_ADDER_SLV_DLY

Name	Bits	Default	Range	Description
PHY_WRLVL_HARD0_DELAY_OBS_3	25:16	0x000	0x0-0x3ff	Observation register for write leveling last hard 0 DQS slave
PHY_WR_SHIFT_OBS_3	10:8	0x0	0x0-0x7	Observation register for automatic half cycle and cycle shift values for
PHY_WR_ADDER_SLV_DLY_ENC_OBS_3	7:0	0x00	0x0-0xff	Observation register for write adder slave delay encoded value for slice

DENALI_PHY_423 (Address PHY_BASE_ADDR + 423)

31 - - - - - 16	15 10	9 - - - - 0
OBSOLETE	RESV	PHY_WRLVL_HARD1_DELA

Name	Bits	Default	Range	Description
PHY_WRLVL_HARD1_DELAY_OBS_3	9:0	0x000	0x0-0x3ff	Observation register for write leveling first hard 1 DQS slave

DENALI_PHY_424 (Address PHY_BASE_ADDR + 424)

31 - - 24	23 17	16 - - - - - - - 0
OBSOLETE	RESV	PHY_WRLVL_STATUS_OBS

Name	Bits	Default	Range	Description
PHY_WRLVL_STATUS_OBS_3	16:0	0x00000	0x0-0x1ffff	Observation register for write leveling status for slice 3. READ-

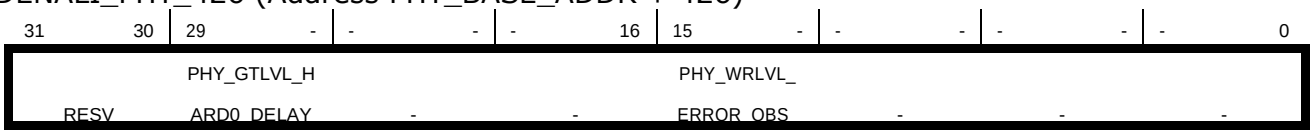
DENALI_PHY_425 (Address PHY_BASE_ADDR + 425)

31 25	24 - - - - 16	15 9	8 - - - - 0
RESV	PHY_GATE_SMPL2_SLV_DL	RESV	PHY_GATE_SMPL1_SLV_DL

Name	Bits	Default	Range	Description
PHY_GATE_SMPL2_SLV_DLY_ENC_OBS_3	24:16	0x000	0x0-0x1ff	Observation register for gate sample1 slave delay encoded

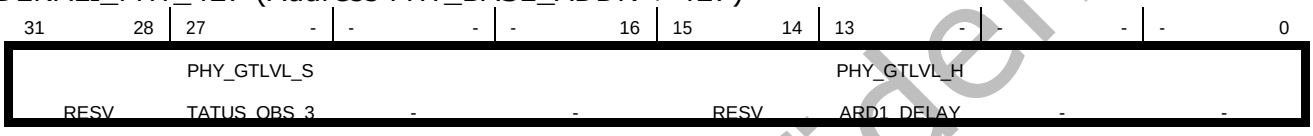
PHY_GATE_SMPL1_SLV_DLY_ENC_OBS_3	8:0	0x000	0x0-0x1ff	Observation register for gate sample1 slave delay encoded

DENALI_PHY_426 (Address PHY_BASE_ADDR + 426)



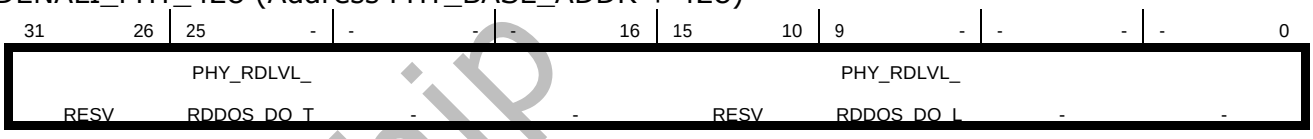
Name	Bits	Default	Range	Description
PHY_GTLVL_HARD0_DELAY_OBS_3	29:16	0x0000	0x0-0x3fff	Observation register for gate training first hard 0 DQS slave
PHY_WRLVL_ERROR_OBS_3	15:0	0x0000	0x0-0xffff	Observation register for write leveling error status for slice 3.

DENALI_PHY_427 (Address PHY_BASE_ADDR + 427)



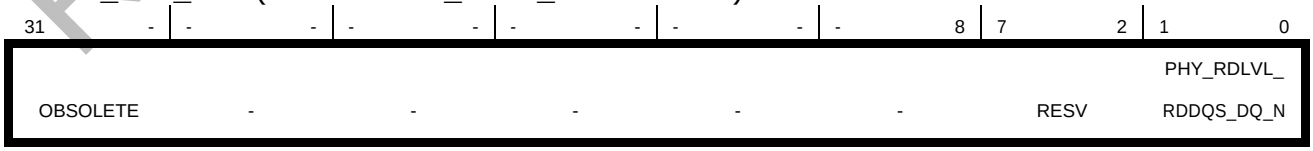
Name	Bits	Default	Range	Description
PHY_GTLVL_STATUS_OBS_3	27:16	0x000	0x0-0xfff	Observation register for gate training status for slice 3. READ-
PHY_GTLVL_HARD1_DELAY_OBS_3	13:0	0x0000	0x0-0x3fff	Observation register for gate training last hard 1 DQS slave

DENALI_PHY_428 (Address PHY_BASE_ADDR + 428)



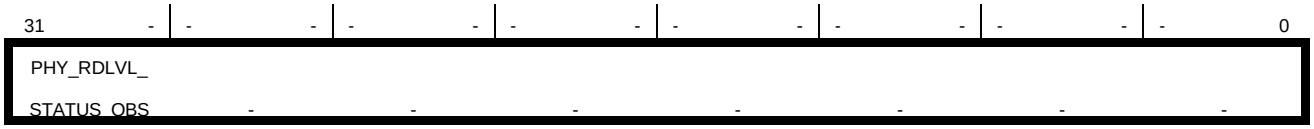
Name	Bits	Default	Range	Description
PHY_RDLVL_RDDQS_DQ_TE_DLY_OBS_	25:16	0x000	0x0-0x3ff	Observation register for read leveling data window trailing edge
PHY_RDLVL_RDDQS_DQ_LE_DLY_OBS_3	9:0	0x000	0x0-0x3ff	Observation register for read leveling data window leading edge

DENALI_PHY_429 (Address PHY_BASE_ADDR + 429)



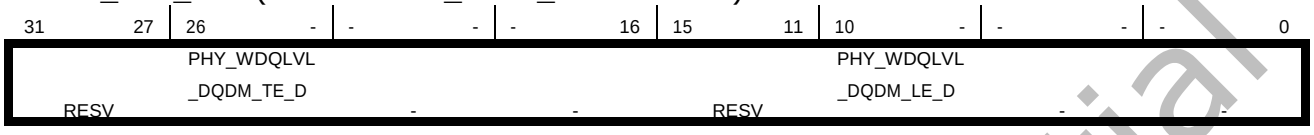
Name	Bits	Default	Range	Description
PHY_RDLVL_RDDQS_DQ_NUM_WINDOWS_OBS_3	1:0	0x0	0x0-0x3	Observation register for read leveling number of windows found

DENALI_PHY_430 (Address PHY_BASE_ADDR + 430)



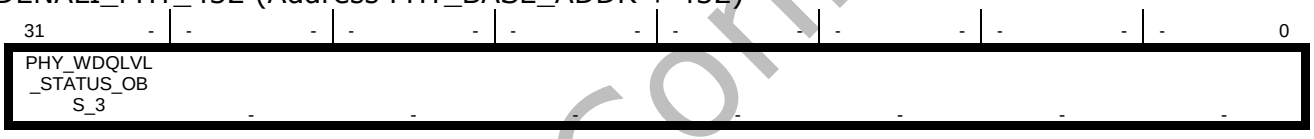
Name	Bits	Default	Range	Description
PHY_RDLVL_STATUS_OBS_3	31:0	0x00000000	0x0-0xffffffff	Observation register for read leveling status for slice 3. READ-

DENALI_PHY_431 (Address PHY_BASE_ADDR + 431)



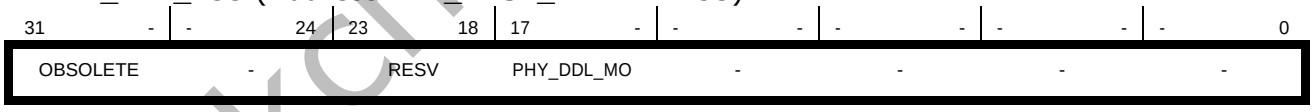
Name	Bits	Default	Range	Description
PHY_WDQLVL_DQDM_TE_DLY_OBS_3	26:16	0x000	0x0-0x7ff	Observation register for write data leveling data window trailing edge
PHY_WDQLVL_DQDM_LE_DLY_OBS_3	10:0	0x000	0x0-0x7ff	Observation register for write data leveling data window leading edge

DENALI_PHY_432 (Address PHY_BASE_ADDR + 432)



Name	Bits	Default	Range	Description
PHY_WDQLVL_STATUS_OBS_3	31:0	0x00000000	0x0-0xffffffff	Observation register for write data leveling status for slice 3. READ-

DENALI_PHY_433 (Address PHY_BASE_ADDR + 433)

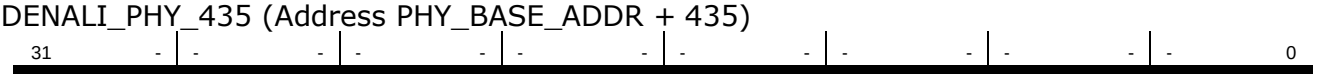


Name	Bits	Default	Range	Description
PHY_DDL_MODE_3	17:0	0x00000	0x0-0x3ffff	DDL mode for slice 3.

DENALI_PHY_434 (Address PHY_BASE_ADDR + 434)

Name	Bits	Default	Range	Description
PHY_DDL_TEST_OBS_3	31:0	0x00000000	0x0-0xffffffff	DDL test observation for slice 3.

DENALI_PHY_435 (Address PHY_BASE_ADDR + 435)



PHY_DDL_TE ST_MSTR_DL	-	-	-	-	-	-	-

Name	Bits	Default	Range	Description
PHY_DDL_TEST_MSTR_DLY_OBS_3	31:0	0x000000	0x0-0xffffffff	DDL test observation delays for

DENALI_PHY_436 (Address PHY_BASE_ADDR + 436)

31	-	- 24	23	-	- 16	15	9	8	8	7	1	0	0
OBSOLETE	-		PHY_RX_CAL _SAMPLE_WA	-		RESV		PHY_RX_CAL OVERRIDE_3		RESV		SC_PHY_RX_ CAL_START_3	

Name	Bits	Default	Range	Description
PHY_RX_CAL_SAMPLE_WAIT_3	23:16	0x00	0x0-0xff	RX Calibration state machine wait
PHY_RX_CAL_OVERRIDE_3	8	0x0	0x0-0x1	Manual setting of RX Calibration
SC_PHY_RX_CAL_START_3	0	0x0	0x0-0x1	Manual RX Calibration start for

DENALI_PHY_437 (Address PHY_BASE_ADDR + 437)

31	28	27	-	-	-	- 16	15	12	11	-	-	-	0
RESV		PHY_RX_CAL _DQ1_3		-	-		RESV		PHY_RX_CAL _DQ0_3		-	-	

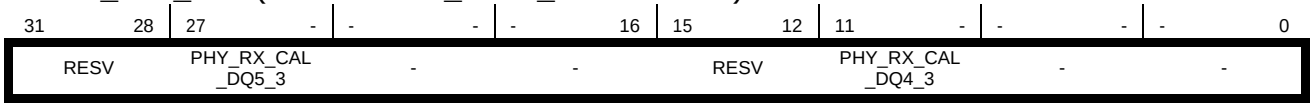
Name	Bits	Default	Range	Description
PHY_RX_CAL_DQ1_3	27:16	0x000	0x0-0xfff	RX Calibration codes for DQ1 for slice 3. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits
PHY_RX_CAL_DQ0_3	11:0	0x000	0x0-0xfff	RX Calibration codes for DQ0 for slice 3. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits

DENALI_PHY_438 (Address PHY_BASE_ADDR + 438)

31	28	27	-	-	-	- 16	15	12	11	-	-	-	0
RESV		PHY_RX_CAL _DQ3_3		-	-		RESV		PHY_RX_CAL _DQ2_3		-	-	

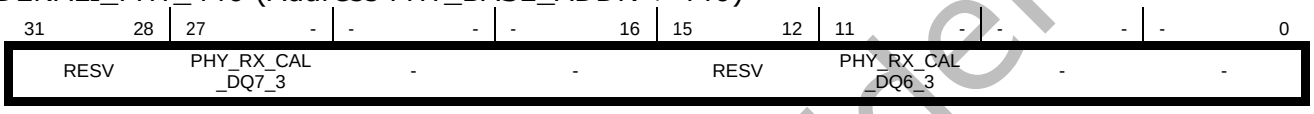
Name	Bits	Default	Range	Description
PHY_RX_CAL_DQ3_3	27:16	0x000	0x0-0xfff	RX Calibration codes for DQ3 for slice 3. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits
PHY_RX_CAL_DQ2_3	11:0	0x000	0x0-0xfff	RX Calibration codes for DQ2 for slice 3. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits

DENALI_PHY_439 (Address PHY_BASE_ADDR + 439)



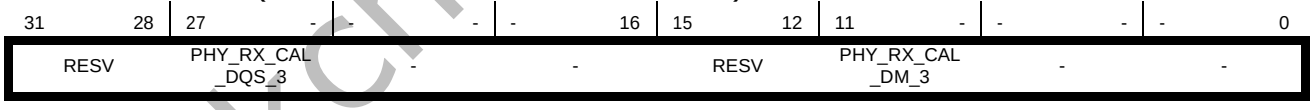
Name	Bits	Default	Range	Description
PHY_RX_CAL_DQ5_3	27:16	0x000	0x0-0xfff	RX Calibration codes for DQ5 for slice 3. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits
PHY_RX_CAL_DQ4_3	11:0	0x000	0x0-0xfff	RX Calibration codes for DQ4 for slice 3. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits

DENALI_PHY_440 (Address PHY_BASE_ADDR + 440)



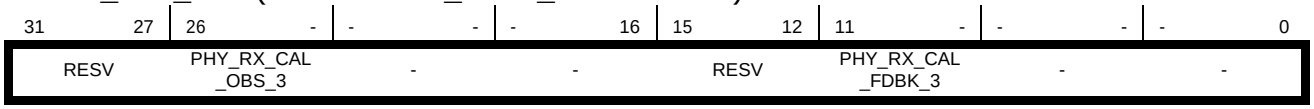
Name	Bits	Default	Range	Description
PHY_RX_CAL_DQ7_3	27:16	0x000	0x0-0xfff	RX Calibration codes for DQ7 for slice 3. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits
PHY_RX_CAL_DQ6_3	11:0	0x000	0x0-0xfff	RX Calibration codes for DQ6 for slice 3. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits

DENALI_PHY_441 (Address PHY_BASE_ADDR + 441)



Name	Bits	Default	Range	Description
PHY_RX_CAL_DQS_3	27:16	0x000	0x0-0xfff	RX Calibration codes for DQS for slice 3. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits
PHY_RX_CAL_DM_3	11:0	0x000	0x0-0xfff	RX Calibration codes for DM for slice 3. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits

DENALI_PHY_442 (Address PHY_BASE_ADDR + 442)



Name	Bits	Default	Range	Description
PHY_RX_CAL_OBS_3	26:16	0x000	0x0-0x7ff	RX Calibration results for slice 3. Bits (7:0) contain calibration results from DQ0-7. Bit (8) contains calibration result from DM. Bit (9)
PHY_RX_CAL_FDBK_3	11:0	0x000	0x0-0xfff	RX Calibration codes for FDBK for slice 3. Bits (5:0) contain rx_cal_code_down. Bits (11:6) contain rx_cal_code_up. Bits

DENALI_PHY_443 (Address PHY_BASE_ADDR + 443)

31	27	26	-	-	-	-	16	15	11	10	-	-	-	-	0
RESV		PHY_CLK_WR DQ1_SLAVE		-		-		RESV		PHY_CLK_WR DQ0_SLAVE		-		-	

Name	Bits	Default	Range	Description
PHY_CLK_WRDQ1_SLAVE_DELAY_3	26:16	0x000	0x0-0x7ff	Write clock slave delay setting for
PHY_CLK_WRDQ0_SLAVE_DELAY_3	10:0	0x000	0x0-0x7ff	Write clock slave delay setting for

DENALI_PHY_444 (Address PHY_BASE_ADDR + 444)

31	27	26	-	-	-	-	16	15	11	10	-	-	-	-	0
RESV		PHY_CLK_WR DQ3_SLAVE		-		-		RESV		PHY_CLK_WR DQ2_SLAVE		-		-	

Name	Bits	Default	Range	Description
PHY_CLK_WRDQ3_SLAVE_DELAY_3	26:16	0x000	0x0-0x7ff	Write clock slave delay setting for
PHY_CLK_WRDQ2_SLAVE_DELAY_3	10:0	0x000	0x0-0x7ff	Write clock slave delay setting for

DENALI_PHY_445 (Address PHY_BASE_ADDR + 445)

31	27	26	-	-	-	-	16	15	11	10	-	-	-	-	0
RESV		PHY_CLK_WR DQ5_SLAVE		-		-		RESV		PHY_CLK_WR DQ4_SLAVE		-		-	

Name	Bits	Default	Range	Description
PHY_CLK_WRDQ5_SLAVE_DELAY_3	26:16	0x000	0x0-0x7ff	Write clock slave delay setting for
PHY_CLK_WRDQ4_SLAVE_DELAY_3	10:0	0x000	0x0-0x7ff	Write clock slave delay setting for

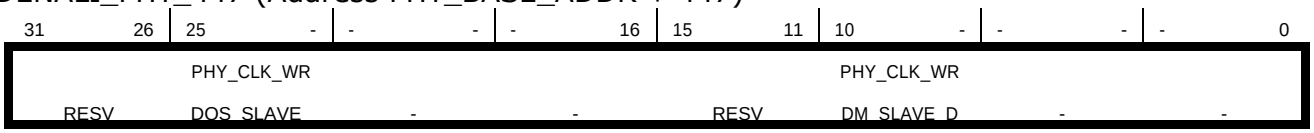
DENALI_PHY_446 (Address PHY_BASE_ADDR + 446)

31	27	26	-	-	-	-	16	15	11	10	-	-	-	-	0
RESV		PHY_CLK_WR DQ7_SLAVE		-		-		RESV		PHY_CLK_WR DQ6_SLAVE		-		-	

Name	Bits	Default	Range	Description

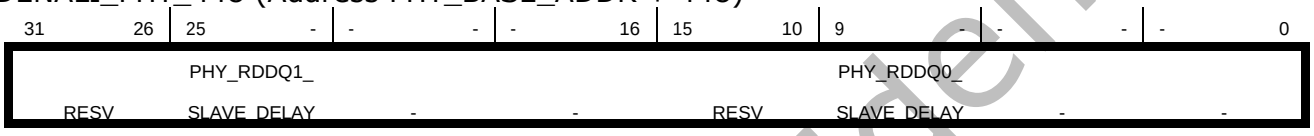
PHY_CLK_WRDQ7_SLAVE_DELAY_3	26:16	0x000	0x0-0x7ff	Write clock slave delay setting for
PHY_CLK_WRDQ6_SLAVE_DELAY_3	10:0	0x000	0x0-0x7ff	Write clock slave delay setting for

DENALI_PHY_447 (Address PHY_BASE_ADDR + 447)



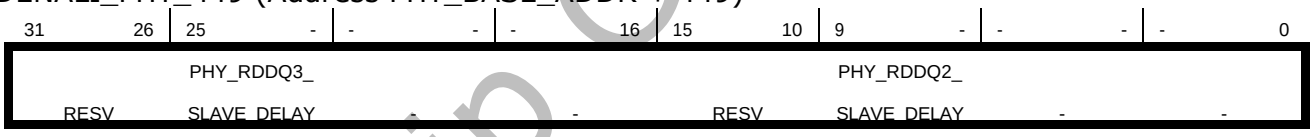
Name	Bits	Default	Range	Description
PHY_CLK_WRDQS_SLAVE_DELAY_3	25:16	0x000	0x0-0x3ff	Write clock slave delay setting for
PHY_CLK_WRDM_SLAVE_DELAY_3	10:0	0x000	0x0-0x7ff	Write clock slave delay setting for

DENALI_PHY_448 (Address PHY_BASE_ADDR + 448)



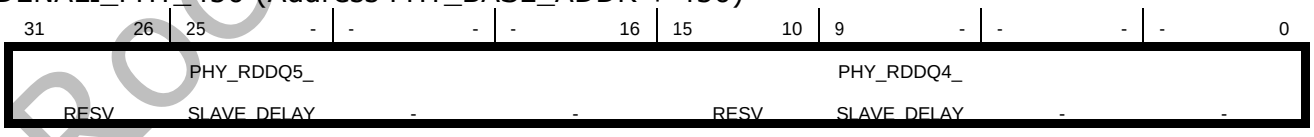
Name	Bits	Default	Range	Description
PHY_RDDQ1_SLAVE_DELAY_3	25:16	0x000	0x0-0x3ff	Read DQ1 slave delay setting for
PHY_RDDQ0_SLAVE_DELAY_3	9:0	0x000	0x0-0x3ff	Read DQ0 slave delay setting for

DENALI_PHY_449 (Address PHY_BASE_ADDR + 449)



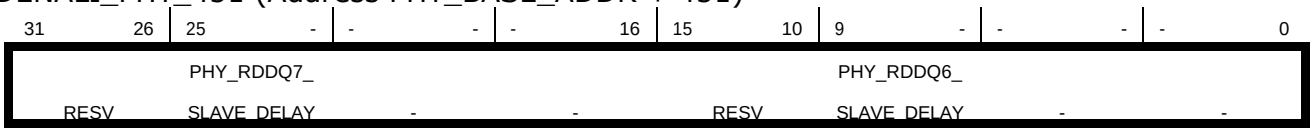
Name	Bits	Default	Range	Description
PHY_RDDQ3_SLAVE_DELAY_3	25:16	0x000	0x0-0x3ff	Read DQ3 slave delay setting for
PHY_RDDQ2_SLAVE_DELAY_3	9:0	0x000	0x0-0x3ff	Read DQ2 slave delay setting for

DENALI_PHY_450 (Address PHY_BASE_ADDR + 450)



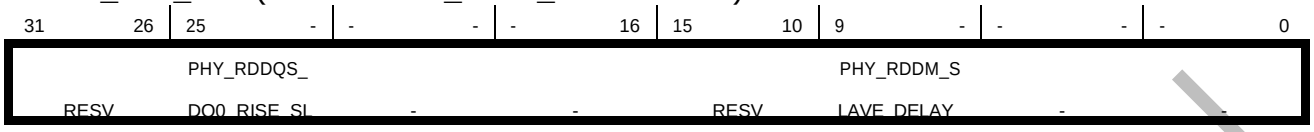
Name	Bits	Default	Range	Description
PHY_RDDQ5_SLAVE_DELAY_3	25:16	0x000	0x0-0x3ff	Read DQ5 slave delay setting for
PHY_RDDQ4_SLAVE_DELAY_3	9:0	0x000	0x0-0x3ff	Read DQ4 slave delay setting for

DENALI_PHY_451 (Address PHY_BASE_ADDR + 451)



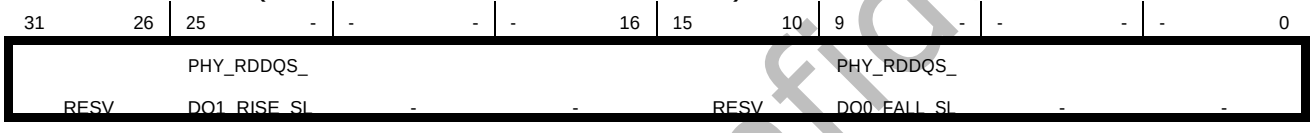
Name	Bits	Default	Range	Description
PHY_RDDQ7_SLAVE_DELAY_3	25:16	0x000	0x0-0x3ff	Read DQ7 slave delay setting for
PHY_RDDQ6_SLAVE_DELAY_3	9:0	0x000	0x0-0x3ff	Read DQ6 slave delay setting for

DENALI_PHY_452 (Address PHY_BASE_ADDR + 452)



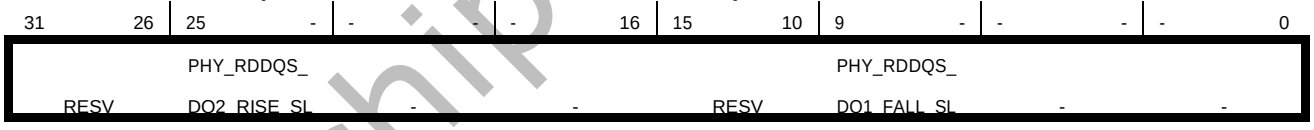
Name	Bits	Default	Range	Description
PHY_RDDQS_DQ0_RISE_SLAVE_DELAY_	25:16	0x000	0x0-0x3ff	Rising edge read DQS slave delay
PHY_RDDM_SLAVE_DELAY_3	9:0	0x000	0x0-0x3ff	Read DM/DBI slave delay setting for slice 3. May be used for data

DENALI_PHY_453 (Address PHY_BASE_ADDR + 453)



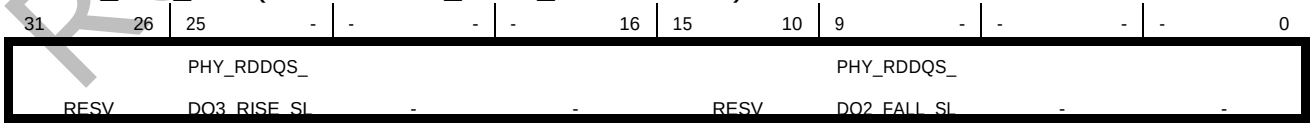
Name	Bits	Default	Range	Description
PHY_RDDQS_DQ1_RISE_SLAVE_DELAY_	25:16	0x000	0x0-0x3ff	Rising edge read DQS slave delay
PHY_RDDQS_DQ0_FALL_SLAVE_DELAY_	9:0	0x000	0x0-0x3ff	Falling edge read DQS slave delay

DENALI_PHY_454 (Address PHY_BASE_ADDR + 454)



Name	Bits	Default	Range	Description
PHY_RDDQS_DQ2_RISE_SLAVE_DELAY_	25:16	0x000	0x0-0x3ff	Rising edge read DQS slave delay
PHY_RDDQS_DQ1_FALL_SLAVE_DELAY_	9:0	0x000	0x0-0x3ff	Falling edge read DQS slave delay

DENALI_PHY_455 (Address PHY_BASE_ADDR + 455)



Name	Bits	Default	Range	Description
PHY_RDDQS_DQ3_RISE_SLAVE_DELAY_	25:16	0x000	0x0-0x3ff	Rising edge read DQS slave delay
PHY_RDDQS_DQ2_FALL_SLAVE_DELAY_	9:0	0x000	0x0-0x3ff	Falling edge read DQS slave delay

DENALI_PHY_456 (Address PHY_BASE_ADDR + 456)

31	26	25	-	-	-	-	16	15	10	9	-	-	-	-	0
		PHY_RDDQS_								PHY_RDDQS_					
RESV		DQ4_RISE_SL		-		-		RESV		DQ3_FALL_SL		-		-	

Name	Bits	Default	Range	Description
PHY_RDDQS_DQ4_RISE_SLAVE_DELAY_	25:16	0x000	0x0-0x3ff	Rising edge read DQS slave delay
PHY_RDDQS_DQ3_FALL_SLAVE_DELAY_	9:0	0x000	0x0-0x3ff	Falling edge read DQS slave delay

DENALI_PHY_457 (Address PHY_BASE_ADDR + 457)

31	26	25	-	-	-	-	16	15	10	9	-	-	-	-	0
		PHY_RDDQS_								PHY_RDDQS_					
RESV		DQ5_RISE_SL		-		-		RESV		DQ4_FALL_SL		-		-	

Name	Bits	Default	Range	Description
PHY_RDDQS_DQ5_RISE_SLAVE_DELAY_	25:16	0x000	0x0-0x3ff	Rising edge read DQS slave delay
PHY_RDDQS_DQ4_FALL_SLAVE_DELAY_	9:0	0x000	0x0-0x3ff	Falling edge read DQS slave delay

DENALI_PHY_458 (Address PHY_BASE_ADDR + 458)

31	26	25	-	-	-	-	16	15	10	9	-	-	-	-	0
		PHY_RDDQS_								PHY_RDDQS_					
RESV		DQ6_RISE_SL		-		-		RESV		DQ5_FALL_SL		-		-	

Name	Bits	Default	Range	Description
PHY_RDDQS_DQ6_RISE_SLAVE_DELAY_	25:16	0x000	0x0-0x3ff	Rising edge read DQS slave delay
PHY_RDDQS_DQ5_FALL_SLAVE_DELAY_	9:0	0x000	0x0-0x3ff	Falling edge read DQS slave delay

DENALI_PHY_459 (Address PHY_BASE_ADDR + 459)

31	26	25	-	-	-	-	16	15	10	9	-	-	-	-	0
		PHY_RDDQS_								PHY_RDDQS_					
RESV		DQ7_RISE_SL		-		-		RESV		DQ6_FALL_SL		-		-	

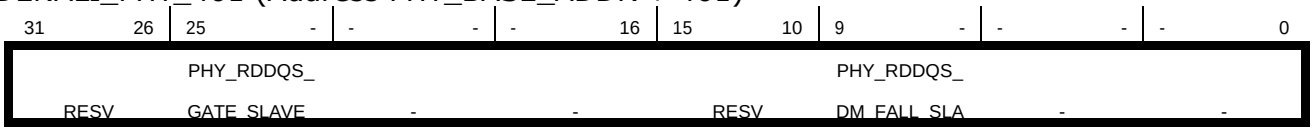
Name	Bits	Default	Range	Description
PHY_RDDQS_DQ7_RISE_SLAVE_DELAY_	25:16	0x000	0x0-0x3ff	Rising edge read DQS slave delay
PHY_RDDQS_DQ6_FALL_SLAVE_DELAY_	9:0	0x000	0x0-0x3ff	Falling edge read DQS slave delay

DENALI_PHY_460 (Address PHY_BASE_ADDR + 460)

31	26	25	-	-	-	-	16	15	10	9	-	-	-	-	0
		PHY_RDDQS_								PHY_RDDQS_					
RESV		DM_RISE_SLA		-		-		RESV		DQ7_FALL_SL		-		-	

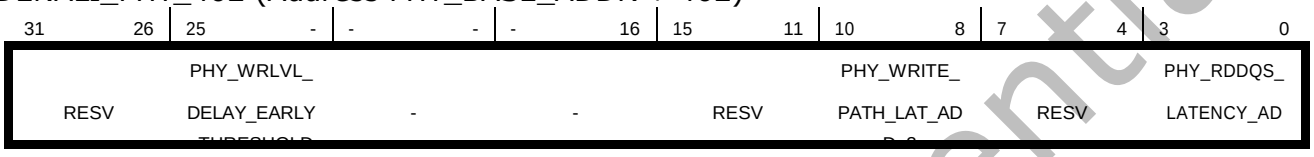
Name	Bits	Default	Range	Description
PHY_RDDQS_DM_RISE_SLAVE_DELAY_3	25:16	0x000	0x0-0x3ff	Rising edge read DQS slave delay
PHY_RDDQS_DQ7_FALL_SLAVE_DELAY_	9:0	0x000	0x0-0x3ff	Falling edge read DQS slave delay

DENALI_PHY_461 (Address PHY_BASE_ADDR + 461)



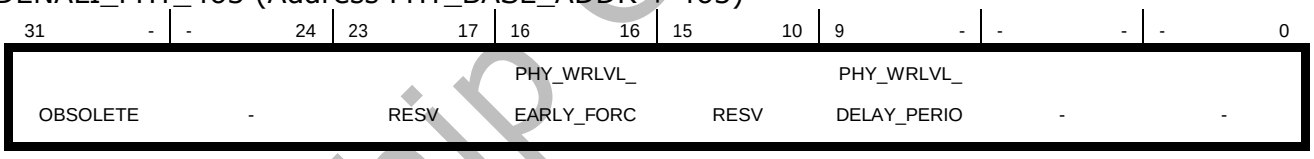
Name	Bits	Default	Range	Description
PHY_RDDQS_GATE_SLAVE_DELAY_3	25:16	0x000	0x0-0x3ff	Read DQS slave delay setting for
PHY_RDDQS_DM_FALL_SLAVE_DELAY_3	9:0	0x000	0x0-0x3ff	Falling edge read DQS slave delay

DENALI_PHY_462 (Address PHY_BASE_ADDR + 462)



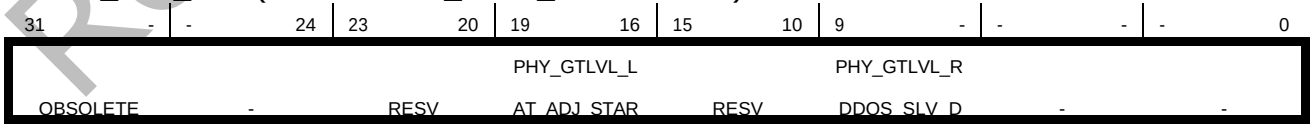
Name	Bits	Default	Range	Description
PHY_WRLVL_DELAY_EARLY_THRESHOLD_3	25:16	0x000	0x0-0x3ff	Write level delay threshold above which will be considered in
PHY_WRITE_PATH_LAT_ADD_3	10:8	0x0	0x0-0x7	Number of cycles to delay the incoming dfi_wrdata_en/dfi_wrdata
PHY_RDDQS_LATENCY_ADJUST_3	3:0	0x0	0x0-0xf	Number of cycles to delay the incoming dfi_rddata_en for read

DENALI_PHY_463 (Address PHY_BASE_ADDR + 463)



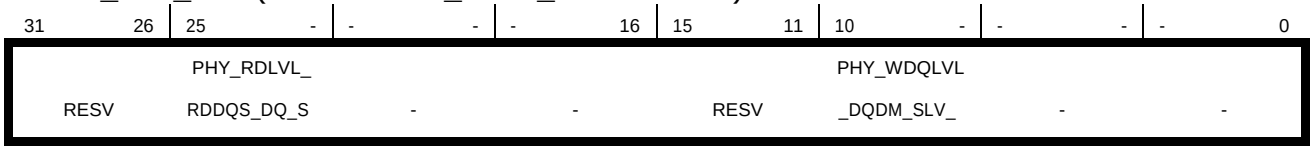
Name	Bits	Default	Range	Description
PHY_WRLVL_EARLY_FORCE_ZERO_3	16	0x0	0x0-0x1	Force the final write level delay value (that meets the early
PHY_WRLVL_DELAY_PERIOD_THRESHOLD_3	9:0	0x000	0x0-0x3ff	Write level delay threshold below which will add a cycle of write path

DENALI_PHY_464 (Address PHY_BASE_ADDR + 464)



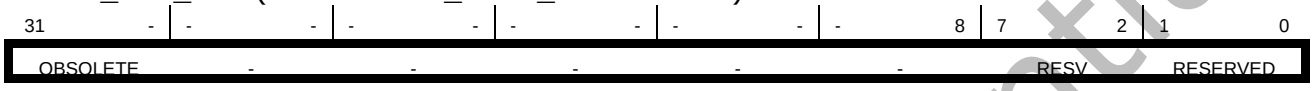
Name	Bits	Default	Range	Description
PHY_GTLVL_LAT_ADJ_START_3	19:16	0x0	0x0-0xf	Initial read DQS gate cycle delay from dfi_rddata_en during gate
PHY_GTLVL_RDDQS_SLV_DLY_START_3	9:0	0x000	0x0-0x3ff	Initial read DQS gate slave delay setting during gate training for slice

DENALI_PHY_465 (Address PHY_BASE_ADDR + 465)



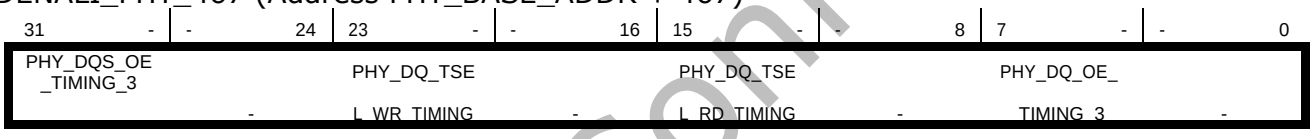
Name	Bits	Default	Range	Description
PHY_RDLVL_RDDQS_DQ_SLV_DLY_START_3	25:16	0x000	0x0-0x3ff	Read leveling starting value for the DQS/DQ slave delay settings for
PHY_WDQLVL_DQDM_SLV_DLY_START_3	10:0	0x000	0x0-0x7ff	Initial DQ/DM slave delay setting during write data leveling for slice

DENALI_PHY_466 (Address PHY_BASE_ADDR + 466)



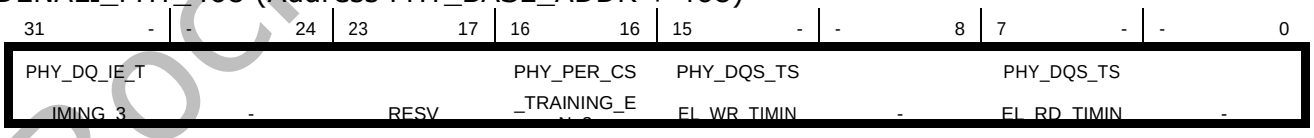
Name	Bits	Default	Range	Description
RESERVED	1:0	0x0	0x0-0x3	Reserved for future use. Refer to the regconfig files for the default

DENALI_PHY_467 (Address PHY_BASE_ADDR + 467)



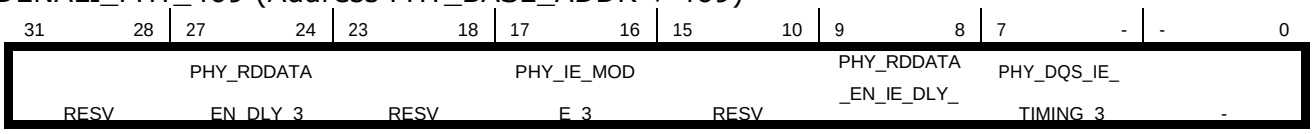
Name	Bits	Default	Range	Description
PHY_DQS_OE_TIMING_3	31:24	0x00	0x0-0xff	Start/end timing values for DQS
PHY_DQ_TSEL_WR_TIMING_3	23:16	0x00	0x0-0xff	Start/end timing values for DQ/DM write based termination enable and
PHY_DQ_TSEL_RD_TIMING_3	15:8	0x00	0x0-0xff	Start/end timing values for DQ/DM read based termination enable and
PHY_DQ_OE_TIMING_3	7:0	0x00	0x0-0xff	Start/end timing values for DQ/DM

DENALI_PHY_468 (Address PHY_BASE_ADDR + 468)



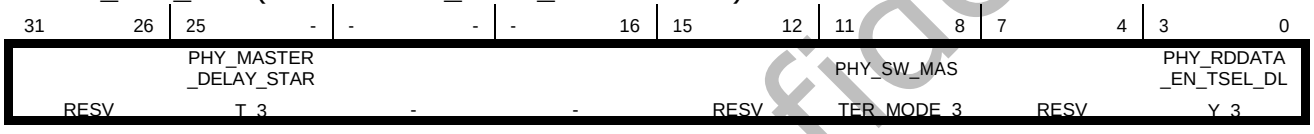
Name	Bits	Default	Range	Description
PHY_DQ_IE_TIMING_3	31:24	0x00	0x0-0xff	Start/end timing values for DQ/DM
PHY_PER_CS_TRAINING_EN_3	16	0x0	0x0-0x1	Enables the per-rank training and read/write timing capabilities. Must
PHY_DQS_TSEL_WR_TIMING_3	15:8	0x00	0x0-0xff	Start/end timing values for DQS write based termination enable and
PHY_DQS_TSEL_RD_TIMING_3	7:0	0x00	0x0-0xff	Start/end timing values for DQS read based termination enable and

DENALI_PHY_469 (Address PHY_BASE_ADDR + 469)



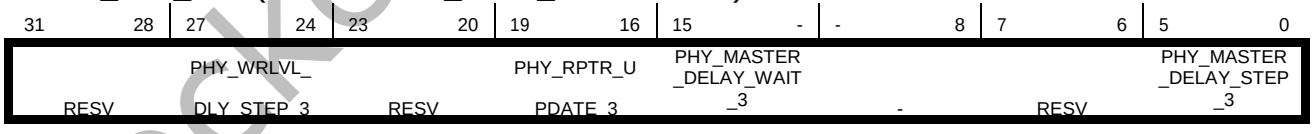
Name	Bits	Default	Range	Description
PHY_RDDATA_EN_DLY_3	27:24	0x0	0x0-0xf	Number of cycles that the dfi_rddata_en signal is early for
PHY_IE_MODE_3	17:16	0x0	0x0-0x3	Input enable mode bits for slice 3. Bit (0) enables the mode where the input enables are always on; set to
PHY_RDDATA_EN_IE_DLY_3	9:8	0x0	0x0-0x3	Number of cycles that the dfi_rddata_en signal is earlier than
PHY_DQS_IE_TIMING_3	7:0	0x00	0x0-0xff	Start/end timing values for DQS

DENALI_PHY_470 (Address PHY_BASE_ADDR + 470)



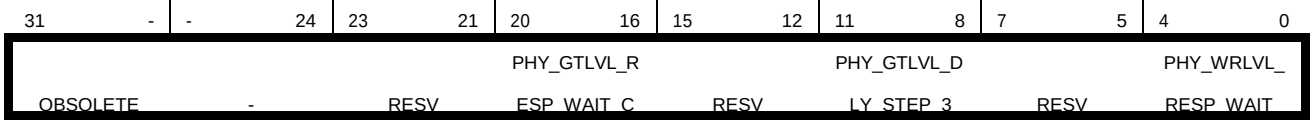
Name	Bits	Default	Range	Description
PHY_MASTER_DELAY_START_3	25:16	0x000	0x0-0x3ff	Start value for master delay line
PHY_SW_MASTER_MODE_3	11:8	0x0	0x0-0xf	Master delay line override settings for slice 3. Bit (0) enables software half clock mode. Bit (1) is the software half clock mode value. Bit
PHY_RDDATA_EN_TSEL_DLY_3	3:0	0x0	0x0-0xf	Number of cycles that the dfi_rddata_en signal is earlier than

DENALI_PHY_471 (Address PHY_BASE_ADDR + 471)



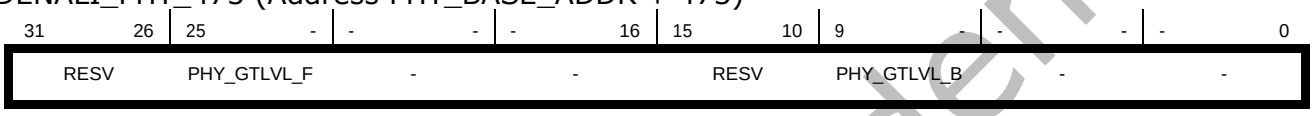
Name	Bits	Default	Range	Description
PHY_WRLVL_DLY_STEP_3	27:24	0x0	0x0-0xf	DQS slave delay step size during
PHY_RPTR_UPDATE_3	19:16	0x0	0x0-0xf	Offset in cycles from the dfi_rddata_en signal to release
PHY_MASTER_DELAY_WAIT_3	15:8	0x00	0x0-0xff	Wait cycles for master delay line locking algorithm for slice 3. Bits (3:0) are the cycle wait count after a calibration clock setting change.
PHY_MASTER_DELAY_STEP_3	5:0	0x00	0x0-0x3f	Incremental step size for master delay line locking algorithm for slice

DENALI_PHY_472 (Address PHY_BASE_ADDR + 472)



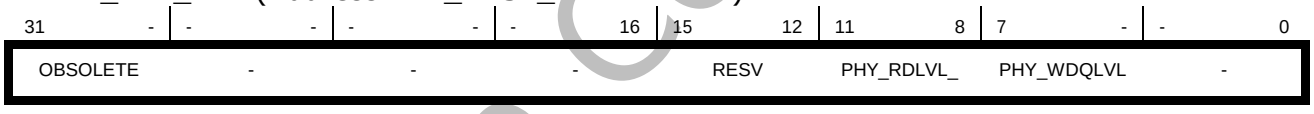
Name	Bits	Default	Range	Description
PHY_GTLVL_RESP_WAIT_CNT_3	20:16	0x00	0x0-0x1f	Number of cycles + 4 to wait between dfi_rddata_en and the sampling of the DQS during gate
PHY_GTLVL_DLY_STEP_3	11:8	0x0	0x0-0xf	DQS slave delay step size during
PHY_WRLVL_RESP_WAIT_CNT_3	4:0	0x00	0x0-0x1f	Number of cycles to wait between dfi_wrlvl_strobe and the sampling

DENALI_PHY_473 (Address PHY_BASE_ADDR + 473)



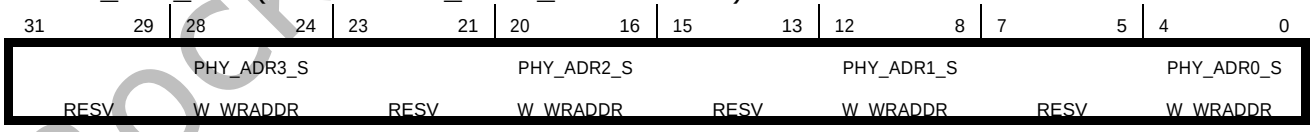
Name	Bits	Default	Range	Description
PHY_GTLVL_FINAL_STEP_3	25:16	0x000	0x0-0x3ff	Final backup step delay used in
PHY_GTLVL_BACK_STEP_3	9:0	0x000	0x0-0x3ff	Interim backup step delay used in

DENALI_PHY_474 (Address PHY_BASE_ADDR + 474)



Name	Bits	Default	Range	Description
PHY_RDLVL_DLY_STEP_3	11:8	0x0	0x0-0xf	DQS slave delay step size during
PHY_WDQLVL_DLY_STEP_3	7:0	0x00	0x0-0xff	DQ slave delay step size during

DENALI_PHY_512 (Address PHY_BASE_ADDR + 512)



Name	Bits	Default	Range	Description
PHY_ADR3_SW_WRADDR_SHIFT_0	28:24	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for address slice 0. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits

PHY_ADR2_SW_WRADDR_SHIFT_0	20:16	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for address slice 0. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits
PHY_ADR1_SW_WRADDR_SHIFT_0	12:8	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for address slice 0. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits
PHY_ADR0_SW_WRADDR_SHIFT_0	4:0	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for address slice 0. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits

DENALI_PHY_513 (Address PHY_BASE_ADDR + 513)

31 27	26 -	- -	- 16	15 13	12 8	7 5	4 0
RESV	PHY_ADR_CLK_WR_BYPAS	-	-	RESV	PHY_ADR5_SW_WRADDR_	RESV	PHY_ADR4_SW_WRADDR_

Name	Bits	Default	Range	Description
PHY_ADR_CLK_WR_BYPASS_SLAVE_DELAY_0	26:16	0x000	0x0-0x7ff	Write address clock bypass mode slave delay setting for address slice
PHY_ADR5_SW_WRADDR_SHIFT_0	12:8	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for address slice 0. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits
PHY_ADR4_SW_WRADDR_SHIFT_0	4:0	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for address slice 0. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits

DENALI_PHY_514 (Address PHY_BASE_ADDR + 514)

31 -	- -	- -	- 16	15 11	10 8	7 1	0 0
OBSOLETE	-	-	-	RESV	SC_PHY_ADR_MANUAL_CL	RESV	PHY_ADR_CLK_BYPASS_O

Name	Bits	Default	Range	Description

SC_PHY_ADR_MANUAL_CLEAR_0	10:8	0x0	0x0-0x7	Manual reset/clear of internal logic for address slice 0. Bit (0) is reset of master delay min/max lock values. Bit (1) is manual reset of
PHY_ADR_CLK_BYPASS_OVERRIDE_0	0	0x0	0x0-0x1	Bypass mode override setting for

DENALI_PHY_515 (Address PHY_BASE_ADDR + 515)

31 - 0
PHY_ADR_LPBK_RESULT

Name	Bits	Default	Range	Description
PHY_ADR_LPBK_RESULT_OBS_0	31:0	0x00000000	0x0-0xffffffff	Observation register containing loopback status/results for address

DENALI_PHY_516 (Address PHY_BASE_ADDR + 516)

31 - 24	23 - 19	18 - 16	15 - 0
OBSOLETE	RESV	PHY_ADR_MASTER_DLY_L	PHY_ADR_LPBK_ERROR_C

Name	Bits	Default	Range	Description
PHY_ADR_MASTER_DLY_LOCK_OBS_SELECT_0	18:16	0x0	0x0-0x7	Select value to map the internal master delay observation registers to the accessible master delay
PHY_ADR_LPBK_ERROR_COUNT_OBS_0	15:0	0x0000	0x0-0xffff	Observation register containing total number of loopback error data

DENALI_PHY_517 (Address PHY_BASE_ADDR + 517)

31 - 27	26 - 24	23 - 19	18 - 16	15 - 10	9 - 0
RESV	PHY_ADR_SLV_DLY_ENC_	RESV	PHY_ADR_SLAVE_LOOP_C	RESV	PHY_ADR_MASTER_DLY_L

Name	Bits	Default	Range	Description
PHY_ADR_SLV_DLY_ENC_OBS_SELECT_	26:24	0x0	0x0-0x7	Select value to map the addr bits delay observation registers to the
PHY_ADR_SLAVE_LOOP_CNT_UPDATE_	18:16	0x0	0x0-0x7	Sets the frequency by which the slave delay encoded value holding
PHY_ADR_MASTER_DLY_LOCK_OBS_0	9:0	0x000	0x0-0x3ff	Observation register for master delay results for address slice 0.

DENALI_PHY_518 (Address PHY_BASE_ADDR + 518)

31 - 25	24 - 24	23 - 22	21 - 16	15 - 9	8 - 8	7 - 1	0 - 0
RESV	PHY_ADR_PWR_RDC_DISA	RESV	PHY_ADR_LPBK_CONTROL	RESV	PHY_ADR_TSEL_ENABLE_0	RESV	SC_PHY_ADR_SNAP_OBS_

Name	Bits	Default	Range	Description
PHY_ADR_PWR_RDC_DISABLE_0	24	0x0	0x0-0x1	adr slice power reduction disable
PHY_ADR_LPBK_CONTROL_0	21:16	0x00	0x0-0x3f	Loopback control bits for address
PHY_ADR_TSEL_ENABLE_0	8	0x0	0x0-0x1	Enables tsel_en for address slice 0.
SC_PHY_ADR_SNAP_OBS_REGS_0	0	0x0	0x0-0x1	Initiates a snapshot of the internal observation registers for address

DENALI_PHY_519 (Address PHY_BASE_ADDR + 519)

31 - 24	23 - 17	16 - 16	15 - 11	10 - 8	7 - 2	1 - 0
OBSOLETE	RESV	PHY_ADR_IE_MODE_0	RESV	PHY_ADR_WRADDR_SHIFT	RESV	PHY_ADR_TYPE_0

Name	Bits	Default	Range	Description
PHY_ADR_IE_MODE_0	16	0x0	0x0-0x1	Input enable control for address
PHY_ADR_WRADDR_SHIFT_OBS_0	10:8	0x0	0x0-0x7	Observation register for automatic half cycle and cycle shift values for
PHY_ADR_TYPE_0	1:0	0x0	0x0-0x3	DRAM type for address slice 0.

DENALI_PHY_520 (Address PHY_BASE_ADDR + 520)

31 - 16	15 - 15	14 - 0
OBSOLETE	RESV	PHY_ADR_DDL_MODE_0

Name	Bits	Default	Range	Description
PHY_ADR_DDL_MODE_0	14:0	0x0000	0x0-0x7fff	DDL mode for address slice 0.

DENALI_PHY_521 (Address PHY_BASE_ADDR + 521)

31 - 0
PHY_ADR_DDL_TEST_OBS

Name	Bits	Default	Range	Description
PHY_ADR_DDL_TEST_OBS_0	31:0	0x00000000	0x0-0xffffffff	DDL test observation for address

DENALI_PHY_522 (Address PHY_BASE_ADDR + 522)

31 - 0
PHY_ADR_DDL_TEST_MST

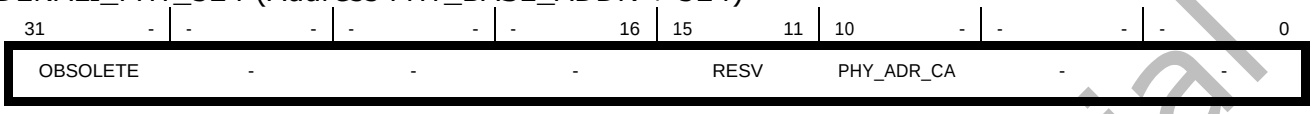
Name	Bits	Default	Range	Description
PHY_ADR_DDL_TEST_MSTR_DLY_OBS_0	31:0	0x00000000	0x0-0xffffffff	DDL test observation delays for address slice 0 master DDL.

DENALI_PHY_523 (Address PHY_BASE_ADDR + 523)

31 - 27	26 - 16	15 - 11	10 - 0
OBSOLETE	RESV	PHY_ADR_DDL_TEST_MST	RESV

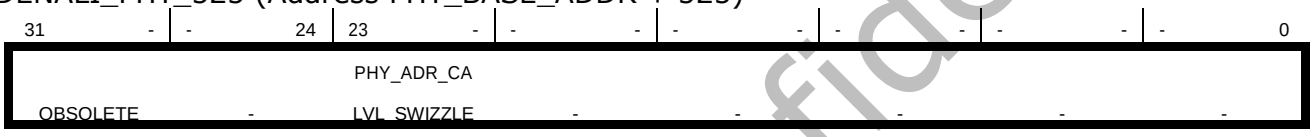
Name	Bits	Default	Range	Description
PHY_ADR_CALVL_COARSE_DLY_0	26:16	0x000	0x0-0x7ff	Coarse CA training DLL increment
PHY_ADR_CALVL_START_0	10:0	0x000	0x0-0x7ff	CA training DLL start value for

DENALI_PHY_524 (Address PHY_BASE_ADDR + 524)



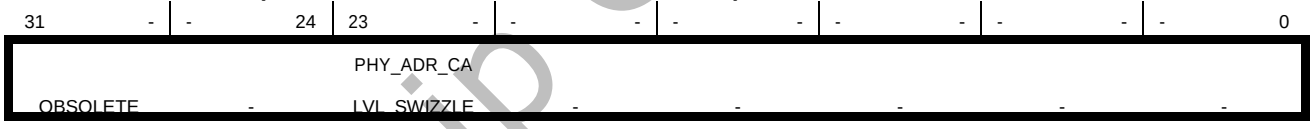
Name	Bits	Default	Range	Description
PHY_ADR_CALVL_QTR_0	10:0	0x000	0x0-0x7ff	CA training DLL quarter cycle delay

DENALI_PHY_525 (Address PHY_BASE_ADDR + 525)



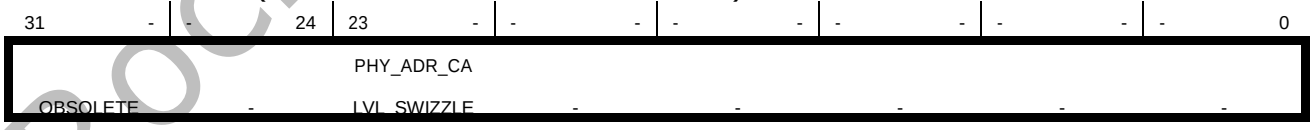
Name	Bits	Default	Range	Description
PHY_ADR_CALVL_SWIZZLE0_0_0	23:0	0x000000	0x0-0xffffff	CA training RD DQ bit swizzlemap

DENALI_PHY_526 (Address PHY_BASE_ADDR + 526)



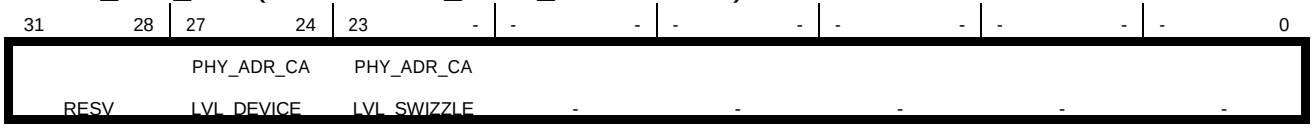
Name	Bits	Default	Range	Description
PHY_ADR_CALVL_SWIZZLE1_0_0	23:0	0x000000	0x0-0xffffff	CA training RD DQ bit swizzlemap

DENALI_PHY_527 (Address PHY_BASE_ADDR + 527)



Name	Bits	Default	Range	Description
PHY_ADR_CALVL_SWIZZLE0_1_0	23:0	0x000000	0x0-0xffffff	CA training RD DQ bit swizzlemap

DENALI_PHY_528 (Address PHY_BASE_ADDR + 528)



Name	Bits	Default	Range	Description

PHY_ADR_CALVL_DEVICE_MAP_0	27:24	0x0	0x0-0xf	Defines the CA training device map
PHY_ADR_CALVL_SWIZZLE1_1_0	23:0	0x000000	0x0-0xffffff	CA training RD DQ bit swizzle map

DENALI_PHY_529 (Address PHY_BASE_ADDR + 529)

31 28	27 24	23 20	19 16	15 10	9 8	7 2	1 0
RESV	PHY_ADR_CALVL_RESP_W	RESV	PHY_ADR_CALVL_CAPTUR	RESV	PHY_ADR_CALVL_NUM_PAT	RESV	PHY_ADR_CALVL_RANK_CT

Name	Bits	Default	Range	Description
PHY_ADR_CALVL_RESP_WAIT_CNT_0	27:24	0x0	0x0-0xf	Number of samples to wait for response during CA training for
PHY_ADR_CALVL_CAPTURE_CNT_0	19:16	0x0	0x0-0xf	Number of samples to take at each ADDR slave delay setting during
PHY_ADR_CALVL_NUM_PATTERNS_0	9:8	0x0	0x0-0x3	Sets the number of patterns to use during CA training for address slice
PHY_ADR_CALVL_RANK_CTRL_0	1:0	0x0	0x0-0x3	Defines the CA training rank control

DENALI_PHY_530 (Address PHY_BASE_ADDR + 530)

31 27	26 24	23 17	16 16	15 9	8 8	7 1	0 0
RESV	PHY_ADR_CALVL_OBS_SEL	RESV	SC_PHY_ADR_CALVL_ERR	RESV	SC_PHY_ADR_CALVL_DEB	RESV	PHY_ADR_CALVL_DEBUG

Name	Bits	Default	Range	Description
PHY_ADR_CALVL_OBS_SELECT_0	26:24	0x0	0x0-0x7	CA bit lane to observe result from (OBS0 and OBS1) during CA
SC_PHY_ADR_CALVL_ERROR_CLR_0	16	0x0	0x0-0x1	Clears the CA training state machine error status for address
SC_PHY_ADR_CALVL_DEBUG_CONT_0	8	0x0	0x0-0x1	Allows the CA training state machine to advance (when in
PHY_ADR_CALVL_DEBUG_MODE_0	0	0x0	0x0-0x1	Enables CA training debug mode for address slice 0. Set to 1 to

DENALI_PHY_531 (Address PHY_BASE_ADDR + 531)

31 -	- -	- -	- -	- -	- -	- -	- 0
PHY_ADR_CA	-	-	-	-	-	-	-

Name	Bits	Default	Range	Description
PHY_ADR_CALVL_OBS0_0	31:0	0x00000000	0x0-0xffffffff	Observation register for CA training

DENALI_PHY_532 (Address PHY_BASE_ADDR + 532)

31 -	- -	- -	- -	- -	- -	- -	- 0
PHY_ADR_CA	-	-	-	-	-	-	-

Name	Bits	Default	Range	Description

PHY_ADR_CALVL_OBS1_0	31:0	0x00000000	0x0-0xffffffff	Observation register for CA training

DENALI_PHY_533 (Address PHY_BASE_ADDR + 533)

31 - 24	23 20	19 - 0
OBSOLETE	RESV	PHY_ADR_CA

Name	Bits	Default	Range	Description
PHY_ADR_CALVL_FG_0_0	19:0	0x00000	0x0-0xfffff	CA training foreground pattern 0 for

DENALI_PHY_534 (Address PHY_BASE_ADDR + 534)

31 - 24	23 20	19 - 0
OBSOLETE	RESV	PHY_ADR_CA

Name	Bits	Default	Range	Description
PHY_ADR_CALVL_BG_0_0	19:0	0x00000	0x0-0xfffff	CA training background pattern 0

DENALI_PHY_535 (Address PHY_BASE_ADDR + 535)

31 - 24	23 20	19 - 0
OBSOLETE	RESV	PHY_ADR_CA

Name	Bits	Default	Range	Description
PHY_ADR_CALVL_FG_1_0	19:0	0x00000	0x0-0xfffff	CA training foreground pattern 1 for

DENALI_PHY_536 (Address PHY_BASE_ADDR + 536)

31 - 24	23 20	19 - 0
OBSOLETE	RESV	PHY_ADR_CA

Name	Bits	Default	Range	Description
PHY_ADR_CALVL_BG_1_0	19:0	0x00000	0x0-0xfffff	CA training background pattern 1

DENALI_PHY_537 (Address PHY_BASE_ADDR + 537)

31 - 24	23 20	19 - 0
OBSOLETE	RESV	PHY_ADR_CA

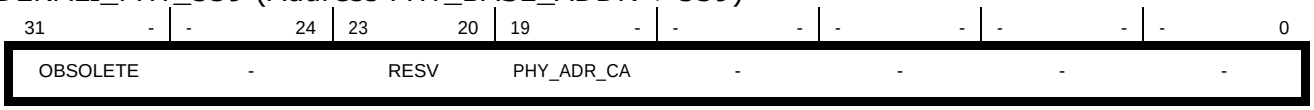
Name	Bits	Default	Range	Description
PHY_ADR_CALVL_FG_2_0	19:0	0x00000	0x0-0xfffff	CA training foreground pattern 2 for

DENALI_PHY_538 (Address PHY_BASE_ADDR + 538)

31 - 24	23 20	19 - 0
OBSOLETE	RESV	PHY_ADR_CA

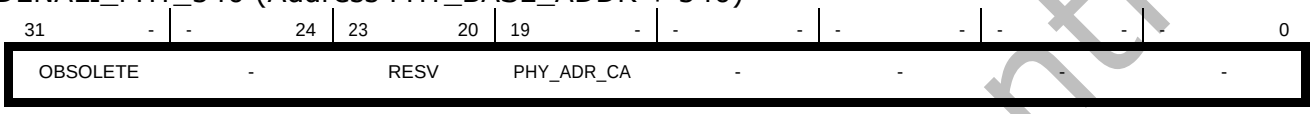
Name	Bits	Default	Range	Description
PHY_ADR_CALVL_BG_2_0	19:0	0x00000	0x0-0xfffff	CA training background pattern 2

DENALI_PHY_539 (Address PHY_BASE_ADDR + 539)



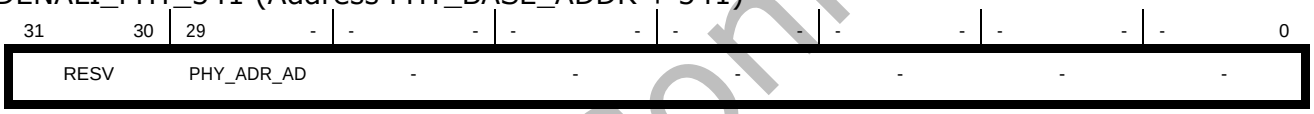
Name	Bits	Default	Range	Description
PHY_ADR_CALVL_FG_3_0	19:0	0x00000	0x0-0xfffff	CA training foreground pattern 3 for

DENALI_PHY_540 (Address PHY_BASE_ADDR + 540)



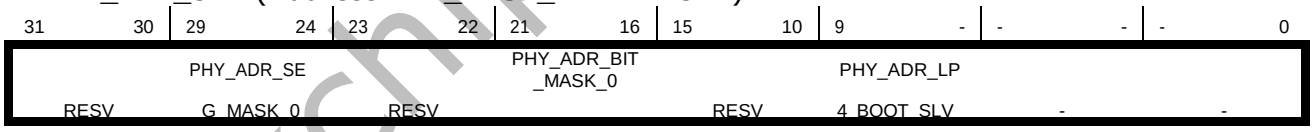
Name	Bits	Default	Range	Description
PHY_ADR_CALVL_BG_3_0	19:0	0x00000	0x0-0xfffff	CA training background pattern 3

DENALI_PHY_541 (Address PHY_BASE_ADDR + 541)



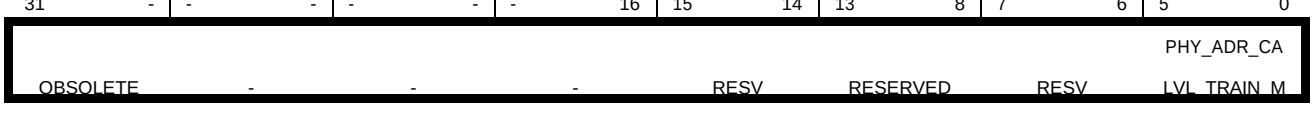
Name	Bits	Default	Range	Description
PHY_ADR_ADDR_SEL_0	29:0	0x00000000	0x0-0x3fffffff	Mux select to map in LPDDR4

DENALI_PHY_542 (Address PHY_BASE_ADDR + 542)



Name	Bits	Default	Range	Description
PHY_ADR_SEG_MASK_0	29:24	0x00	0x0-0x3f	Segment mask bit for address slice 0. Set to 1 to indicate that the bit is
PHY_ADR_BIT_MASK_0	21:16	0x00	0x0-0x3f	Mask bit for address slice 0. Set to 1 to indicate that the bit is masked
PHY_ADR_LP4_BOOT_SLV_DELAY_0	9:0	0x000	0x0-0x3ff	Address slave delay setting during the LPDDR4 boot frequency

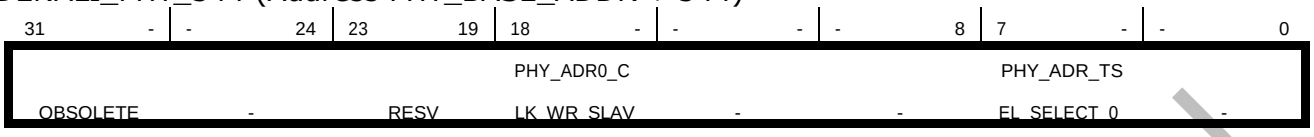
DENALI_PHY_543 (Address PHY_BASE_ADDR + 543)



Name	Bits	Default	Range	Description

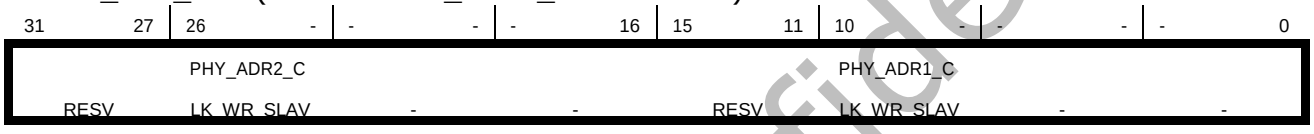
RESERVED	13:8	0x00	0x0-0x3f	Reserved for future use. Refer to the regconfig files for the default
PHY_ADR_CALVL_TRAIN_MASK_0	5:0	0x00	0x0-0x3f	Mask bit for CA training participation for address slice 0. Set

DENALI_PHY_544 (Address PHY_BASE_ADDR + 544)



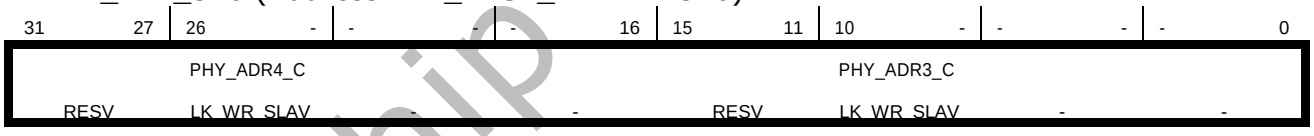
Name	Bits	Default	Range	Description
PHY_ADR0_CLK_WR_SLAVE_DELAY_0	18:8	0x000	0x0-0x7ff	Address slice slave delay setting
PHY_ADR_TSEL_SELECT_0	7:0	0x00	0x0-0xff	Tsel select values for address slice

DENALI_PHY_545 (Address PHY_BASE_ADDR + 545)



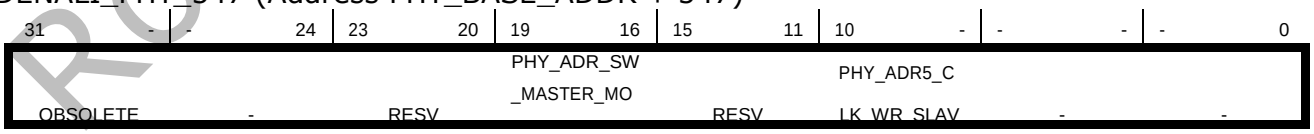
Name	Bits	Default	Range	Description
PHY_ADR2_CLK_WR_SLAVE_DELAY_0	26:16	0x000	0x0-0x7ff	Address slice slave delay setting
PHY_ADR1_CLK_WR_SLAVE_DELAY_0	10:0	0x000	0x0-0x7ff	Address slice slave delay setting

DENALI_PHY_546 (Address PHY_BASE_ADDR + 546)



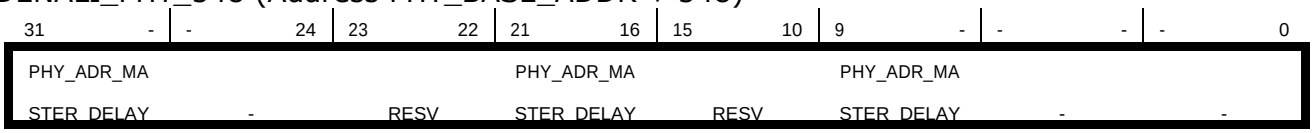
Name	Bits	Default	Range	Description
PHY_ADR4_CLK_WR_SLAVE_DELAY_0	26:16	0x000	0x0-0x7ff	Address slice slave delay setting
PHY_ADR3_CLK_WR_SLAVE_DELAY_0	10:0	0x000	0x0-0x7ff	Address slice slave delay setting

DENALI_PHY_547 (Address PHY_BASE_ADDR + 547)



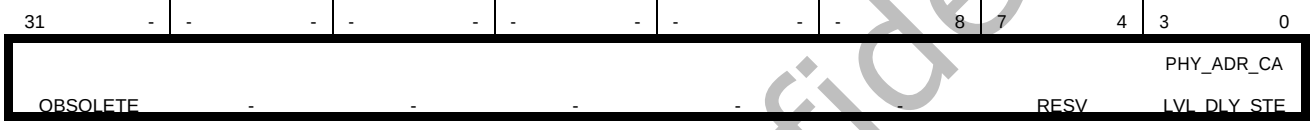
Name	Bits	Default	Range	Description
PHY_ADR_SW_MASTER_MODE_0	19:16	0x0	0x0-0xf	Master delay line override settings for address slice 0. Bit (0) enables software half clock mode. Bit (1) is the software half clock mode value.
PHY_ADR5_CLK_WR_SLAVE_DELAY_0	10:0	0x000	0x0-0x7ff	Address slice slave delay setting

DENALI_PHY_548 (Address PHY_BASE_ADDR + 548)



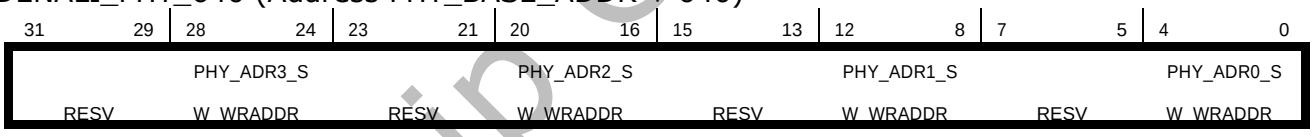
Name	Bits	Default	Range	Description
PHY_ADR_MASTER_DELAY_WAIT_0	31:24	0x00	0x0-0xff	Wait cycles for master delay line locking algorithm for address slice 0. Bits (3:0) is the cycle wait count after a calibration clock setting
PHY_ADR_MASTER_DELAY_STEP_0	21:16	0x00	0x0-0x3f	Incremental step size for master delay line locking algorithm for
PHY_ADR_MASTER_DELAY_START_0	9:0	0x000	0x0-0x3ff	Start value for master delay line locking algorithm for address slice

DENALI_PHY_549 (Address PHY_BASE_ADDR + 549)



Name	Bits	Default	Range	Description
PHY_ADR_CALVL_DLY_STEP_0	3:0	0x0	0x0-0xf	Sets the delay step size plus 1 during CA training for address slice

DENALI_PHY_640 (Address PHY_BASE_ADDR + 640)



Name	Bits	Default	Range	Description
PHY_ADR3_SW_WRADDR_SHIFT_1	28:24	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for address slice 1. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits
PHY_ADR2_SW_WRADDR_SHIFT_1	20:16	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for address slice 1. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits

PHY_ADR1_SW_WRADDR_SHIFT_1	12:8	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for address slice 1. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits
PHY_ADR0_SW_WRADDR_SHIFT_1	4:0	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for address slice 1. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits

DENALI_PHY_641 (Address PHY_BASE_ADDR + 641)

31 27	26 -	- -	- 16	15 13	12 8	7 5	4 0
RESV	PHY_ADR_CLK_WR_BYPAS	-	-	RESV	PHY_ADR5_SW_WRADDR_	RESV	PHY_ADR4_SW_WRADDR_

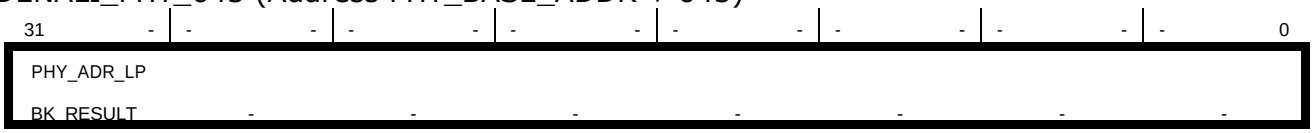
Name	Bits	Default	Range	Description
PHY_ADR_CLK_WR_BYPASS_SLAVE_DELAY_1	26:16	0x000	0x0-0x7ff	Write address clock bypass mode slave delay setting for address slice
PHY_ADR5_SW_WRADDR_SHIFT_1	12:8	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for address slice 1. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits
PHY_ADR4_SW_WRADDR_SHIFT_1	4:0	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for address slice 1. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits

DENALI_PHY_642 (Address PHY_BASE_ADDR + 642)

31 -	- -	- -	- 16	15 11	10 8	7 1	0 0
OBSOLETE	-	-	-	RESV	SC_PHY_ADR_MANUAL_CL	RESV	PHY_ADR_CLK_BYPASS_O

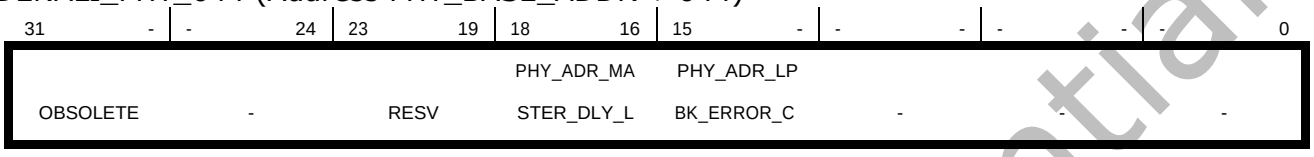
Name	Bits	Default	Range	Description
SC_PHY_ADR_MANUAL_CLEAR_1	10:8	0x0	0x0-0x7	Manual reset/clear of internal logic for address slice 1. Bit (0) is reset of master delay min/max lock values. Bit (1) is manual reset of
PHY_ADR_CLK_BYPASS_OVERRIDE_1	0	0x0	0x0-0x1	Bypass mode override setting for

DENALI_PHY_643 (Address PHY_BASE_ADDR + 643)



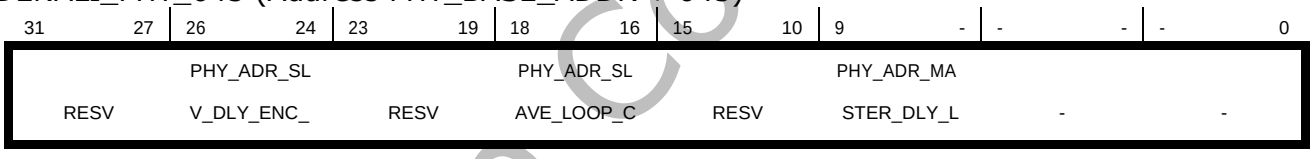
Name	Bits	Default	Range	Description
PHY_ADR_LPBK_RESULT_OBS_1	31:0	0x00000000	0x0-0xffffffff	Observation register containing loopback status/results for address

DENALI_PHY_644 (Address PHY_BASE_ADDR + 644)



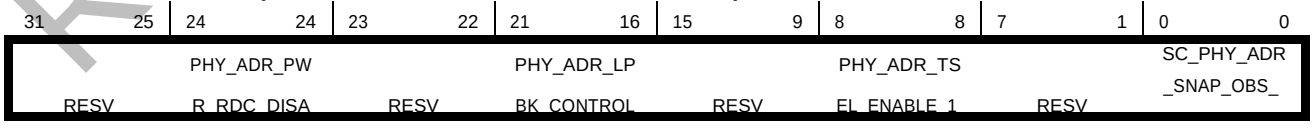
Name	Bits	Default	Range	Description
PHY_ADR_MASTER_DLY_LOCK_OBS_SELECT_1	18:16	0x0	0x0-0x7	Select value to map the internal master delay observation registers to the accessible master delay
PHY_ADR_LPBK_ERROR_COUNT_OBS_1	15:0	0x0000	0x0-0xffff	Observation register containing total number of loopback error data

DENALI_PHY_645 (Address PHY_BASE_ADDR + 645)



Name	Bits	Default	Range	Description
PHY_ADR_SLV_DLY_ENC_OBS_SELECT_	26:24	0x0	0x0-0x7	Select value to map the addr bits delay observation registers to the
PHY_ADR_SLAVE_LOOP_CNT_UPDATE_	18:16	0x0	0x0-0x7	Sets the frequency by which the slave delay encoded value holding
PHY_ADR_MASTER_DLY_LOCK_OBS_1	9:0	0x000	0x0-0x3ff	Observation register for master delay results for address slice 1.

DENALI_PHY_646 (Address PHY_BASE_ADDR + 646)



Name	Bits	Default	Range	Description
PHY_ADR_PWR_RDC_DISABLE_1	24	0x0	0x0-0x1	adr slice power reduction disable
PHY_ADR_LPBK_CONTROL_1	21:16	0x00	0x0-0x3f	Loopback control bits for address
PHY_ADR_TSEL_ENABLE_1	8	0x0	0x0-0x1	Enables tsel_en for address slice 1.

SC_PHY_ADR_SNAP_OBS_REGS_1	0	0x0	0x0-0x1	Initiates a snapshot of the internal observation registers for address

DENALI_PHY_647 (Address PHY_BASE_ADDR + 647)

31 - 24	23 - 17	16 - 16	15 - 11	10 - 8	7 - 2	1 - 0
OBSOLETE	RESV	PHY_ADR_IE_MODE_1	RESV	PHY_ADR_WRADDR_SHIFT	RESV	PHY_ADR_TYPE_1

Name	Bits	Default	Range	Description
PHY_ADR_IE_MODE_1	16	0x0	0x0-0x1	Input enable control for address
PHY_ADR_WRADDR_SHIFT_OBS_1	10:8	0x0	0x0-0x7	Observation register for automatic half cycle and cycle shift values for
PHY_ADR_TYPE_1	1:0	0x0	0x0-0x3	DRAM type for address slice 1.

DENALI_PHY_648 (Address PHY_BASE_ADDR + 648)

31 - 16	15 - 15	14 - 0
OBSOLETE	RESV	PHY_ADR_DDL_MODE_1

Name	Bits	Default	Range	Description
PHY_ADR_DDL_MODE_1	14:0	0x0000	0x0-0x7fff	DDL mode for address slice 1.

DENALI_PHY_649 (Address PHY_BASE_ADDR + 649)

31 - 0
PHY_ADR_DDL_TEST_OBS

Name	Bits	Default	Range	Description
PHY_ADR_DDL_TEST_OBS_1	31:0	0x00000000	0x0-0xffffffff	DDL test observation for address

DENALI_PHY_650 (Address PHY_BASE_ADDR + 650)

31 - 0
PHY_ADR_DDL_TEST_MST

Name	Bits	Default	Range	Description
PHY_ADR_DDL_TEST_MSTR_DLY_OBS_1	31:0	0x00000000	0x0-0xffffffff	DDL test observation delays for address slice 1 master DDL.

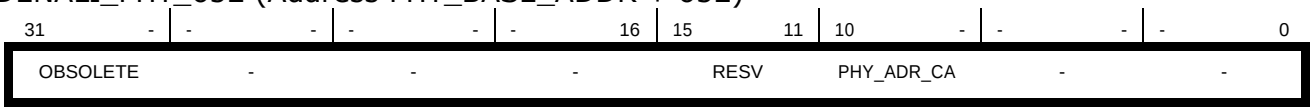
DENALI_PHY_651 (Address PHY_BASE_ADDR + 651)

31 - 27	26 - 16	15 - 11	10 - 0
RESV	PHY_ADR_CALVL_COARSE	RESV	PHY_ADR_CALVL_START_1

Name	Bits	Default	Range	Description
PHY_ADR_CALVL_COARSE_DLY_1	26:16	0x000	0x0-0x7ff	Coarse CA training DLL increment

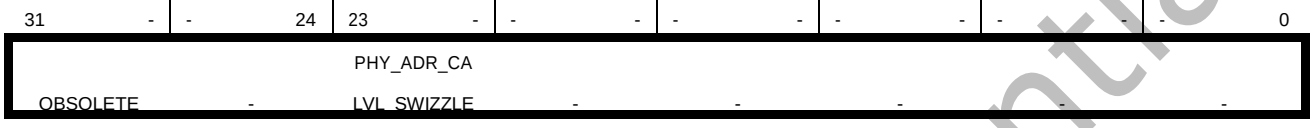
PHY_ADR_CALVL_START_1	10:0	0x000	0x0-0x7ff	CA training DLL start value for

DENALI_PHY_652 (Address PHY_BASE_ADDR + 652)



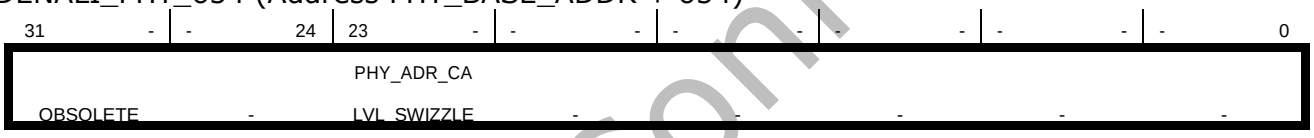
Name	Bits	Default	Range	Description
PHY_ADR_CALVL_QTR_1	10:0	0x000	0x0-0x7ff	CA training DLL quarter cycle delay

DENALI_PHY_653 (Address PHY_BASE_ADDR + 653)



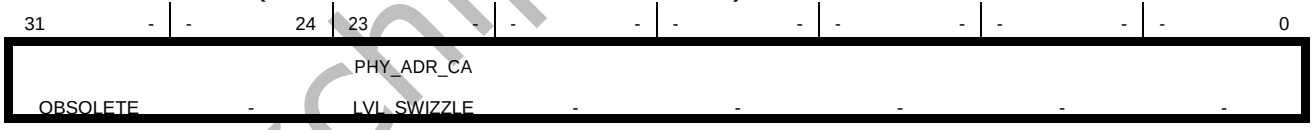
Name	Bits	Default	Range	Description
PHY_ADR_CALVL_SWIZZLE0_0_1	23:0	0x000000	0x0-0xffffff	CA training RD DQ bit swizzlemap

DENALI_PHY_654 (Address PHY_BASE_ADDR + 654)



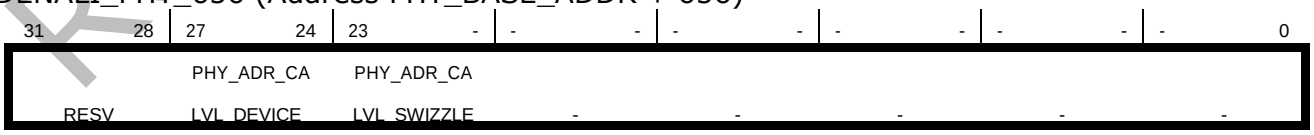
Name	Bits	Default	Range	Description
PHY_ADR_CALVL_SWIZZLE1_0_1	23:0	0x000000	0x0-0xffffff	CA training RD DQ bit swizzlemap

DENALI_PHY_655 (Address PHY_BASE_ADDR + 655)



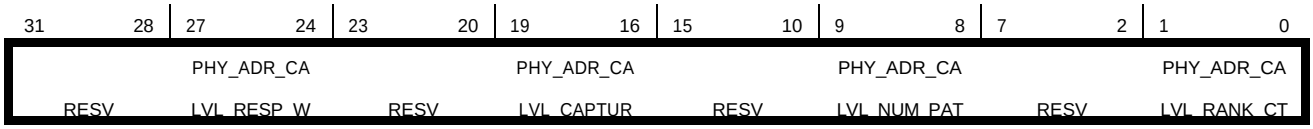
Name	Bits	Default	Range	Description
PHY_ADR_CALVL_SWIZZLE0_1_1	23:0	0x000000	0x0-0xffffff	CA training RD DQ bit swizzlemap

DENALI_PHY_656 (Address PHY_BASE_ADDR + 656)



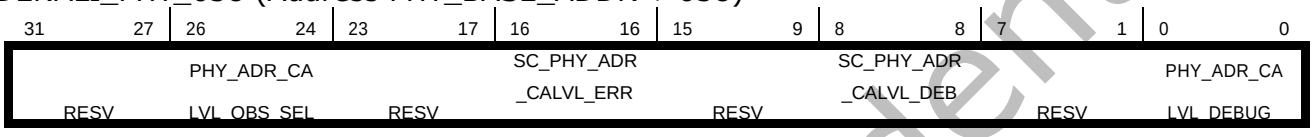
Name	Bits	Default	Range	Description
PHY_ADR_CALVL_DEVICE_MAP_1	27:24	0x0	0x0-0xf	Defines the CA training device map
PHY_ADR_CALVL_SWIZZLE1_1_1	23:0	0x000000	0x0-0xffffff	CA training RD DQ bit swizzlemap

DENALI_PHY_657 (Address PHY_BASE_ADDR + 657)



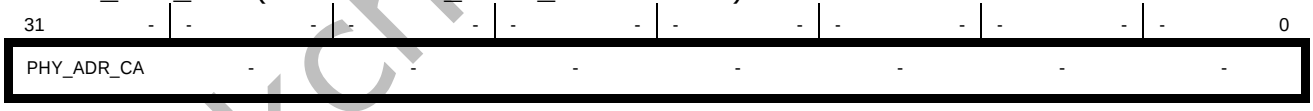
Name	Bits	Default	Range	Description
PHY_ADR_CALVL_RESP_WAIT_CNT_1	27:24	0x0	0x0-0xf	Number of samples to wait for response during CA training for
PHY_ADR_CALVL_CAPTURE_CNT_1	19:16	0x0	0x0-0xf	Number of samples to take at each ADDR slave delay setting during
PHY_ADR_CALVL_NUM_PATTERNS_1	9:8	0x0	0x0-0x3	Sets the number of patterns to use during CA training for address slice
PHY_ADR_CALVL_RANK_CTRL_1	1:0	0x0	0x0-0x3	Defines the CA training rank control

DENALI_PHY_658 (Address PHY_BASE_ADDR + 658)



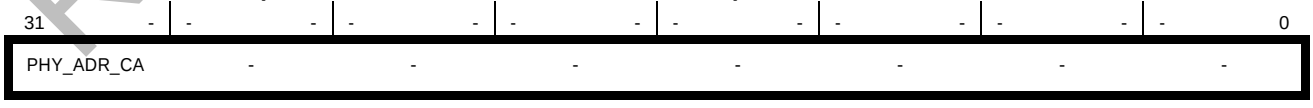
Name	Bits	Default	Range	Description
PHY_ADR_CALVL_OBS_SELECT_1	26:24	0x0	0x0-0x7	CA bit lane to observe result from (OBS0 and OBS1) during CA
SC_PHY_ADR_CALVL_ERROR_CLR_1	16	0x0	0x0-0x1	Clears the CA training state machine error status for address
SC_PHY_ADR_CALVL_DEBUG_CONT_1	8	0x0	0x0-0x1	Allows the CA training state machine to advance (when in
PHY_ADR_CALVL_DEBUG_MODE_1	0	0x0	0x0-0x1	Enables CA training debug mode for address slice 1. Set to 1 to

DENALI_PHY_659 (Address PHY_BASE_ADDR + 659)



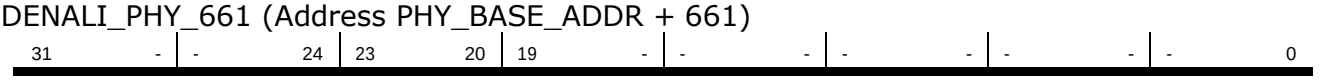
Name	Bits	Default	Range	Description
PHY_ADR_CALVL_OBS0_1	31:0	0x00000000	0x0-0xffffffff	Observation register for CA training

DENALI_PHY_660 (Address PHY_BASE_ADDR + 660)



Name	Bits	Default	Range	Description
PHY_ADR_CALVL_OBS1_1	31:0	0x00000000	0x0-0xffffffff	Observation register for CA training

DENALI_PHY_661 (Address PHY_BASE_ADDR + 661)



OBSOLETE	-	RESV	PHY_ADR_CA	-	-	-	-

Name	Bits	Default	Range	Description
PHY_ADR_CALVL_FG_0_1	19:0	0x00000	0x0-0xfffff	CA training foreground pattern 0 for

DENALI_PHY_662 (Address PHY_BASE_ADDR + 662)

31 - 24	23 20	19 - 0
OBSOLETE	RESV	PHY_ADR_CA

Name	Bits	Default	Range	Description
PHY_ADR_CALVL_BG_0_1	19:0	0x00000	0x0-0xfffff	CA training background pattern 0

DENALI_PHY_663 (Address PHY_BASE_ADDR + 663)

31 - 24	23 20	19 - 0
OBSOLETE	RESV	PHY_ADR_CA

Name	Bits	Default	Range	Description
PHY_ADR_CALVL_FG_1_1	19:0	0x00000	0x0-0xfffff	CA training foreground pattern 1 for

DENALI_PHY_664 (Address PHY_BASE_ADDR + 664)

31 - 24	23 20	19 - 0
OBSOLETE	RESV	PHY_ADR_CA

Name	Bits	Default	Range	Description
PHY_ADR_CALVL_BG_1_1	19:0	0x00000	0x0-0xfffff	CA training background pattern 1

DENALI_PHY_665 (Address PHY_BASE_ADDR + 665)

31 - 24	23 20	19 - 0
OBSOLETE	RESV	PHY_ADR_CA

Name	Bits	Default	Range	Description
PHY_ADR_CALVL_FG_2_1	19:0	0x00000	0x0-0xfffff	CA training foreground pattern 2 for

DENALI_PHY_666 (Address PHY_BASE_ADDR + 666)

31 - 24	23 20	19 - 0
OBSOLETE	RESV	PHY_ADR_CA

Name	Bits	Default	Range	Description
PHY_ADR_CALVL_BG_2_1	19:0	0x00000	0x0-0xfffff	CA training background pattern 2

DENALI_PHY_667 (Address PHY_BASE_ADDR + 667)

31 - 24	23 20	19 - 0
OBSOLETE	RESV	PHY_ADR_CA

Name	Bits	Default	Range	Description
PHY_ADR_CALVL_FG_3_1	19:0	0x00000	0x0-0xfffff	CA training foreground pattern 3 for

DENALI_PHY_668 (Address PHY_BASE_ADDR + 668)

31 - 24	23 20	19 - 0
OBSOLETE	RESV	PHY_ADR_CA

Name	Bits	Default	Range	Description
PHY_ADR_CALVL_BG_3_1	19:0	0x00000	0x0-0xfffff	CA training background pattern 3

DENALI_PHY_669 (Address PHY_BASE_ADDR + 669)

31 30	29 - 0
RESV	PHY_ADR_AD

Name	Bits	Default	Range	Description
PHY_ADR_ADDR_SEL_1	29:0	0x00000000	0x0-0x3fffffff	Mux select to map in LPDDR4

DENALI_PHY_670 (Address PHY_BASE_ADDR + 670)

31 30	29 24	23 22	21 16	15 10	9 - 0
RESV	PHY_ADR_SEG_MASK_1	RESV	PHY_ADR_BIT_MASK_1	RESV	PHY_ADR_LP4_BOOT_SLV_DELAY_1

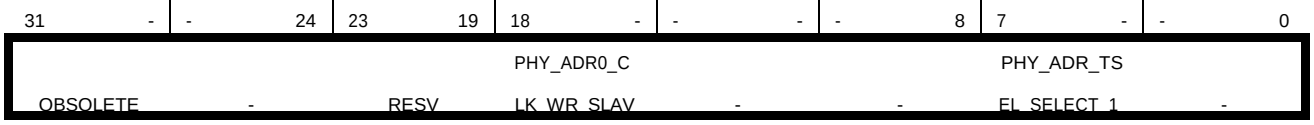
Name	Bits	Default	Range	Description
PHY_ADR_SEG_MASK_1	29:24	0x00	0x0-0x3f	Segment mask bit for address slice 1. Set to 1 to indicate that the bit is
PHY_ADR_BIT_MASK_1	21:16	0x00	0x0-0x3f	Mask bit for address slice 1. Set to 1 to indicate that the bit is masked
PHY_ADR_LP4_BOOT_SLV_DELAY_1	9:0	0x000	0x0-0x3ff	Address slave delay setting during the LPDDR4 boot frequency

DENALI_PHY_671 (Address PHY_BASE_ADDR + 671)

31 - 16	15 14	13 8	7 6	5 0
OBSOLETE	RESV	RESERVED	RESV	PHY_ADR_CALVL_TRAIN_M

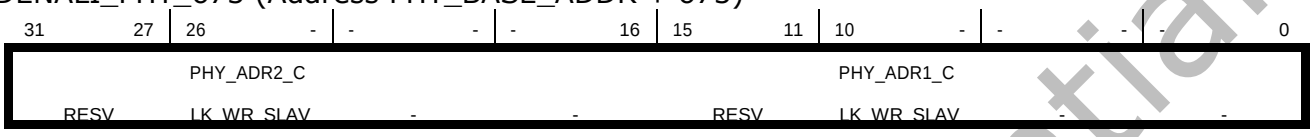
Name	Bits	Default	Range	Description
RESERVED	13:8	0x00	0x0-0x3f	Reserved for future use. Refer to the regconfig files for the default
PHY_ADR_CALVL_TRAIN_MASK_1	5:0	0x00	0x0-0x3f	Mask bit for CA training participation for address slice 1. Set

DENALI_PHY_672 (Address PHY_BASE_ADDR + 672)



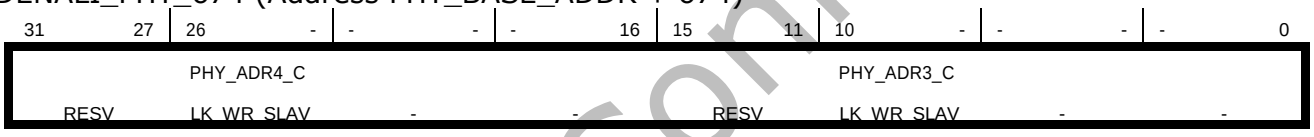
Name	Bits	Default	Range	Description
PHY_ADR0_CLK_WR_SLAVE_DELAY_1	18:8	0x000	0x0-0x7ff	Address slice slave delay setting
PHY_ADR_TSEL_SELECT_1	7:0	0x00	0x0-0xff	Tsel select values for address slice

DENALI_PHY_673 (Address PHY_BASE_ADDR + 673)



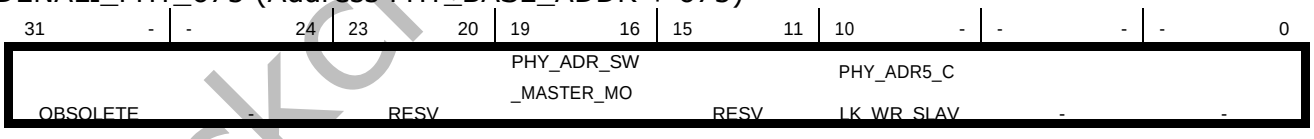
Name	Bits	Default	Range	Description
PHY_ADR2_CLK_WR_SLAVE_DELAY_1	26:16	0x000	0x0-0x7ff	Address slice slave delay setting
PHY_ADR1_CLK_WR_SLAVE_DELAY_1	10:0	0x000	0x0-0x7ff	Address slice slave delay setting

DENALI_PHY_674 (Address PHY_BASE_ADDR + 674)



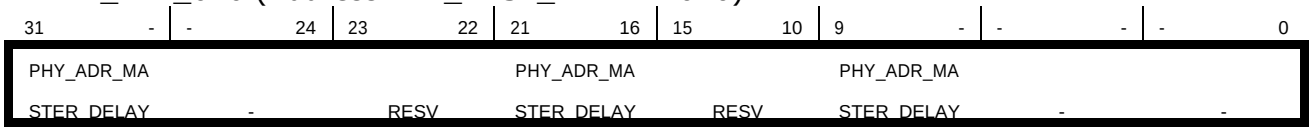
Name	Bits	Default	Range	Description
PHY_ADR4_CLK_WR_SLAVE_DELAY_1	26:16	0x000	0x0-0x7ff	Address slice slave delay setting
PHY_ADR3_CLK_WR_SLAVE_DELAY_1	10:0	0x000	0x0-0x7ff	Address slice slave delay setting

DENALI_PHY_675 (Address PHY_BASE_ADDR + 675)



Name	Bits	Default	Range	Description
PHY_ADR_SW_MASTER_MODE_1	19:16	0x0	0x0-0xf	Master delay line override settings for address slice 1. Bit (0) enables software half clock mode. Bit (1) is the software half clock mode value.
PHY_ADR5_CLK_WR_SLAVE_DELAY_1	10:0	0x000	0x0-0x7ff	Address slice slave delay setting

DENALI_PHY_676 (Address PHY_BASE_ADDR + 676)



Name	Bits	Default	Range	Description

PHY_ADR_MASTER_DELAY_WAIT_1	31:24	0x00	0x0-0xff	Wait cycles for master delay line locking algorithm for address slice 1. Bits (3:0) is the cycle wait count after a calibration clock setting
PHY_ADR_MASTER_DELAY_STEP_1	21:16	0x00	0x0-0x3f	Incremental step size for master delay line locking algorithm for
PHY_ADR_MASTER_DELAY_START_1	9:0	0x000	0x0-0x3ff	Start value for master delay line locking algorithm for address slice

DENALI_PHY_677 (Address PHY_BASE_ADDR + 677)

31 - 8	7 - 4	3 - 0
OBSOLETE	RESV	PHY_ADR_CALVL_DLY_STEP

Name	Bits	Default	Range	Description
PHY_ADR_CALVL_DLY_STEP_1	3:0	0x0	0x0-0xf	Sets the delay step size plus 1 during CA training for address slice

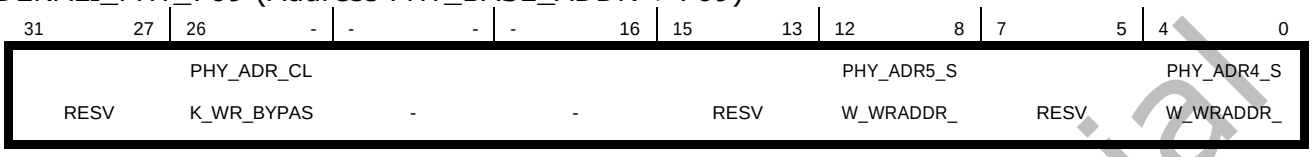
DENALI_PHY_768 (Address PHY_BASE_ADDR + 768)

31 - 29	28 - 24	23 - 21	20 - 16	15 - 13	12 - 8	7 - 5	4 - 0
RESV	PHY_ADR3_SW_WRADDR	RESV	PHY_ADR2_SW_WRADDR	RESV	PHY_ADR1_SW_WRADDR	RESV	PHY_ADR0_SW_WRADDR

Name	Bits	Default	Range	Description
PHY_ADR3_SW_WRADDR_SHIFT_2	28:24	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for address slice 2. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits
PHY_ADR2_SW_WRADDR_SHIFT_2	20:16	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for address slice 2. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits
PHY_ADR1_SW_WRADDR_SHIFT_2	12:8	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for address slice 2. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits

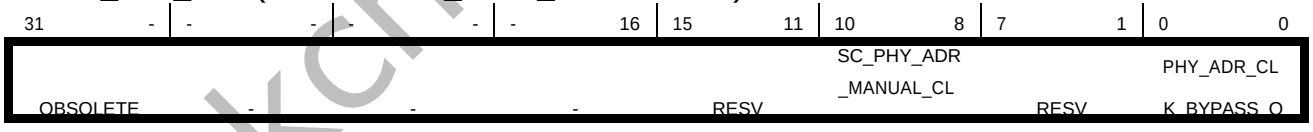
PHY_ADR0_SW_WRADDR_SHIFT_2	4:0	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for address slice 2. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits

DENALI_PHY_769 (Address PHY_BASE_ADDR + 769)



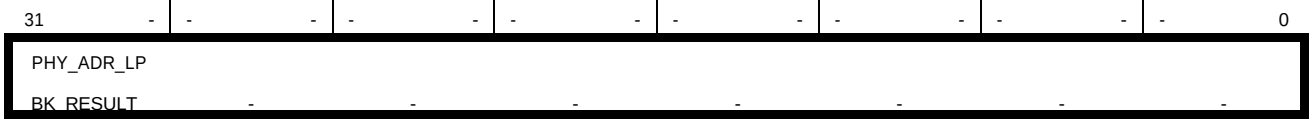
Name	Bits	Default	Range	Description
PHY_ADR_CLK_WR_BYPASS_SLAVE_DELAY_2	26:16	0x000	0x0-0x7ff	Write address clock bypass mode slave delay setting for address slice
PHY_ADR5_SW_WRADDR_SHIFT_2	12:8	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for address slice 2. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits
PHY_ADR4_SW_WRADDR_SHIFT_2	4:0	0x00	0x0-0x1f	Manual override of automatic half_cycle_shift/cycle_shift for address slice 2. Bit (0) enables override of half_cycle_shift. Bit (1) is the half_cycle_shift value. Bit (2) enables override of cycle shift. Bits

DENALI_PHY_770 (Address PHY_BASE_ADDR + 770)



Name	Bits	Default	Range	Description
SC_PHY_ADR_MANUAL_CLEAR_2	10:8	0x0	0x0-0x7	Manual reset/clear of internal logic for address slice 2. Bit (0) is reset of master delay min/max lock values. Bit (1) is manual reset of
PHY_ADR_CLK_BYPASS_OVERRIDE_2	0	0x0	0x0-0x1	Bypass mode override setting for

DENALI_PHY_771 (Address PHY_BASE_ADDR + 771)



Name	Bits	Default	Range	Description

PHY_ADR_LPBK_RESULT_OBS_2	31:0	0x00000000	0x0-0xffffffff	Observation register containing loopback status/results for address

DENALI_PHY_772 (Address PHY_BASE_ADDR + 772)

31 -	- 24	23 19	18 16	15 -	-	-	-	-	0
OBSOLETE	-	RESV	PHY_ADR_MASTER_DLY_L	PHY_ADR_LPBK_ERROR_C	-	-	-		

Name	Bits	Default	Range	Description
PHY_ADR_MASTER_DLY_LOCK_OBS_SELECT_2	18:16	0x0	0x0-0x7	Select value to map the internal master delay observation registers to the accessible master delay
PHY_ADR_LPBK_ERROR_COUNT_OBS_2	15:0	0x0000	0x0-0xffff	Observation register containing total number of loopback error data

DENALI_PHY_773 (Address PHY_BASE_ADDR + 773)

31 27	26 24	23 19	18 16	15 10	9 -	-	-	-	0
RESV	PHY_ADR_SLV_DLY_ENC_	RESV	PHY_ADR_SLAVE_LOOP_C	RESV	PHY_ADR_MASTER_DLY_L	-	-		

Name	Bits	Default	Range	Description
PHY_ADR_SLV_DLY_ENC_OBS_SELECT_	26:24	0x0	0x0-0x7	Select value to map the addr bits delay observation registers to the
PHY_ADR_SLAVE_LOOP_CNT_UPDATE_	18:16	0x0	0x0-0x7	Sets the frequency by which the slave delay encoded value holding
PHY_ADR_MASTER_DLY_LOCK_OBS_2	9:0	0x000	0x0-0x3ff	Observation register for master delay results for address slice 2.

DENALI_PHY_774 (Address PHY_BASE_ADDR + 774)

31 25	24 24	23 22	21 16	15 9	8 8	7 1	0 0
RESV	PHY_ADR_PWR_RDC_DISA	RESV	PHY_ADR_LPBK_CONTROL	RESV	PHY_ADR_TSEL_ENABLE_2	RESV	SC_PHY_ADR_SNAP_OBS_

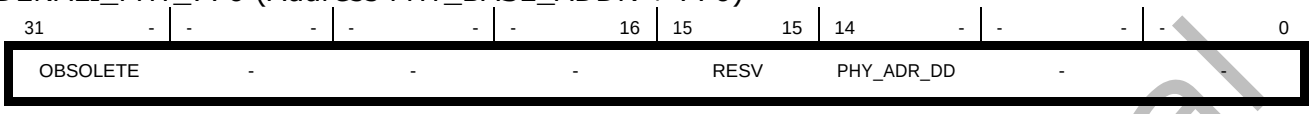
Name	Bits	Default	Range	Description
PHY_ADR_PWR_RDC_DISABLE_2	24	0x0	0x0-0x1	adr slice power reduction disable
PHY_ADR_LPBK_CONTROL_2	21:16	0x00	0x0-0x3f	Loopback control bits for address
PHY_ADR_TSEL_ENABLE_2	8	0x0	0x0-0x1	Enables tsel_en for address slice 2.
SC_PHY_ADR_SNAP_OBS_REGS_2	0	0x0	0x0-0x1	Initiates a snapshot of the internal observation registers for address

DENALI_PHY_775 (Address PHY_BASE_ADDR + 775)

31 -	- 24	23 17	16 16	15 11	10 8	7 2	1 0
OBSOLETE	-	RESV	PHY_ADR_IE_MODE_2	RESV	PHY_ADR_WR_ADDR_SHIFT	RESV	PHY_ADR_TYPE_2

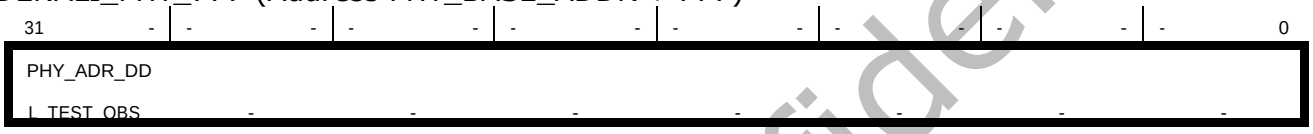
Name	Bits	Default	Range	Description
PHY_ADR_IE_MODE_2	16	0x0	0x0-0x1	Input enable control for address
PHY_ADR_WRADDR_SHIFT_OBS_2	10:8	0x0	0x0-0x7	Observation register for automatic half cycle and cycle shift values for
PHY_ADR_TYPE_2	1:0	0x0	0x0-0x3	DRAM type for address slice 2.

DENALI_PHY_776 (Address PHY_BASE_ADDR + 776)



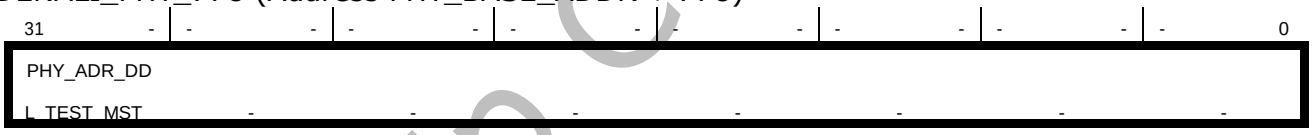
Name	Bits	Default	Range	Description
PHY_ADR_DDL_MODE_2	14:0	0x0000	0x0-0x7fff	DDL mode for address slice 2.

DENALI_PHY_777 (Address PHY_BASE_ADDR + 777)



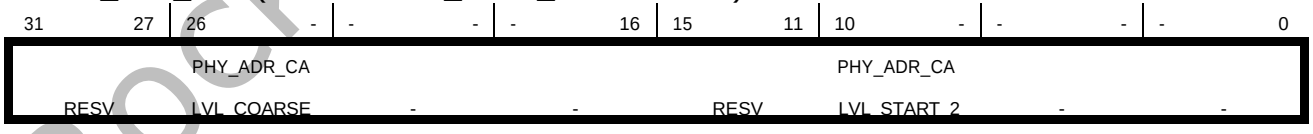
Name	Bits	Default	Range	Description
PHY_ADR_DDL_TEST_OBS_2	31:0	0x00000000	0x0-0xffffffff	DDL test observation for address

DENALI_PHY_778 (Address PHY_BASE_ADDR + 778)



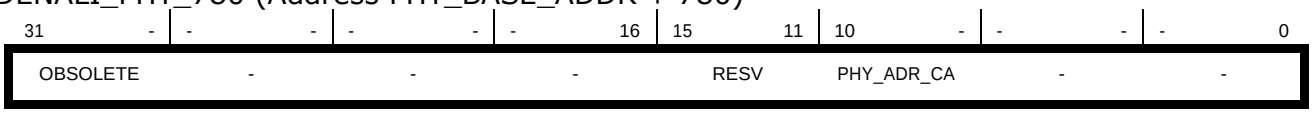
Name	Bits	Default	Range	Description
PHY_ADR_DDL_TEST_MSTR_DLY_OBS_2	31:0	0x00000000	0x0-0xffffffff	DDL test observation delays for address slice 2 master DDL.

DENALI_PHY_779 (Address PHY_BASE_ADDR + 779)



Name	Bits	Default	Range	Description
PHY_ADR_CALVL_COARSE_DLY_2	26:16	0x000	0x0-0x7ff	Coarse CA training DLL increment
PHY_ADR_CALVL_START_2	10:0	0x000	0x0-0x7ff	CA training DLL start value for

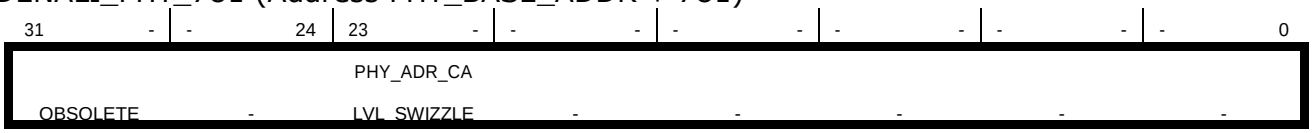
DENALI_PHY_780 (Address PHY_BASE_ADDR + 780)



Name	Bits	Default	Range	Description

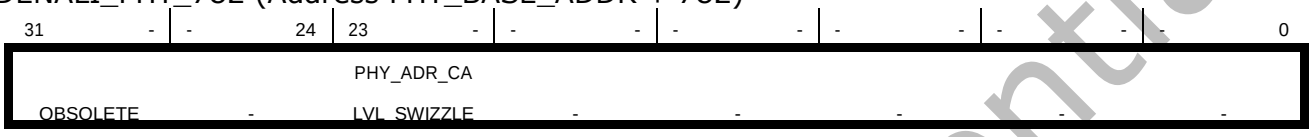
PHY_ADR_CALVL_QTR_2	10:0	0x000	0x0-0x7ff	CA training DLL quarter cycle delay

DENALI_PHY_781 (Address PHY_BASE_ADDR + 781)



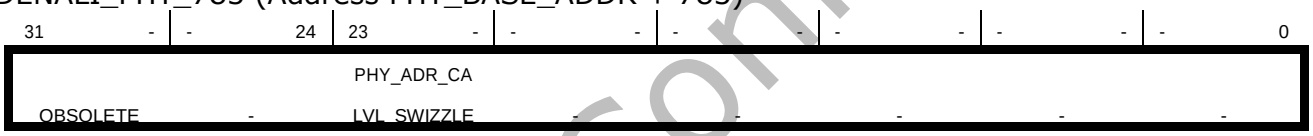
Name	Bits	Default	Range	Description
PHY_ADR_CALVL_SWIZZLE0_0_2	23:0	0x000000	0x0-0xffffff	CA training RD DQ bit swizzle map

DENALI_PHY_782 (Address PHY_BASE_ADDR + 782)



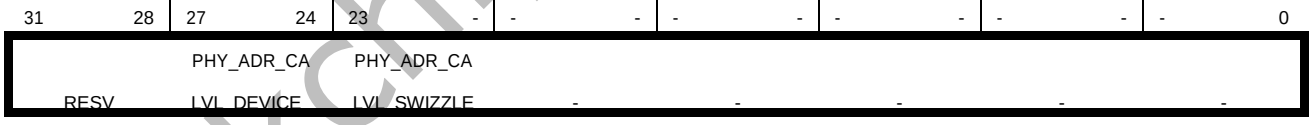
Name	Bits	Default	Range	Description
PHY_ADR_CALVL_SWIZZLE1_0_2	23:0	0x000000	0x0-0xffffff	CA training RD DQ bit swizzle map

DENALI_PHY_783 (Address PHY_BASE_ADDR + 783)



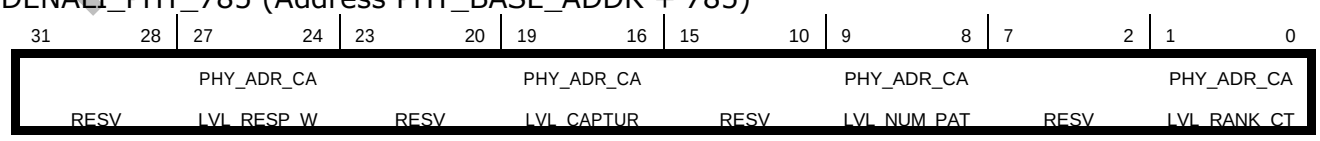
Name	Bits	Default	Range	Description
PHY_ADR_CALVL_SWIZZLE0_1_2	23:0	0x000000	0x0-0xffffff	CA training RD DQ bit swizzle map

DENALI_PHY_784 (Address PHY_BASE_ADDR + 784)



Name	Bits	Default	Range	Description
PHY_ADR_CALVL_DEVICE_MAP_2	27:24	0x0	0x0-0xf	Defines the CA training device map
PHY_ADR_CALVL_SWIZZLE1_1_2	23:0	0x000000	0x0-0xffffff	CA training RD DQ bit swizzle map

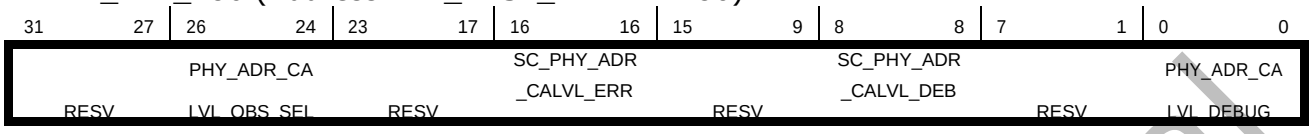
DENALI_PHY_785 (Address PHY_BASE_ADDR + 785)



Name	Bits	Default	Range	Description
PHY_ADR_CALVL_RESP_WAIT_CNT_2	27:24	0x0	0x0-0xf	Number of samples to wait for response during CA training for

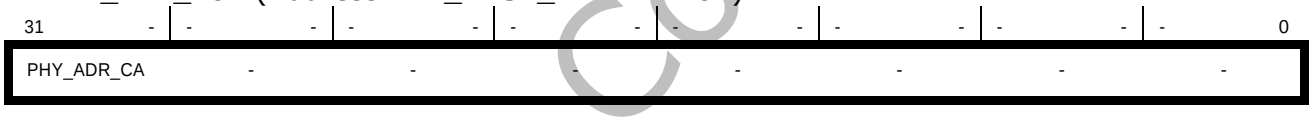
PHY_ADR_CALVL_CAPTURE_CNT_2	19:16	0x0	0x0-0xf	Number of samples to take at each ADDR slave delay setting during
PHY_ADR_CALVL_NUM_PATTERNS_2	9:8	0x0	0x0-0x3	Sets the number of patterns to use during CA training for address slice
PHY_ADR_CALVL_RANK_CTRL_2	1:0	0x0	0x0-0x3	Defines the CA training rank control

DENALI_PHY_786 (Address PHY_BASE_ADDR + 786)



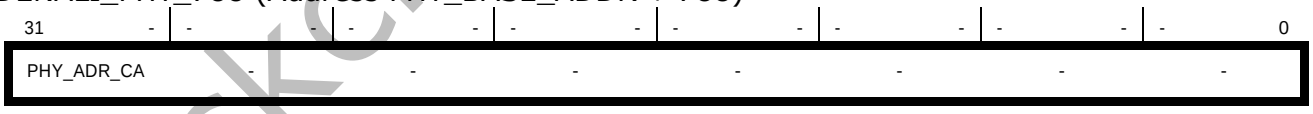
Name	Bits	Default	Range	Description
PHY_ADR_CALVL_OBS_SELECT_2	26:24	0x0	0x0-0x7	CA bit lane to observe result from (OBS0 and OBS1) during CA
SC_PHY_ADR_CALVL_ERROR_CLR_2	16	0x0	0x0-0x1	Clears the CA training state machine error status for address
SC_PHY_ADR_CALVL_DEBUG_CONT_2	8	0x0	0x0-0x1	Allows the CA training state machine to advance (when in
PHY_ADR_CALVL_DEBUG_MODE_2	0	0x0	0x0-0x1	Enables CA training debug mode for address slice 2. Set to 1 to

DENALI_PHY_787 (Address PHY_BASE_ADDR + 787)



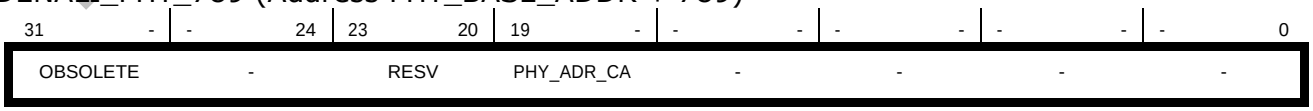
Name	Bits	Default	Range	Description
PHY_ADR_CALVL_OBS0_2	31:0	0x00000000	0x0-0xffffffff	Observation register for CA training

DENALI_PHY_788 (Address PHY_BASE_ADDR + 788)



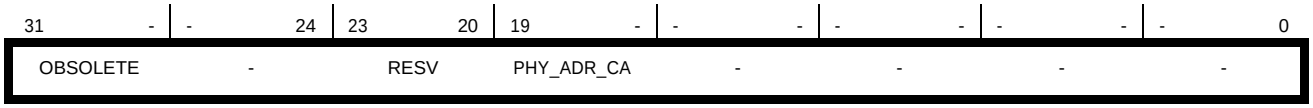
Name	Bits	Default	Range	Description
PHY_ADR_CALVL_OBS1_2	31:0	0x00000000	0x0-0xffffffff	Observation register for CA training

DENALI_PHY_789 (Address PHY_BASE_ADDR + 789)



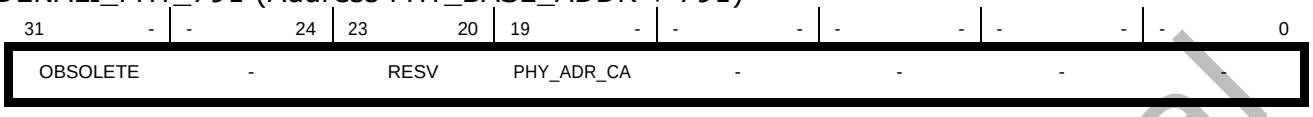
Name	Bits	Default	Range	Description
PHY_ADR_CALVL_FG_0_2	19:0	0x00000	0x0-0xfffff	CA training foreground pattern 0 for

DENALI_PHY_790 (Address PHY_BASE_ADDR + 790)



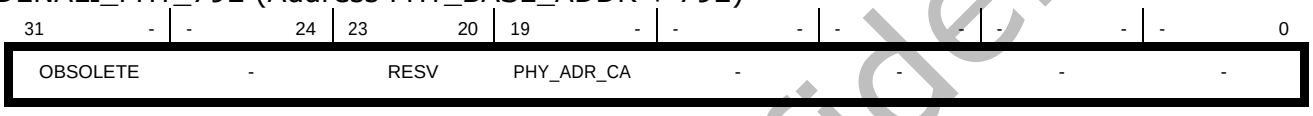
Name	Bits	Default	Range	Description
PHY_ADR_CALVL_BG_0_2	19:0	0x00000	0x0-0xfffff	CA training background pattern 0

DENALI_PHY_791 (Address PHY_BASE_ADDR + 791)



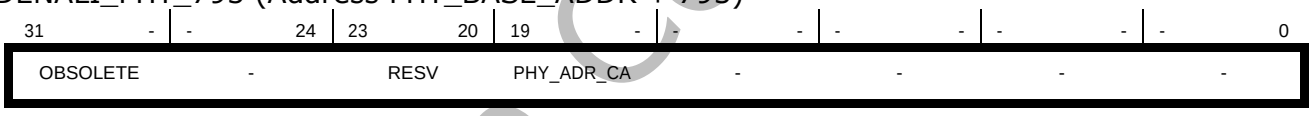
Name	Bits	Default	Range	Description
PHY_ADR_CALVL_FG_1_2	19:0	0x00000	0x0-0xfffff	CA training foreground pattern 1 for

DENALI_PHY_792 (Address PHY_BASE_ADDR + 792)



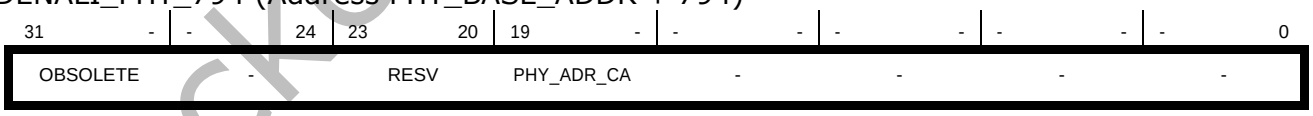
Name	Bits	Default	Range	Description
PHY_ADR_CALVL_BG_1_2	19:0	0x00000	0x0-0xfffff	CA training background pattern 1

DENALI_PHY_793 (Address PHY_BASE_ADDR + 793)



Name	Bits	Default	Range	Description
PHY_ADR_CALVL_FG_2_2	19:0	0x00000	0x0-0xfffff	CA training foreground pattern 2 for

DENALI_PHY_794 (Address PHY_BASE_ADDR + 794)

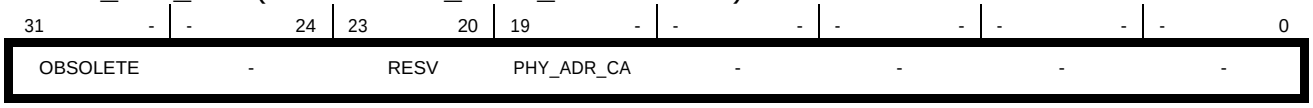


Name	Bits	Default	Range	Description
PHY_ADR_CALVL_BG_2_2	19:0	0x00000	0x0-0xfffff	CA training background pattern 2

DENALI_PHY_795 (Address PHY_BASE_ADDR + 795)

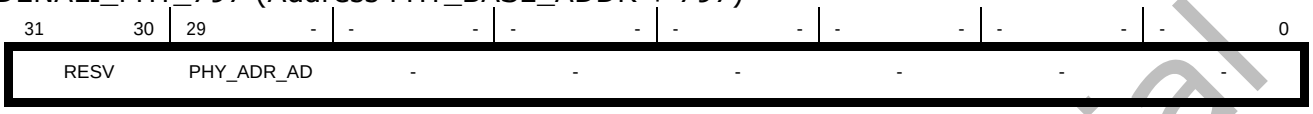
Name	Bits	Default	Range	Description
PHY_ADR_CALVL_FG_3_2	19:0	0x00000	0x0-0xfffff	CA training foreground pattern 3 for

DENALI_PHY_796 (Address PHY_BASE_ADDR + 796)



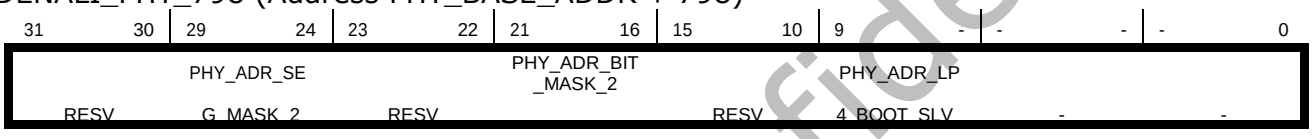
Name	Bits	Default	Range	Description
PHY_ADR_CALVL_BG_3_2	19:0	0x00000	0x0-0xfffff	CA training background pattern 3

DENALI_PHY_797 (Address PHY_BASE_ADDR + 797)



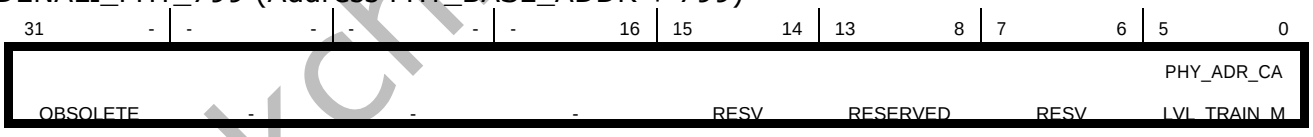
Name	Bits	Default	Range	Description
PHY_ADR_ADDR_SEL_2	29:0	0x00000000	0x0-0x3fffffff	Mux select to map in LPDDR4

DENALI_PHY_798 (Address PHY_BASE_ADDR + 798)



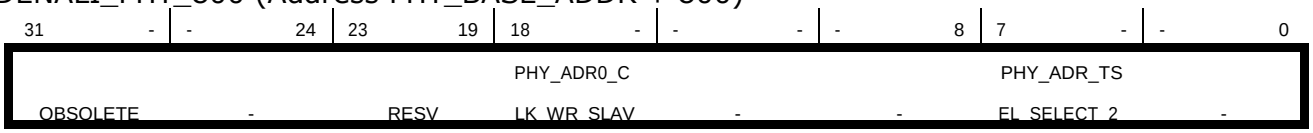
Name	Bits	Default	Range	Description
PHY_ADR_SEG_MASK_2	29:24	0x00	0x0-0x3f	Segment mask bit for address slice 2. Set to 1 to indicate that the bit is
PHY_ADR_BIT_MASK_2	21:16	0x00	0x0-0x3f	Mask bit for address slice 2. Set to 1 to indicate that the bit is masked
PHY_ADR_LP4_BOOT_SLV_DELAY_2	9:0	0x000	0x0-0x3ff	Address slave delay setting during the LPDDR4 boot frequency

DENALI_PHY_799 (Address PHY_BASE_ADDR + 799)



Name	Bits	Default	Range	Description
RESERVED	13:8	0x00	0x0-0x3f	Reserved for future use. Refer to the regconfig files for the default
PHY_ADR_CALVL_TRAIN_MASK_2	5:0	0x00	0x0-0x3f	Mask bit for CA training participation for address slice 2.

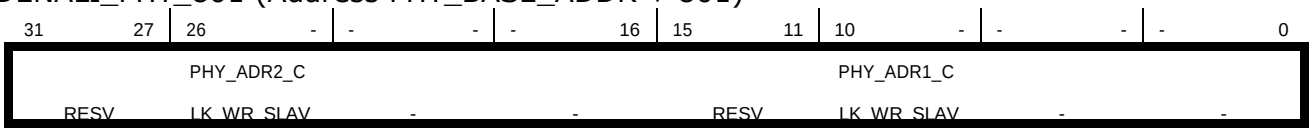
DENALI_PHY_800 (Address PHY_BASE_ADDR + 800)



Name	Bits	Default	Range	Description
PHY_ADR0_CLK_WR_SLAVE_DELAY_2	18:8	0x000	0x0-0x7ff	Address slice slave delay setting

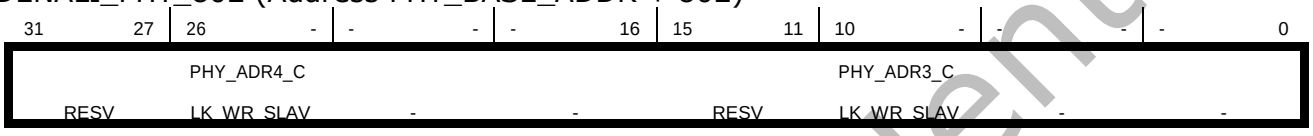
PHY_ADR_TSEL_SELECT_2	7:0	0x00	0x0-0xff	Tsel select values for address slice

DENALI_PHY_801 (Address PHY_BASE_ADDR + 801)



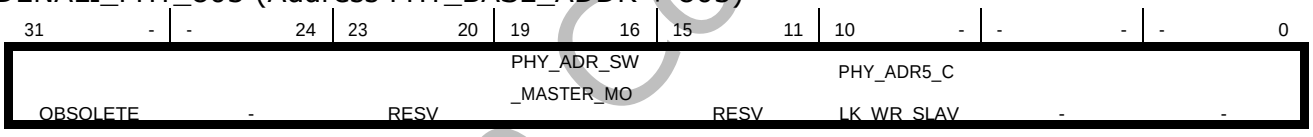
Name	Bits	Default	Range	Description
PHY_ADR2_CLK_WR_SLAVE_DELAY_2	26:16	0x000	0x0-0x7ff	Address slice slave delay setting
PHY_ADR1_CLK_WR_SLAVE_DELAY_2	10:0	0x000	0x0-0x7ff	Address slice slave delay setting

DENALI_PHY_802 (Address PHY_BASE_ADDR + 802)



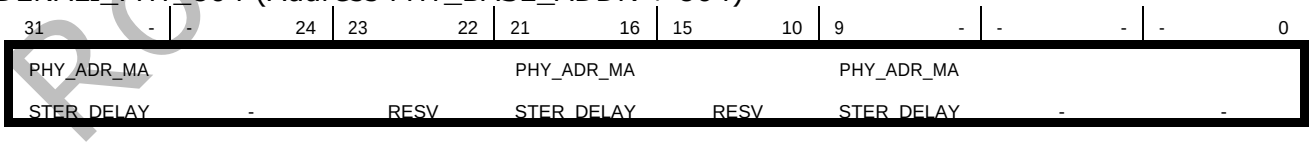
Name	Bits	Default	Range	Description
PHY_ADR4_CLK_WR_SLAVE_DELAY_2	26:16	0x000	0x0-0x7ff	Address slice slave delay setting
PHY_ADR3_CLK_WR_SLAVE_DELAY_2	10:0	0x000	0x0-0x7ff	Address slice slave delay setting

DENALI_PHY_803 (Address PHY_BASE_ADDR + 803)



Name	Bits	Default	Range	Description
PHY_ADR_SW_MASTER_MODE_2	19:16	0x0	0x0-0xf	Master delay line override settings for address slice 2. Bit (0) enables software half clock mode. Bit (1) is the software half clock mode value.
PHY_ADR5_CLK_WR_SLAVE_DELAY_2	10:0	0x000	0x0-0x7ff	Address slice slave delay setting

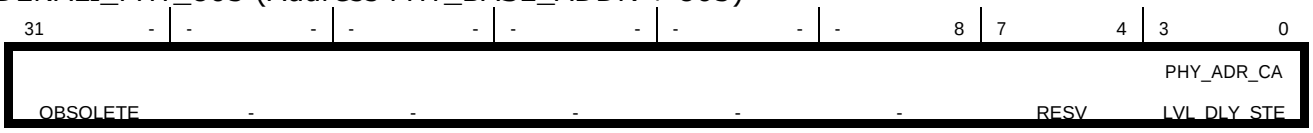
DENALI_PHY_804 (Address PHY_BASE_ADDR + 804)



Name	Bits	Default	Range	Description
PHY_ADR_MASTER_DELAY_WAIT_2	31:24	0x00	0x0-0xff	Wait cycles for master delay line locking algorithm for address slice 2. Bits (3:0) is the cycle wait count after a calibration clock setting
PHY_ADR_MASTER_DELAY_STEP_2	21:16	0x00	0x0-0x3f	Incremental step size for master delay line locking algorithm for

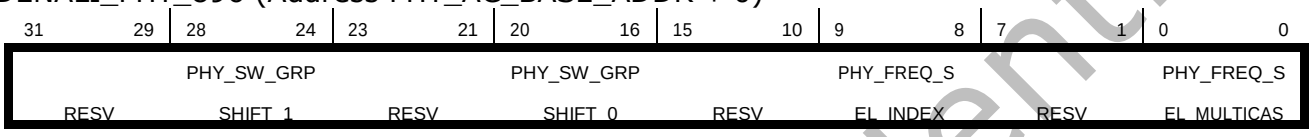
PHY_ADR_MASTER_DELAY_START_2	9:0	0x000	0x0-0x3ff	Start value for master delay line locking algorithm for address slice

DENALI_PHY_805 (Address PHY_BASE_ADDR + 805)



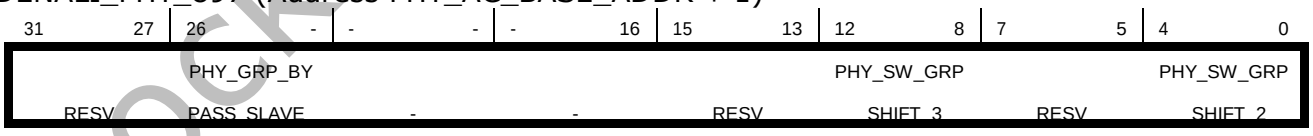
Name	Bits	Default	Range	Description
PHY_ADR_CALVL_DLY_STEP_2	3:0	0x0	0x0-0xf	Sets the delay step size plus 1 during CA training for address slice

DENALI_PHY_896 (Address PHY_AC_BASE_ADDR + 0)



Name	Bits	Default	Range	Description
PHY_SW_GRP_SHIFT_1	28:24	0x00	0x0-0x1f	Address/control group slice 1 manual override of automatic half_cycle_shift/cycle_shift. Bit (0) enables override of
PHY_SW_GRP_SHIFT_0	20:16	0x00	0x0-0x1f	Address/control group slice 0 manual override of automatic half_cycle_shift/cycle_shift. Bit (0) enables override of
PHY_FREQ_SEL_INDEX	9:8	0x0	0x0-0x3	Selects which frequency set to
PHY_FREQ_SEL_MULTICAST_EN	0	0x1	0x0-0x1	When set, a register write will update parameters for all frequency

DENALI_PHY_897 (Address PHY_AC_BASE_ADDR + 1)



Name	Bits	Default	Range	Description
PHY_GRP_BYPASS_SLAVE_DELAY	26:16	0x000	0x0-0x7ff	Address/control group slice bypass
PHY_SW_GRP_SHIFT_3	12:8	0x00	0x0-0x1f	Address/control group slice 3 manual override of automatic half_cycle_shift/cycle_shift. Bit (0) enables override of

PHY_SW_GRP_SHIFT_2	4:0	0x00	0x0-0x1f	Address/control group slice 2 manual override of automatic half_cycle_shift/cycle_shift. Bit (0) enables override of

DENALI_PHY_898 (Address PHY_AC_BASE_ADDR + 2)

31 25	24 24	23 17	16 16	15 9	8 8	7 5	4 0
RESV	PHY_LP4_BOOT_DISABLE	RESV	SC_PHY_MANUAL_UPDATE	RESV	PHY_GRP_BYPASS_OVERRIDE	RESV	PHY_SW_GRP_BYPASS_SHI

Name	Bits	Default	Range	Description
PHY_LP4_BOOT_DISABLE	24	0x0	0x0-0x1	Controls the handling of the DFI frequency. When set to 1, DFI frequency 0 is considered the first operational frequency. When cleared to 0, DFI frequency 0 is the
SC_PHY_MANUAL_UPDATE	16	0x0	0x0-0x1	Manual update of all slave delay line settings. Set to 1 to trigger.
PHY_GRP_BYPASS_OVERRIDE	8	0x0	0x0-0x1	Address/control group slice bypass
PHY_SW_GRP_BYPASS_SHIFT	4:0	0x00	0x0-0x1f	Address/control group slice bypass

DENALI_PHY_899 (Address PHY_AC_BASE_ADDR + 3)

31 27	26 -	- -	- 16	15 12	11 8	7 1	0 0
RESV	PHY_CSLVL_S	-	-	RESV	PHY_CSLVL_	RESV	PHY_CSLVL_E

Name	Bits	Default	Range	Description
PHY_CSLVL_START	26:16	0x000	0x0-0x7ff	Defines the CS training DLL start
PHY_CSLVL_CS_MAP	11:8	0x0	0x0-0xf	CS training map. Set each CS bit to 1 to allow that CS to participate in
PHY_CSLVL_ENABLE	0	0x0	0x0-0x1	CS training enable. Set to 1 to enable CS training during CA

DENALI_PHY_900 (Address PHY_AC_BASE_ADDR + 4)

31 -	- 24	23 20	19 16	15 11	10 -	- -	- 0
OBSOLETE	-	RESV	PHY_CSLVL_CAPTURE_CN	RESV	PHY_CSLVL_QTR	-	-

Name	Bits	Default	Range	Description
PHY_CSLVL_CAPTURE_CNT	19:16	0x0	0x0-0xf	Defines the number of samples to take at each GRP slave delay
PHY_CSLVL_QTR	10:0	0x000	0x0-0x7ff	Defines the CS training DLL

DENALI_PHY_901 (Address PHY_AC_BASE_ADDR + 5)

31 25	24 24	23 20	19 16	15 11	10 -	- -	- 0

	PHY_CSLVL_		PHY_CSLVL_		PHY_CSLVL_		
RESV	DEBUG_MOD	RESV	COARSE_CAP	RESV	COARSE_DLY	-	-

Name	Bits	Default	Range	Description
PHY_CSLVL_DEBUG_MODE	24	0x0	0x0-0x1	Enables CS training debug mode.
PHY_CSLVL_COARSE_CAPTURE_CNT	19:16	0x0	0x0-0xf	Defines the number of samples to take at each GRP slave delay
PHY_CSLVL_COARSE_DLY	10:0	0x000	0x0-0x7ff	Defines the CS training DLL coarse

DENALI_PHY_902 (Address PHY_AC_BASE_ADDR + 6)

31	-	-	-	-	-	16	15	9	8	8	7	1	0	0
									SC_PHY_CSL				SC_PHY_CSL	
OBSOLETE	-	-	-		RESV				VL_ERROR_C		RESV		VL_DEBUG_C	

Name	Bits	Default	Range	Description
SC_PHY_CSLVL_ERROR_CLR	8	0x0	0x0-0x1	Clears the CS training state machine error status. Set to 1 to
SC_PHY_CSLVL_DEBUG_CONT	0	0x0	0x0-0x1	Allows the CS training state machine to advance (when in

DENALI_PHY_903 (Address PHY_AC_BASE_ADDR + 7)

31	-	-	-	-	-	-	-	-	-	-	-	-	-	0
PHY_CSLVL_		-		-		-		-		-		-		-

Name	Bits	Default	Range	Description
PHY_CSLVL_OBS0	31:0	0x00000000	0x0-0xffffffff	Observation register for CS

DENALI_PHY_904 (Address PHY_AC_BASE_ADDR + 8)

31	-	-	-	-	-	-	-	-	-	-	-	-	-	0
PHY_CSLVL_		-		-		-		-		-		-		-

Name	Bits	Default	Range	Description
PHY_CSLVL_OBS1	31:0	0x000000	0x0-0xffffffff	Observation register for CS

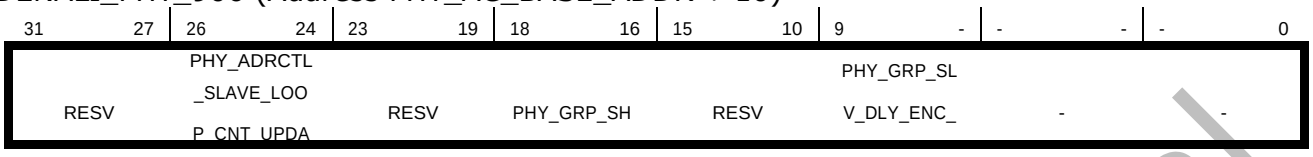
DENALI_PHY_905 (Address PHY_AC_BASE_ADDR + 9)

31	29	28	24	23	18	17	-	-	-	-	8	7	-	-	0
		PHY_GRP_SH				PHY_GRP_SL							PHY_CALVL_		
RESV		IFT_OBS_SEL		RESV		V_DLY_ENC			-		-		CS_MAP		-

Name	Bits	Default	Range	Description
PHY_GRP_SHIFT_OBS_SELECT	28:24	0x00	0x0-0x1f	Select value to map an individual address/control group slice

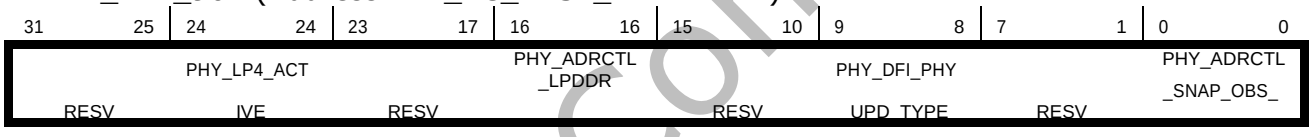
PHY_GRP_SLV_DLY_ENC_OBS_SELECT	17:8	0x000	0x0-0x3ff	Select value to map an individual address/control group slice slave
PHY_CALVL_CS_MAP	7:0	0x00	0x0-0xff	Defines the slice numbers associated with each CS during CA

DENALI_PHY_906 (Address PHY_AC_BASE_ADDR + 10)



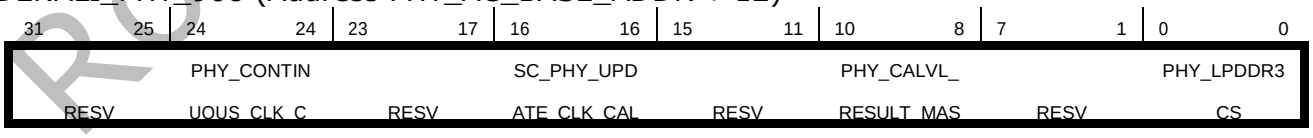
Name	Bits	Default	Range	Description
PHY_ADRCTL_SLAVE_LOOP_CNT_UPDA	26:24	0x0	0x0-0x7	Sets the frequency by which the slave delay encoded value holding
PHY_GRP_SHIFT_OBS	18:16	0x0	0x0-0x7	Observation register for the address/control group automatic
PHY_GRP_SLV_DLY_ENC_OBS	9:0	0x000	0x0-0x3ff	Observation register for all address/control group slice slave

DENALI_PHY_907 (Address PHY_AC_BASE_ADDR + 11)



Name	Bits	Default	Range	Description
PHY_LP4_ACTIVE	24	0x0	0x0-0x1	Indicates LPDDR4 device is
PHY_ADRCTL_LPDDR	16	0x0	0x0-0x1	Adds a cycle of delay for the address/control slices to match the
PHY_DFI_PHYUPD_TYPE	9:8	0x0	0x0-0x3	Defines the value of the dfi_phyupd_type output signal to
PHY_ADRCTL_SNAP_OBS_REGS	0	0x0	0x0-0x1	Initiates a snapshot of the internal observation registers for the

DENALI_PHY_908 (Address PHY_AC_BASE_ADDR + 12)



Name	Bits	Default	Range	Description
PHY_CONTINUOUS_CLK_CAL_UPDATE	24	0x0	0x0-0x1	Continuous update of all latest PVTP,PVTN and PVTR values to
SC_PHY_UPDATE_CLK_CAL_VALUES	16	0x0	0x0-0x1	Manual update of all latest PVTP,PVTN and PVTR values to

PHY_CALVL_RESULT_MASK	10:8	0x0	0x0-0x7	Mask bits to ignore ADR slice CA training results from the address slices. Bit (0) correlates to address
PHY_LPDDR3_CS	0	0x1	0x0-0x1	Alters reset state polarity for

DENALI_PHY_909 (Address PHY_AC_BASE_ADDR + 13)

31 28	27 24	23 20	19 16	15 12	11 8	7 4	3 0
RESV	RESERVED	RESV	RESERVED	RESV	RESERVED	RESV	RESERVED

Name	Bits	Default	Range	Description
RESERVED	27:24	0x0	0x0-0xf	Reserved for future use. Refer to the regconfig files for the default
RESERVED	19:16	0x0	0x0-0xf	Reserved for future use. Refer to the regconfig files for the default
RESERVED	11:8	0x0	0x0-0xf	Reserved for future use. Refer to the regconfig files for the default
RESERVED	3:0	0x0	0x0-0xf	Reserved for future use. Refer to the regconfig files for the default

DENALI_PHY_910 (Address PHY_AC_BASE_ADDR + 14)

31 -	- -	- -	- 16	15 -	- 8	7 1	0 0
OBSOLETE	-	-	-	PHY_PLL_WAI	-	RESV	RESERVED

Name	Bits	Default	Range	Description
PHY_PLL_WAIT	15:8	0x00	0x0-0xff	PHY clock PLL wait time after
RESERVED	0	0x0	0x0-0x1	Reserved for future use. Refer to the regconfig files for the default

DENALI_PHY_911 (Address PHY_AC_BASE_ADDR + 15)

31 29	28 -	- -	- 16	15 13	12 -	- -	- 0
RESV	PHY_PLL_CT	-	-	RESV	PHY_PLL_CT	-	-

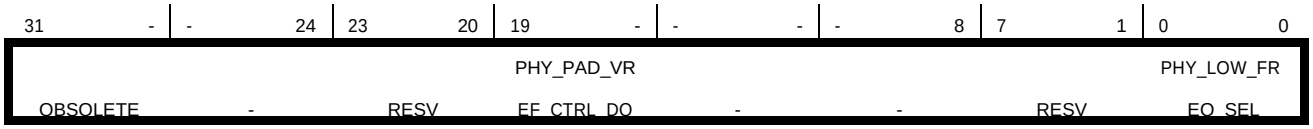
Name	Bits	Default	Range	Description
PHY_PLL_CTRL_CA	28:16	0x0000	0x0-0x1fff	PHY clock PLL controls for CA 2x
PHY_PLL_CTRL	12:0	0x0000	0x0-0x1fff	PHY clock PLL controls.

DENALI_PHY_912 (Address PHY_AC_BASE_ADDR + 16)

31 -	- -	- -	- -	- -	- 8	7 4	3 0
OBSOLETE	-	-	-	-	-	RESV	PHY_PLL_BYP

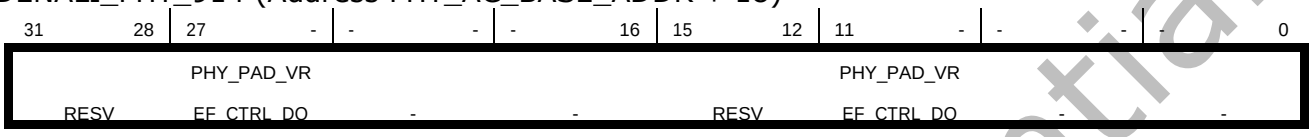
Name	Bits	Default	Range	Description
PHY_PLL_BYPASS	3:0	0x0	0x0-0xf	PHY clock PLL bypass select.

DENALI_PHY_913 (Address PHY_AC_BASE_ADDR + 17)



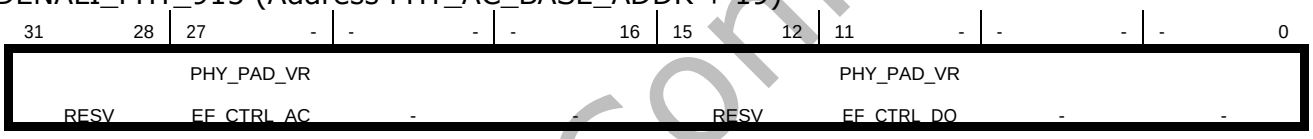
Name	Bits	Default	Range	Description
PHY_PAD_VREF_CTRL_DQ_0	19:8	0x000	0x0-0xfff	Pad VREF control settings for DQ
PHY_LOW_FREQ_SEL	0	0x0	0x0-0x1	Enables the PHY to enter/exit the PLL domain from the negative

DENALI_PHY_914 (Address PHY_AC_BASE_ADDR + 18)



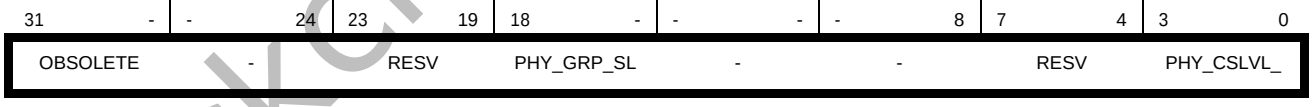
Name	Bits	Default	Range	Description
PHY_PAD_VREF_CTRL_DQ_2	27:16	0x000	0x0-0xfff	Pad VREF control settings for DQ
PHY_PAD_VREF_CTRL_DQ_1	11:0	0x000	0x0-0xfff	Pad VREF control settings for DQ

DENALI_PHY_915 (Address PHY_AC_BASE_ADDR + 19)



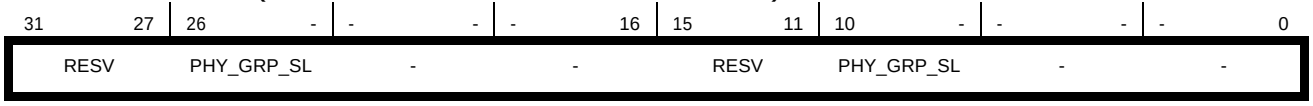
Name	Bits	Default	Range	Description
PHY_PAD_VREF_CTRL_AC	27:16	0x000	0x0-0xfff	Pad VREF control settings for the
PHY_PAD_VREF_CTRL_DQ_3	11:0	0x000	0x0-0xfff	Pad VREF control settings for DQ

DENALI_PHY_916 (Address PHY_AC_BASE_ADDR + 20)



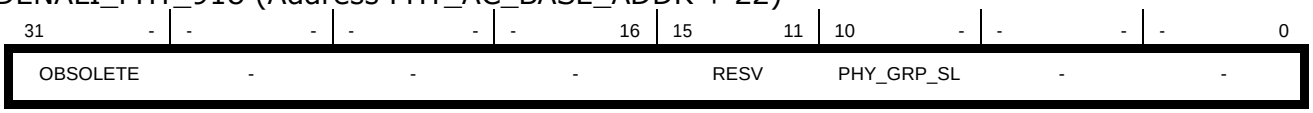
Name	Bits	Default	Range	Description
PHY_GRP_SLAVE_DELAY_0	18:8	0x000	0x0-0x7ff	Address/control group slice 0 slave
PHY_CSLVL_DLY_STEP	3:0	0x0	0x0-0xf	Sets the delay step size plus 1

DENALI_PHY_917 (Address PHY_AC_BASE_ADDR + 21)



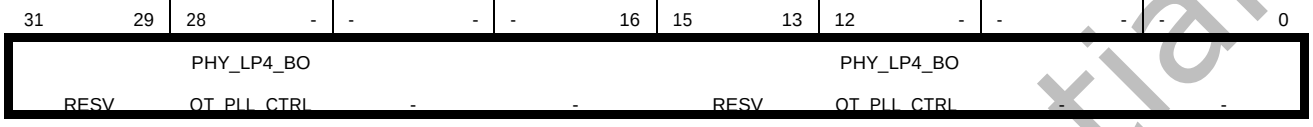
Name	Bits	Default	Range	Description
PHY_GRP_SLAVE_DELAY_2	26:16	0x000	0x0-0x7ff	Address/control group slice 2 slave
PHY_GRP_SLAVE_DELAY_1	10:0	0x000	0x0-0x7ff	Address/control group slice 1 slave

DENALI_PHY_918 (Address PHY_AC_BASE_ADDR + 22)



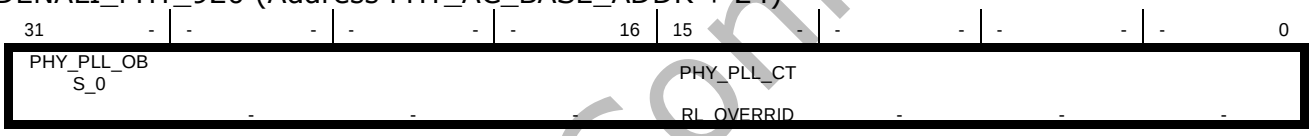
Name	Bits	Default	Range	Description
PHY_GRP_SLAVE_DELAY_3	10:0	0x000	0x0-0x7ff	Address/control group slice 3 slave

DENALI_PHY_919 (Address PHY_AC_BASE_ADDR + 23)



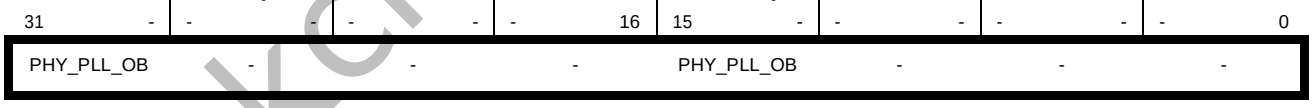
Name	Bits	Default	Range	Description
PHY_LP4_BOOT_PLL_CTRL_CA	28:16	0x0000	0x0-0x1fff	PHY deskew PLL controls for LPDDR4 boot frequency for 2X ca
PHY_LP4_BOOT_PLL_CTRL	12:0	0x0000	0x0-0x1fff	PHY deskew PLL controls for

DENALI_PHY_920 (Address PHY_AC_BASE_ADDR + 24)



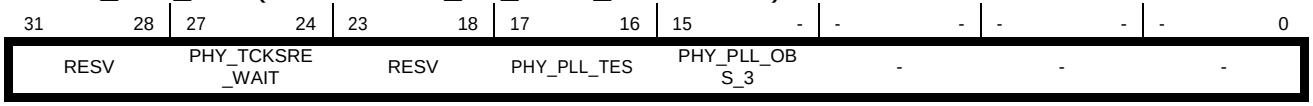
Name	Bits	Default	Range	Description
PHY_PLL_OBS_0	31:16	0x0000	0x0-0xffff	PHY clock PLL_0 observe values.
PHY_PLL_CTRL_OVERRIDE	15:0	0x0000	0x0-0xffff	Individual PHY clock PLL control

DENALI_PHY_921 (Address PHY_AC_BASE_ADDR + 25)



Name	Bits	Default	Range	Description
PHY_PLL_OBS_2	31:16	0x0000	0x0-0xffff	PHY clock PLL_2 observe values.
PHY_PLL_OBS_1	15:0	0x0000	0x0-0xffff	PHY clock PLL_1 observe values.

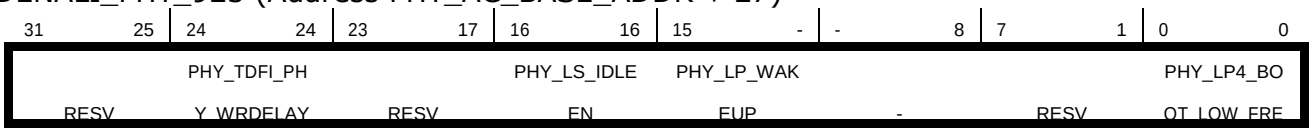
DENALI_PHY_922 (Address PHY_AC_BASE_ADDR + 26)



Name	Bits	Default	Range	Description
PHY_TCKSRE_WAIT	27:24	0x0	0x0-0xf	Specifies the number of cycles the PHY should wait before turning off
PHY_PLL_TESTOUT_SEL	17:16	0x0	0x0-0x3	PHY PLL testout select.

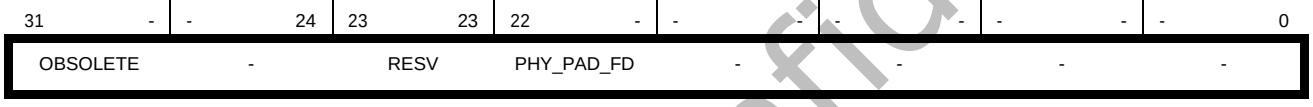
PHY_PLL_OBS_3	15:0	0x0000	0x0-0xffff	PHY TOP level clock PLL_3

DENALI_PHY_923 (Address PHY_AC_BASE_ADDR + 27)



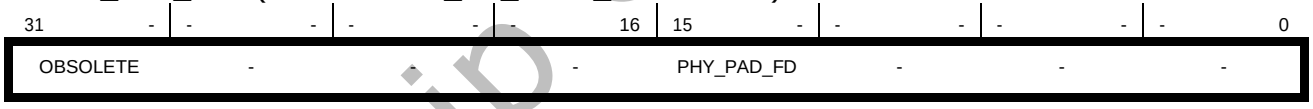
Name	Bits	Default	Range	Description
PHY_TDFI_PHY_WRDELAY	24	0x0	0x0-0x1	DFI timing parameter
PHY_LS_IDLE_EN	16	0x0	0x0-0x1	Indicates the Reduced Idle Power State is enabled in low power
PHY_LP_WAKEUP	15:8	0x00	0x0-0xff	Specifies the number of cycles the PHY takes to wakeup in low power
PHY_LP4_BOOT_LOW_FREQ_SEL	0	0x0	0x0-0x1	Control the PLL domain enter/exit from the negative clock edge for

DENALI_PHY_924 (Address PHY_AC_BASE_ADDR + 28)



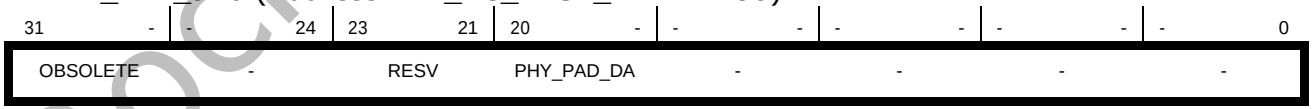
Name	Bits	Default	Range	Description
PHY_PAD_FDBK_DRIVE	22:0	0x0000ff	0x0-0x7fffff	Controls drive settings for gate

DENALI_PHY_925 (Address PHY_AC_BASE_ADDR + 29)



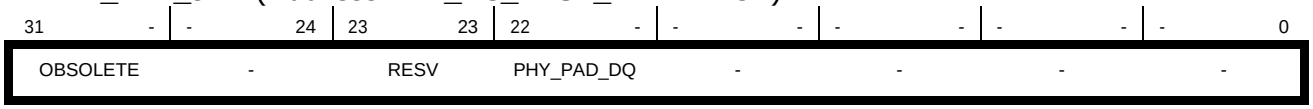
Name	Bits	Default	Range	Description
PHY_PAD_FDBK_DRIVE2	15:0	0x00ff	0x0-0xffff	Controls drive settings (enslice/

DENALI_PHY_926 (Address PHY_AC_BASE_ADDR + 30)



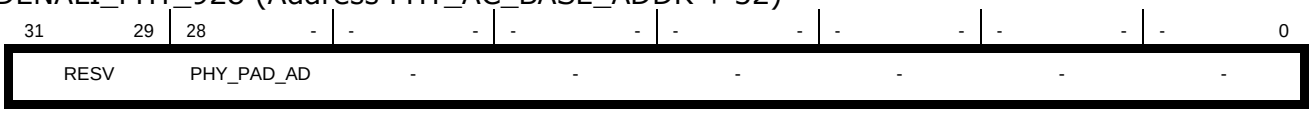
Name	Bits	Default	Range	Description
PHY_PAD_DATA_DRIVE	20:0	0x000000	0x0-0x1fffff	Controls drive settings for data

DENALI_PHY_927 (Address PHY_AC_BASE_ADDR + 31)



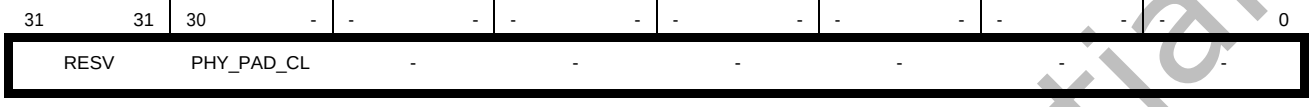
Name	Bits	Default	Range	Description
PHY_PAD_DQS_DRIVE	22:0	0x000000	0x0-0x7fffff	Controls drive settings for dqs

DENALI_PHY_928 (Address PHY_AC_BASE_ADDR + 32)



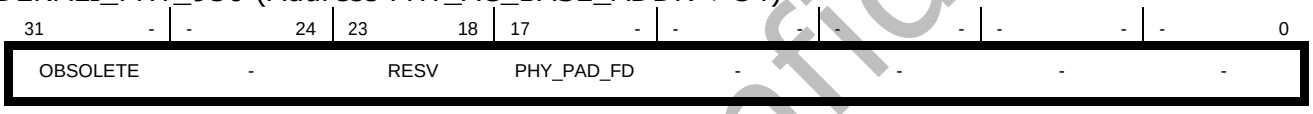
Name	Bits	Default	Range	Description
PHY_PAD_ADDR_DRIVE	28:0	0x000000ff	0x0-0x1fffffff	Controls drive settings for the

DENALI_PHY_929 (Address PHY_AC_BASE_ADDR + 33)



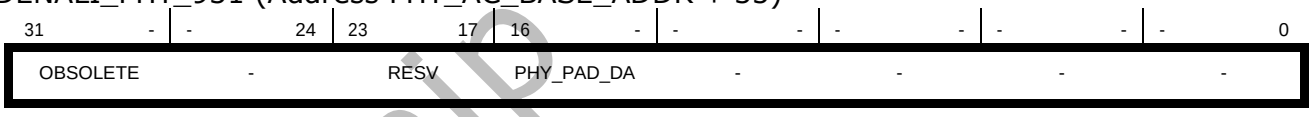
Name	Bits	Default	Range	Description
PHY_PAD_CLK_DRIVE	30:0	0x000000ff	0x0-0x7fffffff	Controls drive settings for clock

DENALI_PHY_930 (Address PHY_AC_BASE_ADDR + 34)



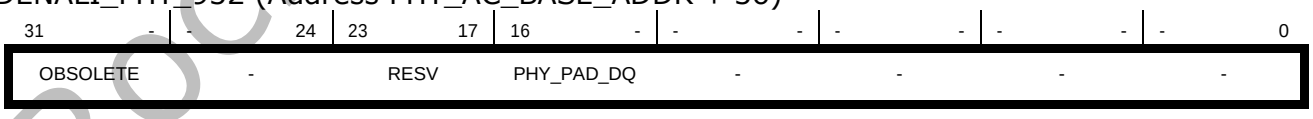
Name	Bits	Default	Range	Description
PHY_PAD_FDBK_TERM	17:0	0x04410	0x0-0x3ffff	Controls term settings for gate

DENALI_PHY_931 (Address PHY_AC_BASE_ADDR + 35)



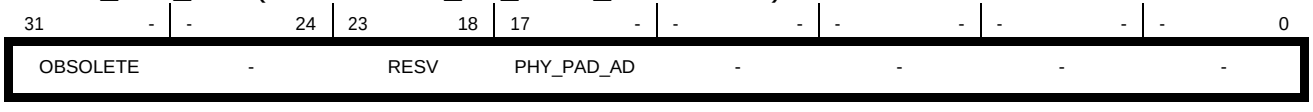
Name	Bits	Default	Range	Description
PHY_PAD_DATA_TERM	16:0	0x04410	0x0-0x1ffff	Controls term settings for data

DENALI_PHY_932 (Address PHY_AC_BASE_ADDR + 36)



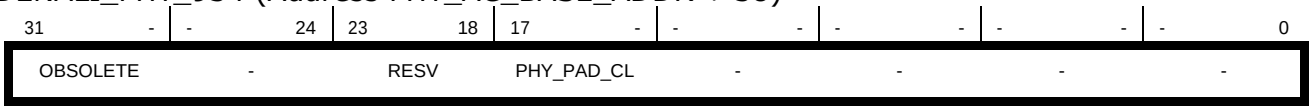
Name	Bits	Default	Range	Description
PHY_PAD_DQS_TERM	16:0	0x04410	0x0-0x1ffff	Controls term settings for dqs pads.

DENALI_PHY_933 (Address PHY_AC_BASE_ADDR + 37)



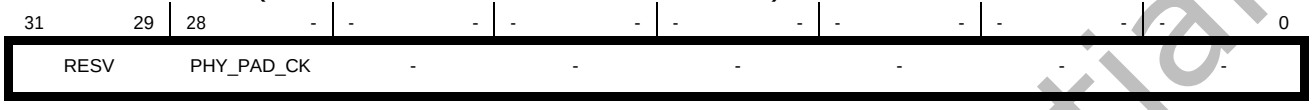
Name	Bits	Default	Range	Description
PHY_PAD_ADDR_TERM	17:0	0x04410	0x0-0x3ffff	Controls term settings for the

DENALI_PHY_934 (Address PHY_AC_BASE_ADDR + 38)



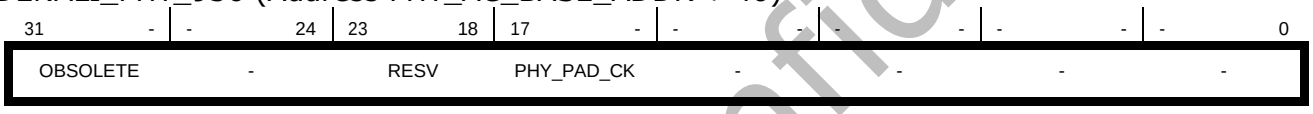
Name	Bits	Default	Range	Description
PHY_PAD_CLK_TERM	17:0	0x04410	0x0-0x3ffff	Controls term settings for clock

DENALI_PHY_935 (Address PHY_AC_BASE_ADDR + 39)



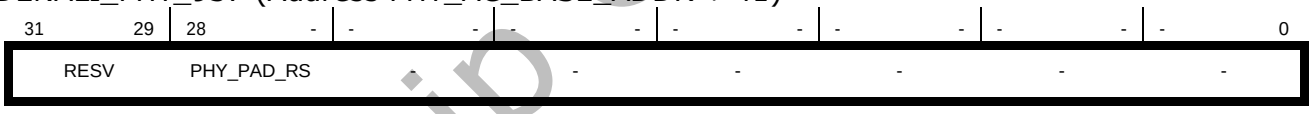
Name	Bits	Default	Range	Description
PHY_PAD_CKE_DRIVE	28:0	0x000000f	0x0-0x1fffffff	Controls drive settings for cke

DENALI_PHY_936 (Address PHY_AC_BASE_ADDR + 40)



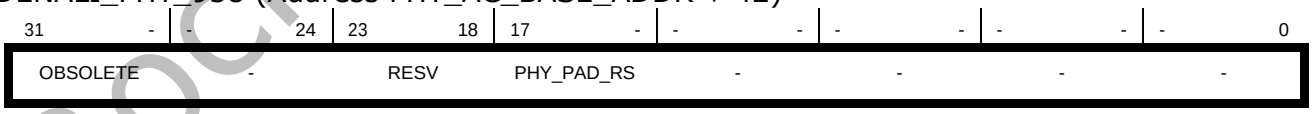
Name	Bits	Default	Range	Description
PHY_PAD_CKE_TERM	17:0	0x04410	0x0-0x3ffff	Controls term settings for ckepads.

DENALI_PHY_937 (Address PHY_AC_BASE_ADDR + 41)



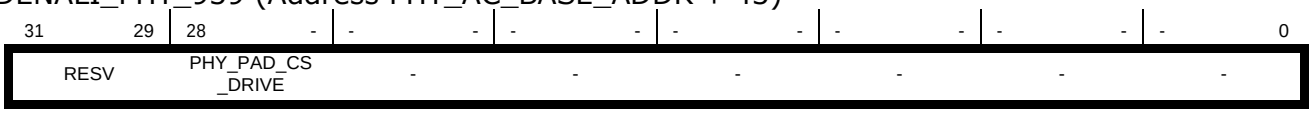
Name	Bits	Default	Range	Description
PHY_PAD_RST_DRIVE	28:0	0x000000f f	0x0-0x1fffffff	Controls drive settings for reset_n

DENALI_PHY_938 (Address PHY_AC_BASE_ADDR + 42)



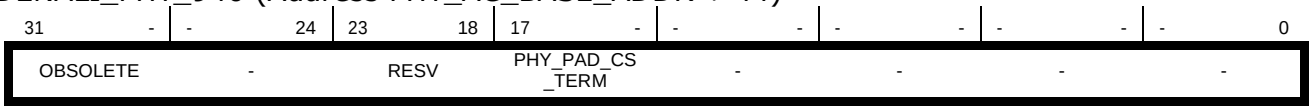
Name	Bits	Default	Range	Description
PHY_PAD_RST_TERM	17:0	0x04410	0x0-0x3ffff	Controls term settings for reset_n

DENALI_PHY_939 (Address PHY_AC_BASE_ADDR + 43)



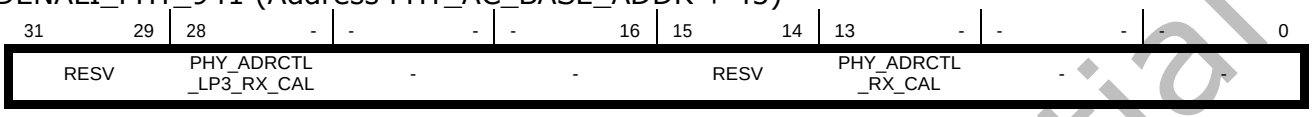
Name	Bits	Default	Range	Description
PHY_PAD_CS_DRIVE	28:0	0x000000f	0x0-0x1fffffff	Controls drive settings for cspads.

DENALI_PHY_940 (Address PHY_AC_BASE_ADDR + 44)



Name	Bits	Default	Range	Description
PHY_PAD_CS_TERM	17:0	0x04410	0x0-0x3ffff	Controls term settings for cs pads.

DENALI_PHY_941 (Address PHY_AC_BASE_ADDR + 45)

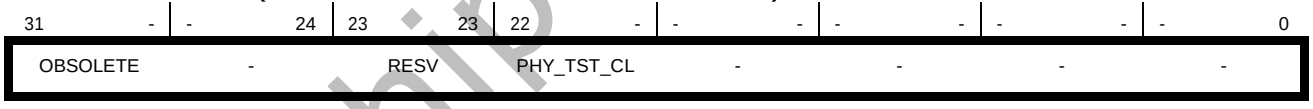


Name	Bits	Default	Range	Description
PHY_ADRCTL_LP3_RX_CAL	28:16	0x0000	0x0-0x1fff	PHY CKE/RESET_N RX calibration controls.
PHY_ADRCTL_RX_CAL	13:0	0x0000	0x0-0x3fff	PHY address/control RX calibration

DENALI_PHY_942 (Address PHY_AC_BASE_ADDR + 46)

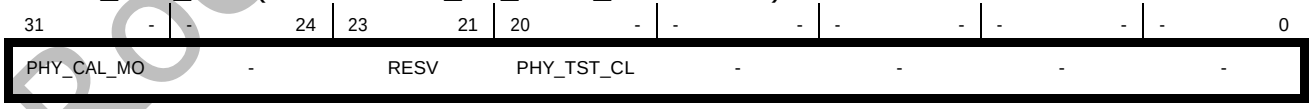
Name	Bits	Default	Range	Description
PHY_TST_CLK_PAD_CTRL	31:0	0x000000	0x0-0xffffffff	PHY test clock pad controls.

DENALI_PHY_943 (Address PHY_AC_BASE_ADDR + 47)



Name	Bits	Default	Range	Description
PHY_TST_CLK_PAD_CTRL2	22:0	0x000000	0x0-0x7fffff	PHY test clock pad additional

DENALI_PHY_944 (Address PHY_AC_BASE_ADDR + 48)



Name	Bits	Default	Range	Description
PHY_CAL_MODE_0	31:24	0x00	0x0-0xff	Pad calibration mode bits for block 0. Bit (0) disables pad calibration upon initialization. Bit (1) enables automatic interval based calibration. Bits (3:2) set the base
PHY_TST_CLK_PAD_CTRL3	20:0	0x000000	0x0-0x1fffff	PHY test clock pad additional

DENALI_PHY_945 (Address PHY_AC_BASE_ADDR + 49)

31 -	- -	- -	- 16	15 9	8 8	7 1	0 0
OBSOLETE	-	-	-	RESV	PHY_CAL_ST	RESV	PHY_CAL_CL

Name	Bits	Default	Range	Description
PHY_CAL_START_0	8	0x0	0x0-0x1	Manual start for the pad calibration state machine for block 0. Set to 1
PHY_CAL_CLEAR_0	0	0x0	0x0-0x1	Clear the pad calibration state machine and results for block 0.

DENALI_PHY_946 (Address PHY_AC_BASE_ADDR + 50)

31 -	- -	- -	- -	- -	- -	- -	- -	- 0
PHY_CAL_INT ERVAL_COUN	-	-	-	-	-	-	-	-

Name	Bits	Default	Range	Description
PHY_CAL_INTERVAL_COUNT_0	31:0	0x000000	0x0-0xffffffff	Pad calibration interval counter

DENALI_PHY_947 (Address PHY_AC_BASE_ADDR + 51)

31 -	- -	- -	- 16	15 11	10 8	7 -	- 0
OBSOLETE	-	-	-	RESV	PHY_CAL_CL	PHY_CAL_SA	-

Name	Bits	Default	Range	Description
PHY_CAL_CLK_SELECT_0	10:8	0x0	0x0-0x7	Pad calibration pad clock frequency
PHY_CAL_SAMPLE_WAIT_0	7:0	0x00	0x0-0xff	Pad calibration state machine wait count in pad clock cycles for block

DENALI_PHY_948 (Address PHY_AC_BASE_ADDR + 52)

31 -	- 24	23 -	- -	- -	- -	- -	- -	- 0
OBSOLETE	-	PHY_CAL_RE	-	-	-	-	-	

Name	Bits	Default	Range	Description
PHY_CAL_RESULT_OBS_0	23:0	0x000000	0x0-0xffffff	Pad calibration results observation

DENALI_PHY_949 (Address PHY_AC_BASE_ADDR + 53)

31 -	- 24	23 -	- -	- -	- -	- -	- -	- 0
OBSOLETE	-	PHY_CAL_RE	-	-	-	-	-	

Name	Bits	Default	Range	Description
PHY_CAL_RESULT2_OBS_0	23:0	0x000000	0x0-0xffffff	Pad calibration results (CKE/ RESET_N) observation values for

DENALI_PHY_950 (Address PHY_AC_BASE_ADDR + 54)

31 25	24 24	23 17	16 16	15 -	- -	- -	- 0

RESV	PHY_AC_LPBK_ERR_CLEA	RESV	PHY_ADRCTL_MANUAL_UP	PHY_PAD_AT B_CTRL	-	-	-

Name	Bits	Default	Range	Description
PHY_AC_LPBK_ERR_CLEAR	24	0x0	0x0-0x1	Address/control loopback error clear. Set to 1 to clear error.
PHY_ADRCTL_MANUAL_UPDATE	16	0x0	0x0-0x1	Address/control manual update of slave delay lines. Set to 1 to
PHY_PAD_ATB_CTRL	15:0	0x0000	0x0-0xffff	Pad ATB control settings. Bit (0) is the enable signal. Bits (5:1) are the ATB data signals. Bits (15:8) are

DENALI_PHY_951 (Address PHY_AC_BASE_ADDR + 55)

31 -	- 24	23 -	- 16	15 12	11 8	7 2	1 0
OBSOLETE	-	PHY_AC_LPBK_CONTROL	-	RESV	PHY_AC_LPBK_ENABLE	RESV	PHY_AC_LPBK_OBS_SELE

Name	Bits	Default	Range	Description
PHY_AC_LPBK_CONTROL	23:16	0x00	0x0-0xff	Address/control slice loopback
PHY_AC_LPBK_ENABLE	11:8	0x0	0x0-0xf	Loopback enable for the address/
PHY_AC_LPBK_OBS_SELECT	1:0	0x0	0x0-0x3	Select value to map an individual address/control slice observation

DENALI_PHY_952 (Address PHY_AC_BASE_ADDR + 56)

31 -	- -	- -	- -	- -	- -	- -	- 0
PHY_AC_LPBK_RESULT_O	-	-	-	-	-	-	-

Name	Bits	Default	Range	Description
PHY_AC_LPBK_RESULT_OBS	31:0	0x00000000	0x0-0xffffffff	Observation register for the address/control slices. READ-

DENALI_PHY_953 (Address PHY_AC_BASE_ADDR + 57)

31 -	- 24	23 22	21 16	15 10	9 8	7 1	0 0
OBSOLETE	-	RESV	PHY_AC_CLK_LPBK_CONT	RESV	PHY_AC_CLK_LPBK_ENABL	RESV	PHY_AC_CLK_LPBK_OBS_

Name	Bits	Default	Range	Description
PHY_AC_CLK_LPBK_CONTROL	21:16	0x00	0x0-0x3f	Mem clk block loopback control
PHY_AC_CLK_LPBK_ENABLE	9:8	0x0	0x0-0x3	Loopback enable for mem clk
PHY_AC_CLK_LPBK_OBS_SELECT	0	0x0	0x0-0x1	Select value to map an individual mem clk block observation register

DENALI_PHY_954 (Address PHY_AC_BASE_ADDR + 58)

31 -	- 24	23 17	16 16	15 -	- -	- -	- 0

PHY_DATA_BYTE_ORDER	-	RESV	PHY_AC_PWR_RDC_DISABL	PHY_AC_CLK_LPBK_RESU	-	-	-

Name	Bits	Default	Range	Description
PHY_DATA_BYTE_ORDER_SEL	31:24	0x00	0x0-0xff	Used to define the data
PHY_AC_PWR_RDC_DISABLE	16	0x0	0x0-0x1	ac slice power reduction disable.
PHY_AC_CLK_LPBK_RESULT_OBS	15:0	0x0000	0x0-0xffff	Observation register for mem clk

DENALI_PHY_955 (Address PHY_AC_BASE_ADDR + 59)

31	-	24	23	17	16	16	15	10	9	8	7	3	2	0
OBSOLETE	-	RESV			PHY_CS_DLY_UPT_PER_A		RESV		PHY_ADRCTL_MSTR_DLY_		RESV		PHY_ADR_DIS ABLE	

Name	Bits	Default	Range	Description
PHY_CS_DLY_UPT_PER_AC_SLICE	16	0x0	0x0-0x1	cs grp slave delay line is updated
PHY_ADRCTL_MSTR_DLY_ENC_SEL	9:8	0x0	0x0-0x3	Select the
PHY_ADR_DISABLE	2:0	0x0	0x0-0x7	Disable the unused adr slice to

DENALI_PHY_956 (Address PHY_AC_BASE_ADDR + 60)

31	-	-	-	-	-	-	-	-	-	-	-	-	-	0
PHY_DDL_AC_ENABLE		-		-		-		-		-		-		-

Name	Bits	Default	Range	Description
PHY_DDL_AC_ENABLE	31:0	0x00000000	0x0-0xffffffff	PHY Address/Control DDL BIST

DENALI_PHY_957 (Address PHY_AC_BASE_ADDR + 61)

31	26	25	24	23	17	16	16	15	11	10	-	-	-	-	0
RESV		PHY_DLL_RST_EN		RESV		PHY_PAD_BACKGROUND		RESV		PHY_DDL_AC_MODE			-		-

Name	Bits	Default	Range	Description
PHY_DLL_RST_EN	25:24	0x0	0x0-0x3	PHY DLL reset software interface
PHY_PAD_BACKGROUND_CAL	16	0x0	0x0-0x1	PHY background pad calibration
PHY_DDL_AC_MODE	10:0	0x000	0x0-0x7ff	PHY Address/Control DDL BIST

DENALI_PHY_958 (Address PHY_AC_BASE_ADDR + 62)

31	-	24	23	20	19	16	15	12	11	-	-	-	-	0
RESV	-	RESV			PHY_DS_INIT_COMPLETE_		RESV		PHY_AC_INIT_COMPLETE_			-		-

Name	Bits	Default	Range	Description
PHY_DS_INIT_COMPLETE_OBS	19:16	0x0	0x0-0xf	Observation register for dfi_init_complete for data slice. Bit0

PHY_AC_INIT_COMPLETE_OBS	11:0	0x000	0x0-0xfff	Observation register for dfi_init_complete for adr and ac slice. Bit 0 is for dfi_init_complete for all slices. Bit(7:4) is for adr slice,

2. PI register

PI_REG_0

Address: Operational Base + offset (0x0000)

DDR PHY Independent Register 0

Bit	Attr	Reset Value	Description
31:16	RO	0x0000	pi_version Holds the PI version number.
15:12	RO	0x0	reserved
11:8	RW	0x0	pi_dram_class Defines the mode of operation of the PI. 4'b0110: DDR3 4'b0111: LPDDR3 4'b1011: LPDDR4 other value: reserved
7:1	RO	0x0	reserved
0	RW	0x0	pi_start Initiates command processing in the PI. Set to 1 to initiate.

PI_REG_1

Address: Operational Base + offset (0x0004)

DDR PHY Independent Register 1

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	pi_tcmp_gap Indicates DRAM timing in DFI clock cycles. Specifies the minimum gap between two commands. Used for guarding the timing from the last command of DDR controller and the first command of PI when DDR controller passes the control of the DFI bus to the PI.
15:9	RO	0x0	reserved
8	RW	0x0	pi_init_lvl_en Enables the initial leveling sequence after PI initialization procedure. Set to 1 to enable.
7:1	RO	0x0	reserved
0	RW	0x0	pi_normal_lvl_seq Enables the PI strategy that PI must finish all the pending leveling before it releases the DFI bus.

PI_REG_2

Address: Operational Base + offset (0x0008)

DDR PHY Independent Register 2

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pi_tdfi_phymstr_max_f0 Defines the DFI tPHYMSTR_MAX timing parameter (in DFI clocks), the maximum cycles that dfi_phymstr_req following the assertion of dfi_phymstr_ack can be asserted. If programmed to a non-zero, a timing violation causes an interrupt and bit0 set in the PI_REG_22.pi_control_error_status parameter. The suffix f0 of the parameter name is omitted when in non-DFS mode.

PI_REG_3
Address: Operational Base + offset (0x000c)
DDR PHY Independent Register 3

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	pi_tdfi_phymstr_resp_f0 Defines the DFI tPHYMSTR_RESP timing parameter (in DFI clocks), the maximum cycles between a dfi_phymstr_req assertion and a dfi_phymstr_ack assertion. If programmed to a non-zero, a timing violation causes an interrupt and bit1 set in the PI_REG_22.pi_control_error_status parameter. The suffix f0 of the parameter name is omitted when in non-DFS mode.

PI_REG_4
Address: Operational Base + offset (0x0010)
DDR PHY Independent Register 4

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pi_tdfi_phymstr_max_f1 Defines the DFI tPHYMSTR_MAX timing parameter (in DFI clocks), the maximum cycles that dfi_phymstr_req following the assertion of dfi_phymstr_ack can be asserted. If programmed to a non-zero, a timing violation causes an interrupt and bit0 set in the PI_REG_22.pi_control_error_status parameter. The suffix f1 of the parameter name is omitted when in non-DFS mode.

PI_REG_5
Address: Operational Base + offset (0x0014)
DDR PHY Independent Register 5

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	pi_tdfi_phymstr_resp_f1 Defines the DFI tPHYMSTR_RESP timing parameter (in DFI clocks), the maximum cycles between a dfi_phymstr_req assertion and a dfi_phymstr_ack assertion. If programmed to a non-zero, a timing violation causes an interrupt and bit1 set in the PI_REG_22.pi_control_error_status parameter. The suffix f1 of the parameter name is omitted when in non-DFS mode.

PI_REG_6
Address: Operational Base + offset (0x0018)
DDR PHY Independent Register 6

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pi_tdfi_phymstr_max_f2 Defines the DFI tPHYMSTR_MAX timing parameter (in DFI clocks), the maximum cycles that dfi_phymstr_req following the assertion of dfi_phymstr_ack can be asserted. If programmed to a non-zero, a timing violation causes an interrupt and bit0 set in the PI_REG_22.pi_control_error_status parameter. The suffix f2 of the parameter name is omitted when in non-DFS mode.

PI_REG_7
Address: Operational Base + offset (0x001c)
DDR PHY Independent Register 7

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	pi_tdfi_phyupd_resp_f0 Defines the DFI tPHYUPD_RESP timing parameter (in DFI clocks), the maximum cycles between a dfi_phyupd_req assertion and a dfi_phyupd_ack assertion. If programmed to a non-zero, a timing violation causes an interrupt and bit8 set in the PI_REG_193.pi_update_error_status parameter and bit8 set in the PI_REG_22.pi_control_error_status parameter. The suffix f0 of the parameter name is omitted when in non-DFS mode.
15:0	RW	0x0000	pi_tdfi_phymstr_resp_f2 Defines the DFI tPHYMSTR_RESP timing parameter (in DFI clocks), the maximum cycles between a dfi_phymstr_req assertion and a dfi_phymstr_ack assertion. If programmed to a non-zero, a timing violation causes an interrupt and bit1 set in the PI_REG_22.pi_control_error_status parameter. The suffix f2 of the parameter name is omitted when in non-DFS mode.

PI_REG_8
Address: Operational Base + offset (0x0020)
DDR PHY Independent Register 8

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pi_tdfi_phyupd_type0_f0 Defines the DFI tPHYUPD_TYPE0 timing parameter (in DFI clocks), the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for dfi_phyupd_type 0. If programmed to a non-zero, a timing violation causes an interrupt and bit4 set in the PI_REG_193.pi_update_error_status parameter and bit4 set in the PI_REG_22.pi_control_error_status parameter. The suffix f0 of the parameter name is omitted when in non-DFS mode.

PI_REG_9
Address: Operational Base + offset (0x0024)
DDR PHY Independent Register 9

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pi_tdfi_phyupd_type1_f0 Defines the DFI tPHYUPD_TYPE1 timing parameter (in DFI clocks), the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for dfi_phyupd_type 1. If programmed to a non-zero, a timing violation causes an interrupt and bit5 set in the PI_REG_193.pi_update_error_status parameter and bit5 set in the PI_REG_22.pi_control_error_status parameter. The suffix f0 of the parameter name is omitted when in non-DFS mode.

PI_REG_10
Address: Operational Base + offset (0x0028)
DDR PHY Independent Register 10

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pi_tdfi_phyupd_type2_f0 Defines the DFI tPHYUPD_TYPE2 timing parameter (in DFI clocks), the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for dfi_phyupd_type 2. If programmed to a non-zero, a timing violation causes an interrupt and bit6 set in the PI_REG_193.pi_update_error_status parameter and bit6 set in the PI_REG_22.pi_control_error_status parameter. The suffix f0 of the parameter name is omitted when in non-DFS mode.

PI_REG_11
Address: Operational Base + offset (0x002c)
DDR PHY Independent Register 11

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pi_tdfi_phyupd_type3_f0 Defines the DFI tPHYUPD_TYPE3 timing parameter (in DFI clocks), the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for dfi_phyupd_type 3. If programmed to a non-zero, a timing violation causes an interrupt and bit7 set in the PI_REG_193.pi_update_error_status parameter and bit7 set in the PI_REG_22.pi_control_error_status parameter. The suffix f0 of the parameter name is omitted when in non-DFS mode.

PI_REG_12
Address: Operational Base + offset (0x0030)
DDR PHY Independent Register 12

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	pi_tdfi_phyupd_resp_f1 Defines the DFI tPHYUPD_RESP timing parameter (in DFI clocks), the maximum cycles between a dfi_phyupd_req assertion and a dfi_phyupd_ack assertion. If programmed to a non-zero, a timing violation causes an interrupt and bit8 set in the PI_REG_193.pi_update_error_status parameter and bit8 set in the PI_REG_22.pi_control_error_status parameter. The suffix f1 of the parameter name is omitted when in non-DFS mode.

PI_REG_13
Address: Operational Base + offset (0x0034)
DDR PHY Independent Register 13

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pi_tdfi_phyupd_type0_f1 Defines the DFI tPHYUPD_TYPE0 timing parameter (in DFI clocks), the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for dfi_phyupd_type 0. If programmed to a non-zero, a timing violation causes an interrupt and bit4 set in the PI_REG_193.pi_update_error_status parameter and bit4 set in the PI_REG_22.pi_control_error_status parameter. The suffix f1 of the parameter name is omitted when in non-DFS mode.

PI_REG_14
Address: Operational Base + offset (0x0038)
DDR PHY Independent Register 14

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pi_tdfi_phyupd_type1_f1 Defines the DFI tPHYUPD_TYPE1 timing parameter (in DFI clocks), the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for dfi_phyupd_type 1. If programmed to a non-zero, a timing violation causes an interrupt and bit5 set in the PI_REG_193.pi_update_error_status parameter and bit5 set in the PI_REG_22.pi_control_error_status parameter. The suffix f1 of the parameter name is omitted when in non-DFS mode.

PI_REG_15
Address: Operational Base + offset (0x003c)
DDR PHY Independent Register 15

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pi_tdfi_phyupd_type2_f1 Defines the DFI tPHYUPD_TYPE2 timing parameter (in DFI clocks), the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for dfi_phyupd_type 2. If programmed to a non-zero, a timing violation causes an interrupt and bit6 set in the PI_REG_193.pi_update_error_status parameter and bit6 set in the PI_REG_22.pi_control_error_status parameter. The suffix f1 of the parameter name is omitted when in non-DFS mode.

PI_REG_16
Address: Operational Base + offset (0x0040)
DDR PHY Independent Register 16

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pi_tdfi_phyupd_type3_f1 Defines the DFI tPHYUPD_TYPE3 timing parameter (in DFI clocks), the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for dfi_phyupd_type 3. If programmed to a non-zero, a timing violation causes an interrupt and bit7 set in the PI_REG_193.pi_update_error_status parameter and bit7 set in the PI_REG_22.pi_control_error_status parameter. The suffix f1 of the parameter name is omitted when in non-DFS mode.

PI_REG_17
Address: Operational Base + offset (0x0044)
DDR PHY Independent Register 17

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	pi_tdfi_phyupd_resp_f2 Defines the DFI tPHYUPD_RESP timing parameter (in DFI clocks), the maximum cycles between a dfi_phyupd_req assertion and a dfi_phyupd_ack assertion. If programmed to a non-zero, a timing violation causes an interrupt and bit8 set in the PI_REG_193.pi_update_error_status parameter and bit8 set in the PI_REG_22.pi_control_error_status parameter. The suffix f2 of the parameter name is omitted when in non-DFS mode.

PI_REG_18
Address: Operational Base + offset (0x0048)
DDR PHY Independent Register 18

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pi_tdfi_phyupd_type0_f2 Defines the DFI tPHYUPD_TYPE0 timing parameter (in DFI clocks), the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for dfi_phyupd_type 0. If programmed to a non-zero, a timing violation causes an interrupt and bit4 set in the PI_REG_193.pi_update_error_status parameter and bit4 set in the PI_REG_22.pi_control_error_status parameter. The suffix f2 of the parameter name is omitted when in non-DFS mode.

PI_REG_19
Address: Operational Base + offset (0x004c)
DDR PHY Independent Register 19

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pi_tdfi_phyupd_type1_f2 Defines the DFI tPHYUPD_TYPE1 timing parameter (in DFI clocks), the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for dfi_phyupd_type 1. If programmed to a non-zero, a timing violation causes an interrupt and bit5 set in the PI_REG_193.pi_update_error_status parameter and bit5 set in the PI_REG_22.pi_control_error_status parameter. The suffix f2 of the parameter name is omitted when in non-DFS mode.

PI_REG_20
Address: Operational Base + offset (0x0050)
DDR PHY Independent Register 20

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pi_tdfi_phyupd_type2_f2 Defines the DFI tPHYUPD_TYPE2 timing parameter (in DFI clocks), the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for dfi_phyupd_type 2. If programmed to a non-zero, a timing violation causes an interrupt and bit6 set in the PI_REG_193.pi_update_error_status parameter and bit6 set in the PI_REG_22.pi_control_error_status parameter. The suffix f2 of the parameter name is omitted when in non-DFS mode.

PI_REG_21
Address: Operational Base + offset (0x0054)
DDR PHY Independent Register 21

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pi_tdfi_phyupd_type3_f2 Defines the DFI tPHYUPD_TYPE3 timing parameter (in DFI clocks), the maximum cycles that dfi_phyupd_req can assert after dfi_phyupd_ack for dfi_phyupd_type 3. If programmed to a non-zero, a timing violation causes an interrupt and bit7 set in the PI_REG_193.pi_update_error_status parameter and bit7 set in the PI_REG_22.pi_control_error_status parameter. The suffix f2 of the parameter name is omitted when in non-DFS mode.

PI_REG_22
Address: Operational Base + offset (0x0058)
DDR PHY Independent Register 22

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16	RW	0x1	pi_exit_after_init_calvl Releases the DFI bus after complete initialization CA training and requests DFI bus again for the remaining initialization training. The DFI bus release is for the controller to issue MRW/ZQ after the PI completes initialization CA leveling, based on the JEDEC protocol requirement.
15:9	RO	0x0	reserved
8:0	RW	0x000	pi_control_error_status Identifies the source of any pi_control phyupd_req/ phylvl_req_cs_n errors. Value of 1 indicates a timing violation of the associated timing parameter Bit 8: pi_control triggered phyupd_resp_error. Bit 7: pi_control triggered phyupd_type3_error. Bit 6: pi_control triggered phyupd_type2_error. Bit 5: pi_control triggered phyupd_type1_error. Bit 4: pi_control triggered phyupd_type0_error. Bit 3: phylvl_resp_error. Bit 2: phylvl_max_error. Bit 1: phymstr_resp_error. Bit 0: phymstr_max_error.

PI_REG_23
Address: Operational Base + offset (0x005c)
DDR PHY Independent Register 23

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pi_freq_map User indicates all the supported working frequencies. Each bit represents one supported frequency.

PI_REG_24
Address: Operational Base + offset (0x0060)

DDR PHY Independent Register 24

Bit	Attr	Reset Value	Description
31:24	RW	0x00	pi_power_on_seq_end_array Indicates the step that is the last step of the power-on sequence.
23:16	RW	0x00	pi_power_on_seq_bypass_array Indicates the bypassed steps of power on sequence.
15:9	RO	0x0	reserved
8	RW	0x1	pi_init_dfs_calvl_only Enables the initial leveling sequence loop that only CA training executes DFS.
7:5	RO	0x0	reserved
4:0	RW	0x00	pi_init_work_freq Indicates the initial work frequency after initialization and initial leveling sequence.

PI_REG_25
Address: Operational Base + offset (0x0064)
DDR PHY Independent Register 25

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	pi_seq1_pat Indicates user-defined power-on sequence 1.

PI_REG_26
Address: Operational Base + offset (0x0068)
DDR PHY Independent Register 26

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	pi_seq1_pat_mask Indicates user-defined command mask for power-on sequence 1.

PI_REG_27
Address: Operational Base + offset (0x006c)
DDR PHY Independent Register 27

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	pi_seq2_pat Indicates user-defined power-on sequence 2.

PI_REG_28
Address: Operational Base + offset (0x0070)
DDR PHY Independent Register 28

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	pi_seq2_pat_mask Indicates user-defined command mask for power-on sequence 2.

PI_REG_29
Address: Operational Base + offset (0x0074)
DDR PHY Independent Register 29

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	pi_seq3_pat Indicates user-defined power-on sequence 3.

PI_REG_30
Address: Operational Base + offset (0x0078)
DDR PHY Independent Register 30

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	pi_seq3_pat_mask Indicates user-defined command mask for power-on sequence 3.

PI_REG_31
Address: Operational Base + offset (0x007c)
DDR PHY Independent Register 31

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	pi_seq4_pat Indicates user-defined power-on sequence 4.

PI_REG_32
Address: Operational Base + offset (0x0080)
DDR PHY Independent Register 32

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	pi_seq4_pat_mask Indicates user-defined command mask for power-on sequence 4.

PI_REG_33
Address: Operational Base + offset (0x0084)
DDR PHY Independent Register 33

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	pi_seq5_pat Indicates user-defined power-on sequence 5.

PI_REG_34
Address: Operational Base + offset (0x0088)
DDR PHY Independent Register 34

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	pi_seq5_pat_mask Indicates user-defined command mask for power-on sequence 5.

PI_REG_35
Address: Operational Base + offset (0x008c)
DDR PHY Independent Register 35

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	pi_seq6_pat Indicates user-defined power-on sequence 6.

PI_REG_36
Address: Operational Base + offset (0x0090)
DDR PHY Independent Register 36

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	pi_seq6_pat_mask Indicates user-defined command mask for power-on sequence 6.

PI_REG_37
Address: Operational Base + offset (0x0094)
DDR PHY Independent Register 37

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	pi_seq7_pat Indicates user-defined power-on sequence 7.

PI_REG_38
Address: Operational Base + offset (0x0098)
DDR PHY Independent Register 38

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	pi_seq7_pat_mask Indicates user-defined command mask for power-on sequence 7.

PI_REG_39
Address: Operational Base + offset (0x009c)
DDR PHY Independent Register 39

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	pi_seq8_pat Indicates user-defined power-on sequence 8.

PI_REG_40
Address: Operational Base + offset (0x00a0)
DDR PHY Independent Register 40

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:0	RW	0x00000000	pi_seq8_pat_mask Indicates user-defined command mask for power-on sequence 8.

PI_REG_41
Address: Operational Base + offset (0x00a4)
DDR PHY Independent Register 41

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:24	RW	0x0	pi_cs_map Defines the chip selects that are active.
23:9	RO	0x0	reserved
8	RW	0x1	pi_sw_rst_n Indicates user request to reset the whole system except parameter DFFs. Set 0 to reset, set to 1 to release.
7:1	RO	0x0	reserved
0	RW	0x1	pi_wdt_disable Disables the watchdog caused by phymstr_req/phylvl_req_cs_n response error. Set 1 to disable.

PI_REG_42
Address: Operational Base + offset (0x00a8)
DDR PHY Independent Register 42

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x0	pi_tmrr Indicates DRAM TMRR value in cycles.
23:16	RW	0x00	pi_tdelay_rdwr_2_bus_idle_f2 Indicates the delay from read or write to bus idle. Recommended setting is delay time from read command that issued to the last read data received. The suffix "_f2" of the parameter name is omitted when in non-DFS mode.
15:8	RW	0x00	pi_tdelay_rdwr_2_bus_idle_f1 Indicates the delay from read or write to bus idle. Recommended setting is delay time from read command that issued to the last read data received. The suffix "_f1" of the parameter name is omitted when in non-DFS mode.
7:0	RW	0x00	pi_tdelay_rdwr_2_bus_idle_f0 Indicates the delay from read or write to bus idle. Recommended setting is delay time from read command that issued to the last read data received. The suffix "_f0" of the parameter name is omitted when in non-DFS mode.

PI_REG_43
Address: Operational Base + offset (0x00ac)
DDR PHY Independent Register 43

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x00	pi_wrlat_f1 Indicates DRAM WRLAT value in cycles. The suffix "_f1" of the parameter name is omitted when in non-DFS mode.
23	RO	0x0	reserved
22:16	RW	0x00	pi_caslat_lin_f0 Sets latency from read command send to data receive from/to controller. Bit0 is half-cycle increment and the upper bits define memory CAS latency for the controller. The suffix "_f0" of the parameter name is omitted when in non-DFS mode.
15:14	RO	0x0	reserved
13:8	RW	0x00	pi_additive_lat_f0 Indicates DRAM additive latency value in cycles. The suffix "_f0" of the parameter name is omitted when in non-DFS mode.
7:5	RO	0x0	reserved
4:0	RW	0x00	pi_wrlat_f0 Indicates DRAM WRLAT value in cycles. The suffix "_f0" of the parameter name is omitted when in non-DFS mode.

PI_REG_44
Address: Operational Base + offset (0x00b0)
DDR PHY Independent Register 44

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	pi_additive_lat_f2 Indicates DRAM additive latency value in cycles. The suffix "_f2" of the parameter name is omitted when in non-DFS mode.
23:21	RO	0x0	reserved
20:16	RW	0x00	pi_wrlat_f2 Indicates DRAM WRLAT value in cycles. The suffix "_f2" of the parameter name is omitted when in non-DFS mode.
15	RO	0x0	reserved
14:8	RW	0x00	pi_caslat_lin_f1 Sets latency from read command send to data receive from/to controller. Bit0 is half-cycle increment and the upper bits define memory CAS latency for the controller. The suffix "_f1" of the parameter name is omitted when in non-DFS mode.
7:6	RO	0x0	reserved
5:0	RW	0x00	pi_additive_lat_f1 Indicates DRAM additive latency value in cycles. The suffix "_f1" of the parameter name is omitted when in non-DFS mode.

PI_REG_45
Address: Operational Base + offset (0x00b4)
DDR PHY Independent Register 45

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	pi_mcaref_forward_only Pass mc auto refresh command to DRAM device, not generate auto-refresh by PI. It is recommended to set to 1.
23:17	RO	0x0	reserved
16	WO	0x0	pi_arefresh Initiates auto-refresh at the end of the current burst boundary. Set to 1 to trigger.
15:10	RO	0x0	reserved
9:8	RW	0x0	pi_preamble_support Indicates selection of one or two-cycle preamble for read and write burst transfers.
7	RO	0x0	reserved
6:0	RW	0x00	pi_caslat_lin_f2 Sets latency from read command send to data receive from/to controller. Bit0 is half-cycle increment and the upper bits define memory CAS latency for the controller. The suffix "_f2" of the parameter name is omitted when in non-DFS mode.

PI_REG_46
Address: Operational Base + offset (0x00b8)
DDR PHY Independent Register 46

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	pi_tref_f0 Indicates DRAM TREF value in cycles. The suffix "_f0" of the parameter name is omitted when in non-DFS mode.
15:10	RO	0x0	reserved
9:0	RW	0x000	pi_trfc_f0 Indicates DRAM TRFC value in cycles. The suffix "_f0" of the parameter name is omitted when in non-DFS mode.

PI_REG_47
Address: Operational Base + offset (0x00bc)
DDR PHY Independent Register 47

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	pi_tref_f1 Indicates DRAM TREF value in cycles. The suffix "_f1" of the parameter name is omitted when in non-DFS mode.
15:10	RO	0x0	reserved
9:0	RW	0x000	pi_trfc_f1 Indicates DRAM TRFC value in cycles. The suffix "_f1" of the parameter name is omitted when in non-DFS mode.

PI_REG_48
Address: Operational Base + offset (0x00c0)
DDR PHY Independent Register 48

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	pi_tref_f2 Indicates DRAM TREF value in cycles. The suffix "_f2" of the parameter name is omitted when in non-DFS mode.
15:10	RO	0x0	reserved
9:0	RW	0x000	pi_trfc_f2 Indicates DRAM TRFC value in cycles. The suffix "_f2" of the parameter name is omitted when in non-DFS mode.

PI_REG_49
Address: Operational Base + offset (0x00c4)
DDR PHY Independent Register 49

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	WO	0x0	pi_swlvl_load Indicates user request to load delays and execute software leveling. Set to 1 to trigger.
23:8	RW	0x0000	pi_tref_interval Defines the cycles between refreshes to different chip selects.
7:0	RO	0x0	reserved

PI_REG_50
Address: Operational Base + offset (0x00c8)
DDR PHY Independent Register 50

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RO	0x0	pi_sw_wrlvl_resp_2 Indicates write leveling response for data slice 2.
23:17	RO	0x0	reserved
16	RO	0x0	pi_sw_wrlvl_resp_1 Indicates write leveling response for data slice 1.
15:9	RO	0x0	reserved
8	RO	0x0	pi_sw_wrlvl_resp_0 Indicates write leveling response for data slice 0.
7:1	RO	0x0	reserved
0	RO	0x0	pi_swlvl_op_done Indicates signals that software leveling is currently in progress. Value of 1 indicates operation complete.

PI_REG_51
Address: Operational Base + offset (0x00cc)
DDR PHY Independent Register 51

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:24	RO	0x0	pi_sw_rdlvl_resp_2 Indicates read leveling response for data slice 2.
23:18	RO	0x0	reserved
17:16	RO	0x0	pi_sw_rdlvl_resp_1 Indicates read leveling response for data slice 1.
15:10	RO	0x0	reserved
9:8	RO	0x0	pi_sw_rdlvl_resp_0 Indicates read leveling response for data slice 0.
7:1	RO	0x0	reserved
0	RO	0x0	pi_sw_wrlvl_resp_3 Indicates write leveling response for data slice 3.

PI_REG_52
Address: Operational Base + offset (0x00d0)
DDR PHY Independent Register 52

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	WO	0x0	pi_swlvl_start Indicates user request to initiate software leveling of type in the PI_REG_52.pi_sw_leveling_mode parameter. Set to 1 to trigger.
23:19	RO	0x0	reserved
18:16	RW	0x0	pi_sw_leveling_mode Defines the leveling operation for software leveling. Set to 3'b001 for write leveling, set to 3'b010 for read data eye training, set to 3'b011 for read gate training, set to 3'b100 for ca training, set to 3'b101 for WDQ training.
15:10	RO	0x0	reserved
9:8	RO	0x0	pi_sw_calvl_resp_0 Indicates CA leveling response for data slice 0.
7:2	RO	0x0	reserved
1:0	RO	0x0	pi_sw_rdlvl_resp_3 Indicates read leveling response for data slice 3.

PI_REG_53
Address: Operational Base + offset (0x00d4)
DDR PHY Independent Register 53

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:24	RO	0x0	pi_sw_wdqlvl_resp_0 Indicates WDQ leveling response for data slice 0.
23:17	RO	0x0	reserved

Bit	Attr	Reset Value	Description
16	WO	0x0	pi_swlvl_rd_slice_0 Indicates software leveling read command in WDQ training for data slice 0.
15:9	RO	0x0	reserved
8	WO	0x0	pi_swlvl_wr_slice_0 Indicates software leveling write command in WDQ training for data slice 0.
7:1	RO	0x0	reserved
0	WO	0x0	pi_swlvl_exit Indicates user request to exit software leveling. Set to 1 to exit.

PI_REG_54
Address: Operational Base + offset (0x00d8)
DDR PHY Independent Register 54

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	WO	0x0	pi_swlvl_wr_slice_2 Indicates software leveling write command in WDQ training for data slice 2.
23:18	RO	0x0	reserved
17:16	RO	0x0	pi_sw_wdqlvl_resp_1 Indicates WDQ leveling response for data slice 1.
15:9	RO	0x0	reserved
8	WO	0x0	pi_swlvl_rd_slice_1 Indicates software leveling read command in WDQ training for data slice 1.
7:1	RO	0x0	reserved
0	WO	0x0	pi_swlvl_wr_slice_1 Indicates software leveling write command in WDQ training for data slice 1.

PI_REG_55
Address: Operational Base + offset (0x00dc)
DDR PHY Independent Register 55

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	WO	0x0	pi_swlvl_rd_slice_3 Indicates software leveling read command in WDQ training for data slice 3.
23:17	RO	0x0	reserved
16	WO	0x0	pi_swlvl_wr_slice_3 Indicates software leveling write command in WDQ training for data slice 3.
15:10	RO	0x0	reserved

Bit	Attr	Reset Value	Description
9:8	RO	0x0	pi_sw_wdqlvl_resp_2 Indicates WDQ leveling response for data slice 2.
7:1	RO	0x0	reserved
0	WO	0x0	pi_swlvl_rd_slice_2 Indicates software leveling read command in WDQ training for data slice 2.

PI_REG_56
Address: Operational Base + offset (0x00e0)
DDR PHY Independent Register 56

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	WO	0x0	pi_swlvl_sm2_wr Indicates software leveling write command for stage 2.
23:17	RO	0x0	reserved
16	WO	0x0	pi_swlvl_sm2_start Indicates software leveling start command for stage 2.
15	RO	0x0	reserved
14:8	RW	0x00	pi_sw_wdqlvl_vref Indicates user-defined WDQ vref value in software leveling debug mode.
7:2	RO	0x0	reserved
1:0	RO	0x0	pi_sw_wdqlvl_resp_3 Indicates WDQ leveling response for data slice 3.

PI_REG_57
Address: Operational Base + offset (0x00e4)
DDR PHY Independent Register 57

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	pi_sre_period_en Enables the selfrefresh exit-triggered periodic leveling.
23:17	RO	0x0	reserved
16	RW	0x0	pi_dfs_period_en Enables the DFS-triggered periodic leveling.
15:9	RO	0x0	reserved
8	WO	0x0	pi_sequential_lvl_req Indicates user request to initiate the leveling sequence. Set to 1 to trigger.
7:1	RO	0x0	reserved
0	WO	0x0	pi_swlvl_sm2_rd Indicates software leveling read command for stage 2.

PI_REG_58

Address: Operational Base + offset (0x00e8)
DDR PHY Independent Register 58

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x0	pi_tdfi_ctrl_delay_f1 Defines the DFI tCTRL_DELAY timing parameter (in DFI clocks), the delay between a DFI command change and a memory command. The suffix "_f1" of the parameter name is omitted when in non-DFS mode.
23:20	RO	0x0	reserved
19:16	RW	0x0	pi_tdfi_ctrl_delay_f0 Defines the DFI tCTRL_DELAY timing parameter (in DFI clocks), the delay between a DFI command change and a memory command. The suffix "_f0" of the parameter name is omitted when in non-DFS mode.
15:9	RO	0x0	reserved
8	RW	0x1	pi_16bit_dram_connect Enables 16/32bit DRAM configuration. 1'b1: 16-bit DRAM 1'b0: 32-bit DRAM
7:1	RO	0x0	reserved
0	RW	0x0	pi_dfi40_polarity Control polarity of dfi_wrdata_cs_n/dfi_rddata_cs_n generated by PI. It need match with that of controller's polarity. If controller's dfi_wrdata_cs_n/ dfi_rddata_cs_n is high active, pi_dfi40_polarity should be 1, otherwise, it should be 0. If LPDDR4 connected, it is recommended to set to 1 to match with latest DFI 4.0 protocol.

PI_REG_59
Address: Operational Base + offset (0x00ec)
DDR PHY Independent Register 59

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	pi_wldqsen Indicates delay from the issuing MRS to the first DQS strobe for write leveling.
23:18	RO	0x0	reserved
17:16	RW	0x0	pi_wrlvl_cs Specifies the target chip select for the write leveling operation that is initiated through the PI_REG_59.pi_wrlvl_req parameter.
15:9	RO	0x0	reserved
8	WO	0x0	pi_wrlvl_req Indicates user request to initiate write leveling. Set to 1 to trigger.
7:4	RO	0x0	reserved

Bit	Attr	Reset Value	Description
3:0	RW	0x0	pi_tdfi_ctrl_delay_f2 Defines the DFI tCTRL_DELAY timing parameter (in DFI clocks), the delay between a DFI command change and a memory command. The suffix "_f2" of the parameter name is omitted when in non-DFS mode.

PI_REG_60
Address: Operational Base + offset (0x00f0)
DDR PHY Independent Register 60

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	pi_wrlvl_interval Indicates the number of long count sequences that are counted between automatic write leveling commands.
15:10	RO	0x0	reserved
9:8	RW	0x0	pi_wrlvl_en Enables the PI write leveling module. Bit1 represents the support when non-initialization. Bit0 represents the support when initialization. Set to 1 to enable.
7:6	RO	0x0	reserved
5:0	RW	0x00	pi_wlmrd Indicates delay from the issuing MRS to the first write leveling strobe.

PI_REG_61
Address: Operational Base + offset (0x00f4)
DDR PHY Independent Register 61

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	pi_wrlvl_rotate Enables rotational chip select for interval write leveling. Set to 1 for rotating chip select.
23:20	RO	0x0	reserved
19:16	RW	0x0	pi_wrlvl_resp_mask Indicates mask for the dfi_wrlvl_resp signal during write leveling.
15:9	RO	0x0	reserved
8	RW	0x0	pi_wrlvl_on_sref_exit Enables automatic write leveling on a self-refresh exit. Set to 1 to enable.
7:1	RO	0x0	reserved
0	RW	0x0	pi_wrlvl_periodic Enables the use of the dfi_lvl_periodic signal during write leveling. Set to 1 to enable.

PI_REG_62
Address: Operational Base + offset (0x00f8)
DDR PHY Independent Register 62

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x00	pi_tdfi_wrlvl_en Defines the DFI tWRLVL_EN timing parameter (in DFI clocks), the minimum cycles from a dfi_wrlvl_en assertion to the first dfi_wrlvl_strobe assertion.
15:10	RO	0x0	reserved
9:8	RO	0x0	pi_wrlvl_error_status Holds the error that is associated with the write level error interrupt. Bit0 set indicates a PI_REG_65.pi_tdfi_wrlvl_max parameter violation and bit1 set indicates a PI_REG_64.pi_tdfi_wrlvl_resp parameter violation.
7:2	RO	0x0	reserved
1:0	RW	0x0	pi_wrlvl_cs_map Defines the chip select map for write leveling operations. Bit0 controls cs0, bit1 controls cs1. Set each bit to 1 to enable chip for write leveling.

PI_REG_63
Address: Operational Base + offset (0x00fc)
DDR PHY Independent Register 63

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RW	0x000	pi_tdfi_wrlvl_ww Defines the DFI tWRLVL_WW timing parameter (in DFI clocks), the minimum cycles between dfi_wrlvl_strobe assertions.

PI_REG_64
Address: Operational Base + offset (0x0100)
DDR PHY Independent Register 64

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pi_tdfi_wrlvl_resp Defines the DFI tWRLVL_RESP timing parameter (in DFI clocks), the maximum cycles between a dfi_wrlvl_req assertion and a dfi_wrlvl_en assertion.

PI_REG_65
Address: Operational Base + offset (0x0104)
DDR PHY Independent Register 65

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pi_tdfi_wrlvl_max Defines the DFI tWRLVL_MAX timing parameter (in DFI clocks), the maximum cycles between a dfi_wrlvl_en assertion and a valid dfi_wrlvl_resp.

PI_REG_66
Address: Operational Base + offset (0x0108)
DDR PHY Independent Register 66

Bit	Attr	Reset Value	Description
31:24	RW	0x00	pi_todtl_2cmd_f0 Defines the DRAM delay from an ODT de-assertion to the next non-write, non-read command. The suffix "_f0" of the parameter name is omitted when in non-DFS mode.
23:5	RO	0x0	reserved
4:0	RW	0x00	pi_wrlvl_strobe_num Defines the write leveling strobe number in LPDDR4.

PI_REG_67
Address: Operational Base + offset (0x010c)
DDR PHY Independent Register 67

Bit	Attr	Reset Value	Description
31:24	RW	0x0	pi_todtl_2cmd_f2 Defines the DRAM delay from an ODT de-assertion to the next non-write, non-read command. The suffix "_f2" of the parameter name is omitted when in non-DFS mode.
23:17	RO	0x00	reserved
16	RW	0x0	pi_odt_en_f1 Enables support of DRAM ODT. When enabled, PI asserts and de-asserts ODT output to DRAM as needed. The suffix "_f1" of the parameter name is omitted when in non-DFS mode.
15:8	RW	0x00	pi_todtl_2cmd_f1 Defines the DRAM delay from an ODT de-assertion to the next non-write, non-read command. The suffix "_f1" of the parameter name is omitted when in non-DFS mode.
7:1	RO	0x0	reserved
0	RW	0x0	pi_odt_en_f0 Enables support of DRAM ODT. When enabled, PI asserts and de-asserts ODT output to DRAM as needed. The suffix "_f0" of the parameter name is omitted when in non-DFS mode.

PI_REG_68
Address: Operational Base + offset (0x0110)
DDR PHY Independent Register 68

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved

Bit	Attr	Reset Value	Description
25:24	RW	0x0	pi_odt_rd_map_cs0 Determines the chip(s) that have termination when a read occurs on chip select 0. Set bit X to enable termination on csX when cs0 is performing a read.
23:20	RO	0x0	reserved
19:16	RW	0x0	pi_todth_rd Defines the DRAM minimum ODT high time after an ODT assertion for a read command.
15:12	RO	0x0	reserved
11:8	RW	0x0	pi_todth_wr Defines the DRAM minimum ODT high time after an ODT assertion for a write command.
7:1	RO	0x0	reserved
0	RW	0x0	pi_odt_en_f2 Enables support of DRAM ODT. When enabled, PI asserts and de-asserts ODT output to DRAM as needed. The suffix "_f2" of the parameter name is omitted when in non-DFS mode.

PI_REG_69
Address: Operational Base + offset (0x0114)
DDR PHY Independent Register 69

Bit	Attr	Reset Value	Description
31:18	RO	0x0	reserved
17:16	RW	0x0	pi_odt_wr_map_cs1 Determines the chip(s) that have termination when a write occurs on chip select 1. Set bit X to enable termination on csX when cs1 is performing a write.
15:10	RO	0x0	reserved
9:8	RW	0x0	pi_odt_rd_map_cs1 Determines the chip(s) that have termination when a read occurs on chip select 1. Set bit X to enable termination on csX when cs1 is performing a read.
7:2	RO	0x0	reserved
1:0	RW	0x0	pi_odt_wr_map_cs0 Determines the chip(s) that have termination when a write occurs on chip select 0. Set bit X to enable termination on csX when cs0 is performing a write.

PI_REG_70
Address: Operational Base + offset (0x0118)
DDR PHY Independent Register 70

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved

Bit	Attr	Reset Value	Description
24	RW	0x0	pi_en_odt_assert_except_rd Enables controller to assert ODT at all times except during reads. Assumes a single ODT pin is connected. Set to 1 to enable.
23:0	RO	0x0	reserved

PI_REG_71
Address: Operational Base + offset (0x011c)
DDR PHY Independent Register 71

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x0	pi_todton_min_f1 Defines the point in time when the device termination circuit leaves High-Z and ODT resistance begins to turn on. The suffix "_f1" of the parameter name is omitted when in non-DFS mode.
23:20	RO	0x0	reserved
19:16	RW	0x0	pi_odtlon_f1 Defines the latency from a CAS-2 command to the tODTon reference. The suffix "_f1" of the parameter name is omitted when in non-DFS mode.
15:12	RO	0x0	reserved
11:8	RW	0x0	pi_todton_min_f0 Defines the point in time when the device termination circuit leaves High-Z and ODT resistance begins to turn on. The suffix "_f0" of the parameter name is omitted when in non-DFS mode.
7:4	RO	0x0	reserved
3:0	RW	0x0	pi_odtlon_f0 Defines the latency from a CAS-2 command to the tODTon reference. The suffix "_f0" of the parameter name is omitted when in non-DFS mode.

PI_REG_72
Address: Operational Base + offset (0x0120)
DDR PHY Independent Register 72

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	pi_wr_to_odth_f1 Defines the DRAM Write command to ODT set in cycles. The suffix "_f1" of the parameter name is omitted when in non-DFS mode.
23:22	RO	0x0	reserved
21:16	RW	0x00	pi_wr_to_odth_f0 Defines the DRAM Write command to ODT set in cycles. The suffix "_f0" of the parameter name is omitted when in non-DFS mode.
15:12	RO	0x0	reserved

Bit	Attr	Reset Value	Description
11:8	RW	0x0	pi_todton_min_f2 Defines the point in time when the device termination circuit leaves High-Z and ODT resistance begins to turn on. The suffix "_f2" of the parameter name is omitted when in non-DFS mode.
7:4	RO	0x0	reserved
3:0	RW	0x0	pi_odtlon_f2 Defines the latency from a CAS-2 command to the tODTon reference. The suffix "_f2" of the parameter name is omitted when in non-DFS mode.

PI_REG_73
Address: Operational Base + offset (0x0124)
DDR PHY Independent Register 73

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	pi_rd_to_odth_f2 Defines the DRAM Read command to ODT set in cycles. The suffix "_f2" of the parameter name is omitted when in non-DFS mode.
23:22	RO	0x0	reserved
21:16	RW	0x00	pi_rd_to_odth_f1 Defines the DRAM Read command to ODT set in cycles. The suffix "_f1" of the parameter name is omitted when in non-DFS mode.
15:14	RO	0x0	reserved
13:8	RW	0x00	pi_rd_to_odth_f0 Defines the DRAM Read command to ODT set in cycles. The suffix "_f0" of the parameter name is omitted when in non-DFS mode.
7:6	RO	0x0	reserved
5:0	RW	0x00	pi_wr_to_odth_f2 Defines the DRAM Write command to ODT set in cycles. The suffix "_f2" of the parameter name is omitted when in non-DFS mode.

PI_REG_74
Address: Operational Base + offset (0x0128)
DDR PHY Independent Register 74

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:24	RW	0x0	pi_rdlvl_cs Specifies the target chip select for the data eye training operation that is initiated through the PI_REG_74.pi_rdlvl_req parameter or the gate training operation that is initiated through the PI_REG_74.pi_rdlvl_gate_req parameter.
23:17	RO	0x0	reserved
16	WO	0x0	pi_rdlvl_gate_req Indicates user request to initiate gate training. Set to 1 to trigger.
15:9	RO	0x0	reserved

Bit	Attr	Reset Value	Description
8	WO	0x0	pi_rdlvl_req Indicates user request to initiate data eye training. Set to 1 to trigger.
7:2	RO	0x0	reserved
1:0	RW	0x0	pi_address_mirroring Indicates the chip selects that support address mirroring. Bit0 controls cs0, bit1 controls cs1. Set each bit to 1 to enable.

PI_REG_75
Address: Operational Base + offset (0x012c)
DDR PHY Independent Register 75

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	pi_rdlvl_on_sref_exit Enables automatic data eye training on a self-refresh exit. Set to 1 to enable.
23:17	RO	0x0	reserved
16	RW	0x0	pi_rdlvl_periodic Enables the use of the dfi_lvl_periodic signal during data eye training. Set to 1 to enable.
15:12	RO	0x0	reserved
11:8	RW	0x0	pi_rdlvl_gate_seq_en Specifies the pattern, format and MPR for gate training.
7:4	RO	0x0	reserved
3:0	RW	0x0	pi_rdlvl_seq_en Specifies the pattern, format, and MPR for data eye training.

PI_REG_76
Address: Operational Base + offset (0x0130)
DDR PHY Independent Register 76

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	pi_rdlvl_rotate Enables rotational chip select for interval data eye training. Set to 1 for rotating CS.
23:9	RO	0x0	reserved
8	RW	0x0	pi_rdlvl_gate_on_sref_exit Enables automatic gate training on a self-refresh exit. Set to 1 to enable.
7:1	RO	0x0	reserved
0	RW	0x0	pi_rdlvl_gate_periodic Enables the use of the dfi_lvl_periodic signal during gate training. Set to 1 to enable.

PI_REG_77
Address: Operational Base + offset (0x0134)
DDR PHY Independent Register 77

Bit	Attr	Reset Value	Description
31:18	RO	0x0	reserved
17:16	RW	0x0	pi_rdlvl_gate_cs_map Defines the chip select map for gate training operations. Bit0 controls cs0, bit1 controls cs1. Set each bit to 1 to enable chip for gate training.
15:10	RO	0x0	reserved
9:8	RW	0x0	pi_rdlvl_cs_map Defines the chip select map for data eye training operations. Bit0 controls cs0, bit1 controls cs1. Set each bit to 1 to enable chip for data eye training.
7:1	RO	0x0	reserved
0	RW	0x0	pi_rdlvl_gate_rotate Enables rotational chip select for interval gate training. Set to 1 for rotating CS.

PI_REG_78
Address: Operational Base + offset (0x0138)
DDR PHY Independent Register 78

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:0	RW	0x000	pi_tdfi_rdlvl_rr Defines the DFI tRDLVL_RR timing parameter (in DFI clocks), the minimum cycles between read commands.

PI_REG_79
Address: Operational Base + offset (0x013c)
DDR PHY Independent Register 79

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pi_tdfi_rdlvl_resp Defines the DFI tRDLVL_RESP timing parameter (in DFI clocks), the maximum cycles between a dfi_rdlvl_req or dfi_rdlvl_gate_req assertion and a dfi_rdlvl_en or dfi_rdlvl_gate_en assertion.

PI_REG_80
Address: Operational Base + offset (0x0140)
DDR PHY Independent Register 80

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:24	RW	0x0	pi_rdlvl_gate_en Enables the PI gate training module. Bit1 represents the support when non-initialization. Bit0 represents the support when initialization. Set to 1 to enable.

Bit	Attr	Reset Value	Description
23:18	RO	0x0	reserved
17:16	RW	0x0	pi_rdlvl_en Enables the PI data eye training module. Bit1 represents the support when non-initialization. Bit0 represents the support when initialization. Set to 1 to enable.
15:8	RW	0x00	pi_tdfi_rdlvl_en Defines the DFI tRDLVL_EN timing parameter (in DFI clocks), the minimum cycles from a dfi_rdlvl_en or dfi_rdlvl_gate_en assertion to the first read or MRR.
7:4	RO	0x0	reserved
3:0	RW	0x0	pi_rdlvl_resp_mask Indicates mask for the dfi_rdlvl_resp signal during data eye training.

PI_REG_81
Address: Operational Base + offset (0x0144)
DDR PHY Independent Register 81

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pi_tdfi_rdlvl_max Defines the DFI tRDLVL_MAX timing parameter (in DFI clocks), the maximum cycles between a dfi_rdlvl_en or dfi_rdlvl_gate_en assertion and a valid dfi_rdlvl_resp.

PI_REG_82
Address: Operational Base + offset (0x0148)
DDR PHY Independent Register 82

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:8	RW	0x0000	pi_rdlvl_interval Indicates the number of long count sequences that are counted between automatic data eye training commands.
7:2	RO	0x0	reserved
1:0	RO	0x0	pi_rdlvl_error_status Holds the error that is associated with the data eye training error or gate training error interrupt. The uppermost bit set indicates a PI_REG_79.pi_tdfi_rdlvl_resp parameter violation. The next uppermost bit set indicates a PI_REG_81.pi_tdfi_rdlvl_max parameter violation. Lower bits are reserved.

PI_REG_83
Address: Operational Base + offset (0x014c)
DDR PHY Independent Register 83

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

Bit	Attr	Reset Value	Description
27:24	RW	0x0	pi_rdlvl_pattern_num Defines the number of patterns that are supported in read leveling.
23:20	RO	0x0	reserved
19:16	RW	0x0	pi_rdlvl_pattern_start Defines the start pattern in read leveling.
15:0	RW	0x0000	pi_rdlvl_gate_interval The number of long count sequences that are counted between automatic gate training commands.

PI_REG_84
Address: Operational Base + offset (0x0150)
DDR PHY Independent Register 84

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12:8	RW	0x00	pi_rdlvl_gate_strobe_num Defines the number of back-to-back MPC command in one read process in read gate training.
7:5	RO	0x0	reserved
4:0	RW	0x00	pi_rdlvl_strobe_num Defines the number of back to back MPC command in one read process in read eye training.

PI_REG_85
Address: Operational Base + offset (0x0154)
DDR PHY Independent Register 85

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pi_lpddr4_rdlvl_pattern_8 Indicates user-defined LPDDR4 read data pattern 8.

PI_REG_86
Address: Operational Base + offset (0x0158)
DDR PHY Independent Register 86

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pi_lpddr4_rdlvl_pattern_9 Indicates user-defined LPDDR4 read data pattern 9.

PI_REG_87
Address: Operational Base + offset (0x015c)
DDR PHY Independent Register 87

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pi_lpddr4_rdlvl_pattern_10 Indicates user-defined LPDDR4 read data pattern 10.

PI_REG_88

Address: Operational Base + offset (0x0160)
DDR PHY Independent Register 88

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pi_lpddr4_rdlvl_pattern_11 Indicates user-defined LPDDR4 read data pattern 11.

PI_REG_89
Address: Operational Base + offset (0x0164)
DDR PHY Independent Register 89

Bit	Attr	Reset Value	Description
31:24	RW	0x00	pi_rdlvl_adj_f1 Indicates the adjustment value for PHY read timing. The suffix "_f1" of the parameter name is omitted when in non-DFS mode.
23:16	RW	0x00	pi_rdlvl_adj_f0 Indicates the adjustment value for PHY read timing. The suffix "_f0" of the parameter name is omitted when in non-DFS mode.
15:9	RO	0x0	reserved
8	RW	0x0	pi_reg_dimm_enable Enables registered DIMM operation. Set to 1 to enable.
7:1	RO	0x0	reserved
0	RW	0x0	pi_rd_preamble_training_en Enables read preamble training during data eye training. Set to 1 to enable.

PI_REG_90
Address: Operational Base + offset (0x0168)
DDR PHY Independent Register 90

Bit	Attr	Reset Value	Description
31:24	RW	0x00	pi_wrlat_adj_f1 Indicates the adjustment value for PHY write timing. The suffix "_f1" of the parameter name is omitted when in non-DFS mode.
23:16	RW	0x00	pi_wrlat_adj_f0 Indicates the adjustment value for PHY write timing. The suffix "_f0" of the parameter name is omitted when in non-DFS mode.
15:8	RO	0x00	pi_tdfi_rddata_en Holds the calculated DFI tRDDATA_EN timing parameter (in DFI PHY clocks), the maximum cycles between a read command and a dfi_rddata_en assertion.
7:0	RW	0x00	pi_rdlvl_adj_f2 Indicates the adjustment value for PHY read timing. The suffix "_f2" of the parameter name is omitted when in non-DFS mode.

PI_REG_91
Address: Operational Base + offset (0x016c)
DDR PHY Independent Register 91

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:24	RW	0x00	pi_tdfi_wrcslat_f1 Defines the DFI tPHY_WRCSLAT timing parameter (in DFI PHY clocks), the maximum cycles between a write command and a dfi_wrdata_cs_n assertion. The suffix "_f1" of the parameter name is omitted when in non-DFS mode.
23:16	RW	0x00	pi_tdfi_wrcslat_f0 Defines the DFI tPHY_WRCSLAT timing parameter (in DFI PHY clocks), the maximum cycles between a write command and a dfi_wrdata_cs_n assertion. The suffix "_f0" of the parameter name is omitted when in non-DFS mode.
15:8	RO	0x00	pi_tdfi_phy_wrlat Holds the calculated DFI tPHY_WRLAT timing parameter (in DFI PHY clocks), the maximum cycles between a write command and a dfi_wrdata_en assertion.
7:0	RW	0x00	pi_wrlat_adj_f2 Indicates the adjustment value for PHY write timing. The suffix "_f2" of the parameter name is omitted when in non-DFS mode.

PI_REG_92
Address: Operational Base + offset (0x0170)
DDR PHY Independent Register 92

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:24	RW	0x0	pi_calvl_cs Specifies the target chip select for the CA training operation that is initiated through the PI_REG_92.pi_calvl_req parameter.
23:17	RO	0x0	reserved
16	WO	0x0	pi_calvl_req Indicates user request to initiate CA training. Set to 1 to trigger.
15:11	RO	0x0	reserved
10:8	RW	0x0	pi_tdfi_phy_wrdata Defines the DFI tPHY_WRDATA timing parameter (in DFI PHY clocks), the maximum cycles between a dfi_wrdata_en assertion and a dfi_wrdata signal.
7:0	RW	0x00	pi_tdfi_wrcslat_f2 Defines the DFI tPHY_WRCSLAT timing parameter (in DFI PHY clocks), the maximum cycles between a write command and a dfi_wrdata_cs_n assertion. The suffix "_f2" of the parameter name is omitted when in non-DFS mode.

PI_REG_93
Address: Operational Base + offset (0x0174)
DDR PHY Independent Register 93

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved

Bit	Attr	Reset Value	Description
24	RW	0x0	pi_calvl_periodic Enables the use of the dfi_lvl_periodic signal during CA training. Set to 1 to enable.
23:18	RO	0x0	reserved
17:16	RW	0x0	pi_calvl_seq_en Specifies the CA training patterns that are to be used. Set to 0 for pattern 0 only, set to 1 for patterns 0 and 1, set to 2 for patterns 0, 1, and 2, or set to 3 for all patterns.
15:0	RO	0x0	reserved

PI_REG_94
Address: Operational Base + offset (0x0178)
DDR PHY Independent Register 94

Bit	Attr	Reset Value	Description
31:24	RW	0x00	pi_tdfi_calvl_en Defines the DFI tCALVL_EN timing parameter (in DFI clocks), the minimum cycles between a dfi_calvl_en assertion and a dfi_cke de-assertion.
23:18	RO	0x0	reserved
17:16	RW	0x0	pi_calvl_cs_map Defines the chip select map for CA training operations. Bit0 controls cs0, bit1 controls cs1. Set each bit to 1 to enable chip for CA training.
15:9	RO	0x0	reserved
8	RW	0x0	pi_calvl_rotate Enables rotational chip select for interval CA training. Set to 1 for rotating CS.
7:1	RO	0x0	reserved
0	RW	0x0	pi_calvl_on_sref_exit Enables automatic CA training on a self-refresh exit. Set to 1 to enable.

PI_REG_95
Address: Operational Base + offset (0x017c)
DDR PHY Independent Register 95

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RW	0x000	pi_tdfi_calvl_capture_f0 Defines the DFI tCALVL_CAPTURE timing parameter (in DFI clocks), the minimum cycles between a calibration command and a dfi_calvl_capture pulse. The suffix "_f0" of the parameter name is omitted when in non-DFS mode.
15:10	RO	0x0	reserved

Bit	Attr	Reset Value	Description
9:0	RW	0x000	pi_tdfi_calvl_cc_f0 Defines the DFI tCALVL_CC timing parameter (in DFI clocks), the minimum cycles between calibration commands. The suffix "_f0" of the parameter name is omitted when in non-DFS mode.

PI_REG_96
Address: Operational Base + offset (0x0180)
DDR PHY Independent Register 96

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RW	0x000	pi_tdfi_calvl_capture_f1 Defines the DFI tCALVL_CAPTURE timing parameter (in DFI clocks), the minimum cycles between a calibration command and a dfi_calvl_capture pulse. The suffix "_f1" of the parameter name is omitted when in non-DFS mode.
15:10	RO	0x0	reserved
9:0	RW	0x000	pi_tdfi_calvl_cc_f1 Defines the DFI tCALVL_CC timing parameter (in DFI clocks), the minimum cycles between calibration commands. The suffix "_f1" of the parameter name is omitted when in non-DFS mode.

PI_REG_97
Address: Operational Base + offset (0x0184)
DDR PHY Independent Register 97

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RW	0x000	pi_tdfi_calvl_capture_f2 Defines the DFI tCALVL_CAPTURE timing parameter (in DFI clocks), the minimum cycles between a calibration command and a dfi_calvl_capture pulse. The suffix "_f2" of the parameter name is omitted when in non-DFS mode.
15:10	RO	0x0	reserved
9:0	RW	0x000	pi_tdfi_calvl_cc_f2 Defines the DFI tCALVL_CC timing parameter (in DFI clocks), the minimum cycles between calibration commands. The suffix "_f2" of the parameter name is omitted when in non-DFS mode.

PI_REG_98
Address: Operational Base + offset (0x0188)
DDR PHY Independent Register 98

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pi_tdfi_calvl_resp Defines the DFI tCALVL_RESP timing parameter (in DFI clocks), the maximum cycles between a dfi_calvl_req assertion and a dfi_calvl_en assertion.

PI_REG_99
Address: Operational Base + offset (0x018c)
DDR PHY Independent Register 99

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pi_tdfi_calvl_max Defines the DFI tCALVL_MAX timing parameter (in DFI clocks), the maximum cycles between a dfi_calvl_en assertion and a valid dfi_calvl_resp.

PI_REG_100
Address: Operational Base + offset (0x0190)
DDR PHY Independent Register 100

Bit	Attr	Reset Value	Description
31:18	RO	0x0	reserved
17:16	RO	0x0	pi_calvl_error_status Holds the error that is associated with the CA training error interrupt. Bit0 set indicates a PI_REG_98.pi_tdfi_calvl_resp parameter violation and bit1 set indicates a PI_REG_99.pi_tdfi_calvl_max parameter violation.
15:10	RO	0x0	reserved
9:8	RW	0x0	pi_calvl_en Enables the PI CA training module. Bit1 represents the support when non-initialization. Bit0 represents the support when initialization. Set to 1 to enable.
7:1	RO	0x0	reserved
0	RW	0x0	pi_calvl_resp_mask Indicates mask for the dfi_calvl_resp signal during CA training.

PI_REG_101
Address: Operational Base + offset (0x0194)
DDR PHY Independent Register 101

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	pi_tcamrd Indicates DRAM TCAMRD value in cycles.
23:21	RO	0x0	reserved
20:16	RW	0x00	pi_tcackel Indicates DRAM TCACKEL value in cycles.
15:0	RW	0x0000	pi_calvl_interval Indicates the number of long count sequences that is counted between automatic CA training commands.

PI_REG_102
Address: Operational Base + offset (0x0198)
DDR PHY Independent Register 102

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:16	RW	0x0000	pi_tcaent_f0 Indicates DRAM TCAENT value in cycles. The suffix "_f0" of the parameter name is omitted when in non-DFS mode.
15:13	RO	0x0	reserved
12:8	RW	0x00	pi_tmrz_f0 Indicates DRAM TMRZ value in cycles. The suffix "_f0" of the parameter name is omitted when in non-DFS mode.
7:5	RO	0x0	reserved
4:0	RW	0x00	pi_tcackeh Indicates DRAM TCACKEH value in cycles.

PI_REG_103
Address: Operational Base + offset (0x019c)
DDR PHY Independent Register 103

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x00	pi_tmrz_f2 Indicates DRAM TMRZ value in cycles. The suffix "_f2" of the parameter name is omitted when in non-DFS mode.
23:22	RO	0x0	reserved
21:8	RW	0x0000	pi_tcaent_f1 Indicates DRAM TCAENT value in cycles. The suffix "_f1" of the parameter name is omitted when in non-DFS mode.
7:5	RO	0x0	reserved
4:0	RW	0x00	pi_tmrz_f1 Indicates DRAM TMRZ value in cycles. The suffix "_f1" of the parameter name is omitted when in non-DFS mode.

PI_REG_104
Address: Operational Base + offset (0x01a0)
DDR PHY Independent Register 104

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	pi_ca_train_vref_en Indicates whether to do VREF training during non-power-on-initial CA training or not. Set to 1 to go through the VREF from start-point for non-power-on-initial CA training. Set to 0 to not update VREF for non-power-on-initial CA training.
23:21	RO	0x0	reserved
20:16	RW	0x00	pi_tcaext Indicates DRAM TCAEXT value in cycles.
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13:0	RW	0x0000	pi_tcaent_f2 Indicates DRAM TCAENT value in cycles. The suffix "_f2" of the parameter name is omitted when in non-DFS mode.

PI_REG_105
Address: Operational Base + offset (0x01a4)
DDR PHY Independent Register 105

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RW	0x000	pi_tvref_short_f0 Indicates delay from dfi_calvl_strobe to next CMD (only param_calvl_vref_stepsize change of the VREF). The suffix "_f0" of the parameter name is omitted when in non-DFS mode.
15:13	RO	0x0	reserved
12:8	RW	0x00	pi_tdfi_casel_f0 Indicates DFI tcalvl_ca_sel timing parameter. The suffix "_f0" of the parameter name is omitted when in non-DFS mode.
7:5	RO	0x0	reserved
4:0	RW	0x00	pi_tdfi_cacsca_f0 Indicates DFI tcalvl_cs_ca timing parameter. The suffix "_f0" of the parameter name is omitted when in non-DFS mode.

PI_REG_106
Address: Operational Base + offset (0x01a8)
DDR PHY Independent Register 106

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:24	RW	0x00	pi_tdfi_casel_f1 Indicates DFI tcalvl_ca_sel timing parameter. The suffix "_f1" of the parameter name is omitted when in non-DFS mode.
23:21	RO	0x0	reserved
20:16	RW	0x00	pi_tdfi_cacsca_f1 Indicates DFI tcalvl_cs_ca timing parameter. The suffix "_f1" of the parameter name is omitted when in non-DFS mode.
15:10	RO	0x0	reserved
9:0	RW	0x000	pi_tvref_long_f0 Indicates delay from dfi_calvl_strobe to next CMD (more than one param_calvl_vref_stepsize Vref change). The suffix "_f0" of the parameter name is omitted when in non-DFS mode.

PI_REG_107
Address: Operational Base + offset (0x01ac)
DDR PHY Independent Register 107

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved

Bit	Attr	Reset Value	Description
25:16	RW	0x000	pi_tvref_long_f1 Indicates delay from dfi_calvl_strobe to next CMD (more than one param_calvl_vref_stepsize Vref change). The suffix "_f1" of the parameter name is omitted when in non-DFS mode.
15:10	RO	0x0	reserved
9:0	RW	0x000	pi_tvref_short_f1 Indicates delay from dfi_calvl_strobe to next CMD (only param_calvl_vref_stepsize change of the VREF). The suffix "_f1" of the parameter name is omitted when in non-DFS mode.

PI_REG_108
Address: Operational Base + offset (0x01b0)
DDR PHY Independent Register 108

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RW	0x000	pi_tvref_short_f2 Indicates delay from dfi_calvl_strobe to next CMD (only param_calvl_vref_stepsize change of the VREF). The suffix "_f2" of the parameter name is omitted when in non-DFS mode.
15:13	RO	0x0	reserved
12:8	RW	0x00	pi_tdfi_casel_f2 Indicates DFI tcalvl_ca_sel timing parameter. The suffix "_f2" of the parameter name is omitted when in non-DFS mode.
7:5	RO	0x0	reserved
4:0	RW	0x00	pi_tdfi_cacsca_f2 Indicates DFI tcalvl_cs_ca timing parameter. The suffix "_f2" of the parameter name is omitted when in non-DFS mode.

PI_REG_109
Address: Operational Base + offset (0x01b4)
DDR PHY Independent Register 109

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	pi_calvl_vref_initial_stop_point Indicates the end point of VREF for the Vref(ca) training vrefca_range, vref_ca_setting[5:0]
23	RO	0x0	reserved
22:16	RW	0x00	pi_calvl_vref_initial_start_point Indicates the start point of VREF for the Vref (ca) training vrefca_range, vref_ca_setting[5:0].
15:10	RO	0x0	reserved
9:0	RW	0x000	pi_tvref_long_f2 Indicates delay from dfi_calvl_strobe to next CMD (more than one param_calvl_vref_stepsize Vref change). The suffix "_f2" of the parameter name is omitted when in non-DFS mode.

PI_REG_110
Address: Operational Base + offset (0x01b8)
DDR PHY Independent Register 110

Bit	Attr	Reset Value	Description
31:24	RW	0x00	pi_tdfi_init_start_min Indicates the minimum number of DFI clocks before dfi_init_start can be driven after a previous command or training event.
23:20	RO	0x0	reserved
19:16	RW	0x0	pi_calvl_vref_delta Indicates the CA VREF adjustment for non-initial CA training.
15:12	RO	0x0	reserved
11:8	RW	0x0	pi_calvl_vref_normal_stepsize Indicates the adjust step for the Vref(ca) training.
7:4	RO	0x0	reserved
3:0	RW	0x0	pi_calvl_vref_initial_stepsize Indicates the adjust step for the Vref(ca) training.

PI_REG_111
Address: Operational Base + offset (0x01bc)
DDR PHY Independent Register 111

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x0	pi_tdfi_calvl_strobe_f2 Indicates data setup for VREF training mode. The suffix "_f2" of the parameter name is omitted when in non-DFS mode.
23:20	RO	0x0	reserved
19:16	RW	0x0	pi_tdfi_calvl_strobe_f1 Indicates data setup for VREF training mode. The suffix "_f1" of the parameter name is omitted when in non-DFS mode.
15:12	RO	0x0	reserved
11:8	RW	0x0	pi_tdfi_calvl_strobe_f0 Indicates data setup for VREF training mode. The suffix "_f0" of the parameter name is omitted when in non-DFS mode.
7:0	RW	0x00	pi_tdfi_init_complete_min Indicates the minimum number of DFI clocks from dfi_init_complete to a command or training event.

PI_REG_112
Address: Operational Base + offset (0x01c0)
DDR PHY Independent Register 112

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:24	RW	0x00	pi_tdfi_init_start_f0 Defines the DFI tINIT_START timing parameter (in DFI clocks), the maximum number or cycles between a dfi_init_start assertion and a dfi_init_complete de-assertion from the PHY. The suffix "_f0" of the parameter name is omitted when in non-DFS mode.
23	RO	0x0	reserved
22:16	RW	0x00	pi_sw_ca_train_vref Indicates the VREF value, which is set for software step-by-step CA training.
15:13	RO	0x0	reserved
12:8	RW	0x00	pi_calvl_strobe_num Indicates the consecutive dfi_calvl_strobe number when updating the CA VREF data.
7:4	RO	0x0	reserved
3:0	RW	0x0	pi_tckckeh Indicates clock and command are valid before CKE HIGH.

PI_REG_113
Address: Operational Base + offset (0x01c4)
DDR PHY Independent Register 113

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x00	pi_tdfi_init_start_f1 Defines the DFI tINIT_START timing parameter (in DFI clocks), the maximum number or cycles between a dfi_init_start assertion and a dfi_init_complete de-assertion from the PHY. The suffix "_f1" of the parameter name is omitted when in non-DFS mode.
15:0	RW	0x0000	pi_tdfi_init_complete_f0 Defines the DFI tINIT_COMPLETE timing parameter (in DFI clocks), the maximum cycles between a dfi_init_start de-assertion and a dfi_init_complete assertion from the PHY. The suffix "_f0" of the parameter name is omitted when in non-DFS mode

PI_REG_114
Address: Operational Base + offset (0x01c8)
DDR PHY Independent Register 114

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x00	pi_tdfi_init_start_f2 Defines the DFI tINIT_START timing parameter (in DFI clocks), the maximum number or cycles between a dfi_init_start assertion and a dfi_init_complete de-assertion from the PHY. The suffix "_f2" of the parameter name is omitted when in non-DFS mode.

Bit	Attr	Reset Value	Description
15:0	RW	0x0000	pi_tdfi_init_complete_f1 Defines the DFI tINIT_COMPLETE timing parameter (in DFI clocks), the maximum cycles between a dfi_init_start de-assertion and a dfi_init_complete assertion from the PHY. The suffix "_f1" of the parameter name is omitted when in non-DFS mode

PI_REG_115
Address: Operational Base + offset (0x01cc)
DDR PHY Independent Register 115

Bit	Attr	Reset Value	Description
31:24	RW	0x00	pi_init_startorcomplete_2_clkdisable Defines the delay from deasserting of dfi_init_start or asserting of dfi_init_complete to deasserting of dfi_dram_clk_disable in DFI clock.
23:16	RW	0x00	pi_clkdisable_2_init_start Defines the delay from the asserting of dfi_dram_clk_disable to the asserting of dfi_init_start in DFI clock.
15:0	RW	0x0000	pi_tdfi_init_complete_f2 Defines the DFI tINIT_COMPLETE timing parameter (in DFI clocks), the maximum cycles between a dfi_init_start de-assertion and a dfi_init_complete assertion from the PHY. The suffix "_f2" of the parameter name is omitted when in non-DFS mode

PI_REG_116
Address: Operational Base + offset (0x01d0)
DDR PHY Independent Register 116

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29:24	RW	0x00	pi_tckehdqs_f1 Indicates the DRAM timing TCKEHDQS, minimum delay from CKE high to strobe high impedance. The suffix "_f1" of the parameter name is omitted when in non-DFS mode.
23:22	RO	0x0	reserved
21:16	RW	0x00	pi_tckehdqs_f0 Indicates the DRAM timing TCKEHDQS, minimum delay from CKE high to strobe high impedance. The suffix "_f0" of the parameter name is omitted when in non-DFS mode.
15:9	RO	0x0	reserved
8	RW	0x0	pi_refresh_between_segment_disable Disables the refresh between CA first and second segment training. Defaut is set to 1.
7:1	RO	0x0	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	pi_dram_clk_disable_deassert_sel Indicates dfi_dram_clk_disable deassert following dfi_init_start deassert or dfi_init_complete assert. 1'b0: dfi_dram_clk_disable deassert following dfi_init_start deassert. 1'b1: dfi_dram_clk_disable deassert following dfi_init_complete assert.

PI_REG_117
Address: Operational Base + offset (0x01d4)
DDR PHY Independent Register 117

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:16	RW	0x0	pi_wdqlvl_bst_num Indicates burst number for MPC, the maximum FIFO for LPDDR4 is 5.
15:9	RO	0x0	reserved
8	RW	0x0	pi_wdqlvl_vref_en Indicates whether to do VREF training for non-initial WDQ leveling
7:6	RO	0x0	reserved
5:0	RW	0x00	pi_tckehdqs_f2 Indicates the DRAM timing TCKEHDQS, minimum delay from CKE high to strobe high impedance. The suffix "_f2" of the parameter name is omitted when in non-DFS mode.

PI_REG_118
Address: Operational Base + offset (0x01d8)
DDR PHY Independent Register 118

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RW	0x000	pi_tdfi_wdqlvl_rw Switches time from read to write.
15:10	RO	0x0	reserved
9:0	RW	0x000	pi_tdfi_wdqlvl_wr Switches time from write to read.

PI_REG_119
Address: Operational Base + offset (0x01dc)
DDR PHY Independent Register 119

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:24	RW	0x00	pi_wdqlvl_vref_initial_start_point Indicates write DQ training VREF start value.
23:18	RO	0x0	reserved

Bit	Attr	Reset Value	Description
17:16	RW	0x0	pi_wdqlvl_cs_map Indicates map of chip selects that are included in write DQ training sequence.
15:9	RO	0x0	reserved
8	RW	0x0	pi_wdqlvl_rotate Enables write DQ training rotate for periodic training.
7:4	RO	0x0	reserved
3:0	RW	0x0	pi_wdqlvl_resp_mask Indicates write DQ training response mask.

PI_REG_120
Address: Operational Base + offset (0x01e0)
DDR PHY Independent Register 120

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:24	RW	0x0	pi_wdqlvl_vref_delta Indicates the WDQ VREF adjustment for non-initial WDQ training.
23:21	RO	0x0	reserved
20:16	RW	0x00	pi_wdqlvl_verf_normal_stepsize Indicates write DQ training VREF step size.
15:13	RO	0x0	reserved
12:8	RW	0x00	pi_wdqlvl_vref_initial_stepsize Indicates write DQ training VREF step size.
7	RO	0x0	reserved
6:0	RW	0x00	pi_wdqlvl_vref_initial_stop_point Indicates write DQ training VREF stop value.

PI_REG_121
Address: Operational Base + offset (0x01e4)
DDR PHY Independent Register 121

Bit	Attr	Reset Value	Description
31:24	RW	0x00	pi_tdfi_wdqlvl_en Indicates DFI timing param - enable to FIFO write.
23:18	RO	0x0	reserved
17:16	RW	0x0	pi_wdqlvl_cs Indicates write DQ training target chip select.
15:9	RO	0x0	reserved
8	WO	0x0	pi_wdqlvl_req Indicates software write DQ training request.
7:1	RO	0x0	reserved
0	RW	0x0	pi_wdqlvl_periodic Enables write DQ training periodic.

PI_REG_122

Address: Operational Base + offset (0x01e8)
DDR PHY Independent Register 122

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pi_tdfi_wdqlvl_resp Indicates DFI timing param - req to enable.

PI_REG_123
Address: Operational Base + offset (0x01ec)
DDR PHY Independent Register 123

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pi_tdfi_wdqlvl_max Indicates DFI timing param - max enable to resp (PHY eval).

PI_REG_124
Address: Operational Base + offset (0x01f0)
DDR PHY Independent Register 124

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	pi_wdqlvl_on_sref_exit Issues a write DQ training command on self-refresh exit.
23:18	RO	0x0	reserved
17:16	RW	0x0	pi_wdqlvl_en Indicates if write DQ leveling is enabled. Bit1 represents the support when non-initialization. Bit0 represents the support when initialization.
15:0	RW	0x0000	pi_wdqlvl_interval Indicates write DQ train interval counter program value.

PI_REG_125
Address: Operational Base + offset (0x01f4)
DDR PHY Independent Register 125

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:8	RW	0x0000	pi_mr1_data_f0_0 Indicates data to program into memory mode register 1 for chip select 0. The suffix "_f0" of the parameter name is omitted when in non-DFS mode.
7:2	RO	0x0	reserved
1:0	RO	0x0	pi_wdqlvl_error_status Holds the error associated with the write DQ level error interrupt. Bit0 set indicates a PI_REG_123.pi_tdfi_wdqlvl_max parameter violation and bit1 set indicates a PI_REG_122.pi_tdfi_wdqlvl_resp parameter violation.

PI_REG_126
Address: Operational Base + offset (0x01f8)

DDR PHY Independent Register 126

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	pi_mr3_data_f0_0 Indicates data to program into memory mode register 3 for chip select 0. The suffix "_f0" of the parameter name is omitted when in non-DFS mode.
15:0	RW	0x0000	pi_mr2_data_f0_0 Indicates data to program into memory mode register 2 for chip select 0. The suffix "_f0" of the parameter name is omitted when in non-DFS mode.

PI_REG_127
Address: Operational Base + offset (0x01fc)
DDR PHY Independent Register 127

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x00	pi_mr14_data_f0_0 Indicates data to program into memory mode register 14 for chip select 0. The suffix "_f0" of the parameter name is omitted when in non-DFS mode.
15:8	RW	0x00	pi_mr12_data_f0_0 Indicates data to program into memory mode register 12 for chip select 0. The suffix "_f0" of the parameter name is omitted when in non-DFS mode.
7:0	RW	0x00	pi_mr11_data_f0_0 Indicates data to program into memory mode register 11 for chip select 0. The suffix "_f0" of the parameter name is omitted when in non-DFS mode.

PI_REG_128
Address: Operational Base + offset (0x0200)
DDR PHY Independent Register 128

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	pi_mr2_data_f1_0 Indicates data to program into memory mode register 2 for chip select 0. The suffix "_f1" of the parameter name is omitted when in non-DFS mode.
15:0	RW	0x0000	pi_mr1_data_f1_0 Indicates data to program into memory mode register 1 for chip select 0. The suffix "_f1" of the parameter name is omitted when in non-DFS mode.

PI_REG_129
Address: Operational Base + offset (0x0204)
DDR PHY Independent Register 129

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:24	RW	0x00	pi_mr12_data_f1_0 Indicates data to program into memory mode register 12 for chip select 0. The suffix "_f1" of the parameter name is omitted when in non-DFS mode.
23:16	RW	0x00	pi_mr11_data_f1_0 Indicates data to program into memory mode register 11 for chip select 0. The suffix "_f1" of the parameter name is omitted when in non-DFS mode.
15:0	RW	0x0000	pi_mr3_data_f1_0 Indicates data to program into memory mode register 3 for chip select 0. The suffix "_f1" of the parameter name is omitted when in non-DFS mode.

PI_REG_130
Address: Operational Base + offset (0x0208)
DDR PHY Independent Register 130

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:8	RW	0x0000	pi_mr1_data_f2_0 Indicates data to program into memory mode register 1 for chip select 0. The suffix "_f2" of the parameter name is omitted when in non-DFS mode.
7:0	RW	0x00	pi_mr14_data_f1_0 Indicates data to program into memory mode register 14 for chip select 0. The suffix "_f1" of the parameter name is omitted when in non-DFS mode.

PI_REG_131
Address: Operational Base + offset (0x020c)
DDR PHY Independent Register 131

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	pi_mr3_data_f2_0 Indicates data to program into memory mode register 3 for chip select 0. The suffix "_f2" of the parameter name is omitted when in non-DFS mode.
15:0	RW	0x0000	pi_mr2_data_f2_0 Indicates data to program into memory mode register 2 for chip select 0. The suffix "_f2" of the parameter name is omitted when in non-DFS mode.

PI_REG_132
Address: Operational Base + offset (0x0210)
DDR PHY Independent Register 132

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:24	RW	0x00	pi_mr13_data_0 Indicates data to program into memory mode register 13 for chip select 0.
23:16	RW	0x00	pi_mr14_data_f2_0 Indicates data to program into memory mode register 14 for chip select 0. The suffix "_f2" of the parameter name is omitted when in non-DFS mode.
15:8	RW	0x00	pi_mr12_data_f2_0 Indicates data to program into memory mode register 12 for chip select 0. The suffix "_f2" of the parameter name is omitted when in non-DFS mode.
7:0	RW	0x00	pi_mr11_data_f2_0 Indicates data to program into memory mode register 11 for chip select 0. The suffix "_f2" of the parameter name is omitted when in non-DFS mode.

PI_REG_133
Address: Operational Base + offset (0x0214)
DDR PHY Independent Register 133

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	pi_mr2_data_f0_1 Indicates data to program into memory mode register 2 for chip select 1. The suffix "_f0" of the parameter name is omitted when in non-DFS mode.
15:0	RW	0x0000	pi_mr1_data_f0_1 Indicates data to program into memory mode register 1 for chip select 1. The suffix "_f0" of the parameter name is omitted when in non-DFS mode.

PI_REG_134
Address: Operational Base + offset (0x0218)
DDR PHY Independent Register 134

Bit	Attr	Reset Value	Description
31:24	RW	0x00	pi_mr12_data_f0_1 Indicates data to program into memory mode register 12 for chip select 1. The suffix "_f0" of the parameter name is omitted when in non-DFS mode.
23:16	RW	0x00	pi_mr11_data_f0_1 Indicates data to program into memory mode register 11 for chip select 1. The suffix "_f0" of the parameter name is omitted when in non-DFS mode.
15:0	RW	0x0000	pi_mr3_data_f0_1 Indicates data to program into memory mode register 3 for chip select 1. The suffix "_f0" of the parameter name is omitted when in non-DFS mode.

PI_REG_135
Address: Operational Base + offset (0x021c)
DDR PHY Independent Register 135

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:8	RW	0x0000	pi_mr1_data_f1_1 Indicates data to program into memory mode register 1 for chip select 1. The suffix "_f1" of the parameter name is omitted when in non-DFS mode.
7:0	RW	0x00	pi_mr14_data_f0_1 Indicates data to program into memory mode register 14 for chip select 1. The suffix "_f0" of the parameter name is omitted when in non-DFS mode.

PI_REG_136
Address: Operational Base + offset (0x0220)
DDR PHY Independent Register 136

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	pi_mr3_data_f1_1 Indicates data to program into memory mode register 3 for chip select 1. The suffix "_f1" of the parameter name is omitted when in non-DFS mode.
15:0	RW	0x0000	pi_mr2_data_f1_1 Indicates data to program into memory mode register 2 for chip select 1. The suffix "_f1" of the parameter name is omitted when in non-DFS mode.

PI_REG_137
Address: Operational Base + offset (0x0224)
DDR PHY Independent Register 137

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x00	pi_mr14_data_f1_1 Indicates data to program into memory mode register 14 for chip select 1. The suffix "_f1" of the parameter name is omitted when in non-DFS mode.
15:8	RW	0x00	pi_mr12_data_f1_1 Indicates data to program into memory mode register 12 for chip select 1. The suffix "_f1" of the parameter name is omitted when in non-DFS mode.
7:0	RW	0x00	pi_mr11_data_f1_1 Indicates data to program into memory mode register 11 for chip select 1. The suffix "_f1" of the parameter name is omitted when in non-DFS mode.

PI_REG_138
Address: Operational Base + offset (0x0228)
DDR PHY Independent Register 138

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	pi_mr2_data_f2_1 Indicates data to program into memory mode register 2 for chip select 1. The suffix "_f2" of the parameter name is omitted when in non-DFS mode.
15:0	RW	0x0000	pi_mr1_data_f2_1 Indicates data to program into memory mode register 1 for chip select 1. The suffix "_f2" of the parameter name is omitted when in non-DFS mode.

PI_REG_139
Address: Operational Base + offset (0x022c)
DDR PHY Independent Register 139

Bit	Attr	Reset Value	Description
31:24	RW	0x00	pi_mr12_data_f2_1 Indicates data to program into memory mode register 12 for chip select 1. The suffix "_f2" of the parameter name is omitted when in non-DFS mode.
23:16	RW	0x00	pi_mr11_data_f2_1 Indicates data to program into memory mode register 11 for chip select 1. The suffix "_f2" of the parameter name is omitted when in non-DFS mode.
15:0	RW	0x0000	pi_mr3_data_f2_1 Indicates data to program into memory mode register 3 for chip select 1. The suffix "_f2" of the parameter name is omitted when in non-DFS mode.

PI_REG_140
Address: Operational Base + offset (0x0230)
DDR PHY Independent Register 140

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:8	RW	0x00	pi_mr13_data_1 Indicates data to program into memory mode register 13 for chip select 0.
7:0	RW	0x00	pi_mr14_data_f2_1 Indicates data to program into memory mode register 14 for chip select 1. The suffix "_f2" of the parameter name is omitted when in non-DFS mode.

PI_REG_155
Address: Operational Base + offset (0x026c)
DDR PHY Independent Register 155

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:24	RW	0x0	pi_row_diff Indicates the difference between the number of address pins available and the number being used.
23:18	RO	0x0	reserved
17:16	RW	0x0	pi_bank_diff Indicates encoded number of banks on the DRAM(s).
15:0	RO	0x0	reserved

PI_REG_156
Address: Operational Base + offset (0x0270)
DDR PHY Independent Register 156

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:16	RW	0x000	pi_tfc_f1 Indicates the delay in PHY clock cycles from setting MR13.OP7 to any valid command. The suffix "_f1" of the parameter name is omitted when in non-DFS mode.
15:10	RO	0x0	reserved
9:0	RW	0x000	pi_tfc_f0 Indicates the delay in PHY clock cycles from setting MR13.OP7 to any valid command. The suffix "_f0" of the parameter name is omitted when in non-DFS mode.

PI_REG_157
Address: Operational Base + offset (0x0274)
DDR PHY Independent Register 157

Bit	Attr	Reset Value	Description
31:24	RW	0x00	pi_trtp_f0 Indicates DRAM TRTP value in cycles. The suffix "_f0" of the parameter name is omitted when in non-DFS mode.
23:21	RO	0x0	reserved
20:16	RW	0x00	pi_tccd Indicates DRAM CAS-to-CAS value in cycles.
15:10	RO	0x0	reserved
9:0	RW	0x000	pi_tfc_f2 Indicates the delay in PHY clock cycles from setting MR13.OP7 to any valid command. The suffix "_f2" of the parameter name is omitted when in non-DFS mode.

PI_REG_158
Address: Operational Base + offset (0x0278)
DDR PHY Independent Register 158

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

Bit	Attr	Reset Value	Description
29:24	RW	0x00	pi_twr_f0 Indicates DRAM TWR value in cycles. The suffix "_f0" of the parameter name is omitted when in non-DFS mode.
23:22	RO	0x0	reserved
21:16	RW	0x00	pi_twtr_f0 Indicates DRAM TWTR value in cycles. The suffix "_f0" of the parameter name is omitted when in non-DFS mode.
15:8	RW	0x00	pi_trcd_f0 Indicates DRAM TRCD value in cycles. The suffix "_f0" of the parameter name is omitted when in non-DFS mode.
7:0	RW	0x00	pi_trp_f0 Indicates DRAM TRP value in cycles. The suffix "_f0" of the parameter name is omitted when in non-DFS mode.

PI_REG_159
Address: Operational Base + offset (0x027c)
DDR PHY Independent Register 159

Bit	Attr	Reset Value	Description
31:24	RW	0x00	pi_tras_min_f0 Indicates DRAM TRAS_MIN value in cycles. The suffix "_f0" of the parameter name is omitted when in non-DFS mode.
23:17	RO	0x0	reserved
16:0	RW	0x00000	pi_tras_max_f0 Indicates DRAM TRAS_MAX value in cycles. The suffix "_f0" of parameter name will be omitted when non DFS mode.

PI_REG_160
Address: Operational Base + offset (0x0280)
DDR PHY Independent Register 160

Bit	Attr	Reset Value	Description
31:24	RW	0x00	pi_tmrw_f0 Indicates DRAM TMRW value in cycles. The suffix "_f0" of the parameter name is omitted when in non-DFS mode.
23:22	RO	0x0	reserved
21:16	RW	0x00	pi_tmrd_f0 Indicates DRAM TMRD value in cycles. The suffix "_f0" of the parameter name is omitted when in non-DFS mode.
15:14	RO	0x0	reserved
13:8	RW	0x00	pi_tccdmw_f0 Indicates LPDDR4 DRAM TCCDMW in cycles. The suffix "_f0" of the parameter name is omitted when in non-DFS mode.
7:4	RO	0x0	reserved
3:0	RW	0x0	pi_tdqsck_max_f0 Indicates additional delay that is needed for tDQSCK. The suffix "_f0" of the parameter name is omitted when in non-DFS mode.

PI_REG_161
Address: Operational Base + offset (0x0284)
DDR PHY Independent Register 161

Bit	Attr	Reset Value	Description
31:24	RW	0x00	pi_trcd_f1 Indicates DRAM TRCD value in cycles. The suffix "_f1" of the parameter name is omitted when in non-DFS mode.
23:16	RW	0x00	pi_trp_f1 Indicates DRAM TRP value in cycles. The suffix "_f1" of the parameter name is omitted when in non-DFS mode.
15:8	RW	0x00	pi_trtp_f1 Indicates DRAM TRTP value in cycles. The suffix "_f1" of the parameter name is omitted when in non-DFS mode.
7:0	RW	0x00	pi_tmod_f0 Indicates TMOD value in cycles. The suffix "_f0" of the parameter name is omitted when in non-DFS mode.

PI_REG_162
Address: Operational Base + offset (0x0288)
DDR PHY Independent Register 162

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13:8	RW	0x00	pi_twr_f1 Indicates DRAM TWR value in cycles. The suffix "_f1" of the parameter name is omitted when in non-DFS mode.
7:6	RO	0x0	reserved
5:0	RW	0x00	pi_twtr_f1 Indicates DRAM TWTR value in cycles. The suffix "_f1" of the parameter name is omitted when in non-DFS mode.

PI_REG_163
Address: Operational Base + offset (0x028c)
DDR PHY Independent Register 163

Bit	Attr	Reset Value	Description
31:24	RW	0x00	pi_tras_min_f1 Indicates DRAM TRAS_MIN value in cycles. The suffix "_f1" of the parameter name is omitted when in non-DFS mode.
23:17	RO	0x0	reserved
16:0	RW	0x00000	pi_tras_max_f1 Indicates DRAM TRAS_MAX value in cycles. The suffix "_f1" of parameter name will be omitted when non DFS mode.

PI_REG_164
Address: Operational Base + offset (0x0290)
DDR PHY Independent Register 164

Bit	Attr	Reset Value	Description
31:24	RW	0x00	pi_tmrw_f1 Indicates DRAM TMRW value in cycles. The suffix "_f1" of the parameter name is omitted when in non-DFS mode.
23:22	RO	0x0	reserved
21:16	RW	0x00	pi_tmrd_f1 Indicates DRAM TMRD value in cycles. The suffix "_f1" of the parameter name is omitted when in non-DFS mode.
15:14	RO	0x0	reserved
13:8	RW	0x00	pi_tccdmw_f1 Indicates LPDDR4 DRAM TCCDMW in cycles. The suffix "_f1" of the parameter name is omitted when in non-DFS mode.
7:4	RO	0x0	reserved
3:0	RW	0x0	pi_tdqsck_max_f1 Indicates additional delay that is needed for tDQSCK. The suffix "_f1" of the parameter name is omitted when in non-DFS mode.

PI_REG_165
Address: Operational Base + offset (0x0294)
DDR PHY Independent Register 165

Bit	Attr	Reset Value	Description
31:24	RW	0x00	pi_trcd_f2 Indicates DRAM TRCD value in cycles. The suffix "_f2" of the parameter name is omitted when in non-DFS mode.
23:16	RW	0x00	pi_trp_f2 Indicates DRAM TRP value in cycles. The suffix "_f2" of the parameter name is omitted when in non-DFS mode.
15:8	RW	0x00	pi_trtp_f2 Indicates DRAM TRTP value in cycles. The suffix "_f2" of the parameter name is omitted when in non-DFS mode.
7:0	RW	0x00	pi_tmod_f1 Indicates TMOD value in cycles. The suffix "_f1" of the parameter name is omitted when in non-DFS mode.

PI_REG_166
Address: Operational Base + offset (0x0298)
DDR PHY Independent Register 166

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13:8	RW	0x00	pi_twr_f2 Indicates DRAM TWR value in cycles. The suffix "_f2" of the parameter name is omitted when in non-DFS mode.
7:6	RO	0x0	reserved
5:0	RW	0x00	pi_twtr_f2 Indicates DRAM TWTR value in cycles. The suffix "_f2" of the parameter name is omitted when in non-DFS mode.

PI_REG_167
Address: Operational Base + offset (0x029c)
DDR PHY Independent Register 167

Bit	Attr	Reset Value	Description
31:24	RW	0x00	pi_tras_min_f2 Indicates DRAM TRAS_MIN value in cycles. The suffix "_f2" of the parameter name is omitted when in non-DFS mode.
23:17	RO	0x0	reserved
16:0	RW	0x00000	pi_tras_max_f2 Indicates DRAM TRAS_MAX value in cycles. The suffix "_f2" of parameter name will be omitted when non DFS mode.

PI_REG_168
Address: Operational Base + offset (0x02a0)
DDR PHY Independent Register 168

Bit	Attr	Reset Value	Description
31:24	RW	0x00	pi_tmrw_f2 Indicates DRAM TMRW value in cycles. The suffix "_f2" of the parameter name is omitted when in non-DFS mode.
23:22	RO	0x0	reserved
21:16	RW	0x00	pi_tmrd_f2 Indicates DRAM TMRD value in cycles. The suffix "_f2" of the parameter name is omitted when in non-DFS mode.
15:14	RO	0x0	reserved
13:8	RW	0x00	pi_tccdmw_f2 Indicates LPDDR4 DRAM TCCDMW in cycles. The suffix "_f2" of the parameter name is omitted when in non-DFS mode.
7:4	RO	0x0	reserved
3:0	RW	0x0	pi_tdqsck_max_f2 Indicates additional delay that is needed for tDQSCK. The suffix "_f2" of the parameter name is omitted when in non-DFS mode.

PI_REG_169
Address: Operational Base + offset (0x02a4)
DDR PHY Independent Register 169

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	pi_tmod_f2 Indicates TMOD value in cycles. The suffix "_f2" of the parameter name is omitted when in non-DFS mode.

PI_REG_174
Address: Operational Base + offset (0x02b8)
DDR PHY Independent Register 174

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25:8	RO	0x00000	pi_int_status Indicates status of interrupt features in the PI.
7:0	RO	0x0	reserved

PI_REG_175
Address: Operational Base + offset (0x02bc)
DDR PHY Independent Register 175

Bit	Attr	Reset Value	Description
31:18	RO	0x0	reserved
17:0	WO	0x00000	pi_int_ack Clears the corresponding interrupt bit of the PI_REG_174.pi_int_status parameter.

PI_REG_176
Address: Operational Base + offset (0x02c0)
DDR PHY Independent Register 176

Bit	Attr	Reset Value	Description
31:18	RO	0x0	reserved
17:0	RW	0x00000	pi_int_mask Indicates mask for PI interrupt signals from the PI_REG_174.pi_int_status parameter.

PI_REG_186
Address: Operational Base + offset (0x02e8)
DDR PHY Independent Register 186

Bit	Attr	Reset Value	Description
31:25	RO	0x0	reserved
24	RW	0x0	pi_ctrlupd_req_per_aref_en Enables an automatic PI-initiated update (dfi_ctrlupd_req) after every refresh. Set to 1 to enable.
23:21	RO	0x0	reserved
20:16	RW	0x00	pi_long_count_mask Reduces the length of the long counter from 1024 cycles. The only supported values are 0x00 (1024 cycles), 0x10 (512 clocks), 0x18 (256 clocks), 0x1C (128 clocks), 0x1E (64 clocks), and 0x1F (32 clocks).
15:13	RO	0x0	reserved
12:8	RW	0x00	pi_bstlen Indicates encoded burst length that is sent to DRAMs during initialization. Set to 1 for BL2, set to 2 for BL4, or set to 3 for BL8.
7:0	RO	0x0	reserved

PI_REG_187

Address: Operational Base + offset (0x02ec)
DDR PHY Independent Register 187

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:8	RW	0x0000	pi_tdfi_ctrlupd_max_f0 Defines the DFI tCTRLUPD_MAX timing parameter (in DFI clocks), the maximum cycles that dfi_ctrlupd_req can be asserted. If programmed to a non-zero, a timing violation causes an interrupt and bit (1) set in the PI_REG_193.pi_update_error_status parameter. The suffix "_f0" of the parameter name is omitted when in non-DFS mode.
7:4	RO	0x0	reserved
3:0	RO	0x0	pi_tdfi_ctrlupd_min Reports the DFI tCTRLUPD_MIN timing parameter (in DFI clocks), the minimum cycles that dfi_ctrlupd_req must be asserted.

PI_REG_188
Address: Operational Base + offset (0x02f0)
DDR PHY Independent Register 188

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pi_tdfi_ctrlupd_interval_f0 Defines the DFI tCTRLUPD_INTERVAL timing parameter (in DFI clocks), the maximum cycles between dfi_ctrlupd_req assertions. If programmed to a non-zero, a timing violation causes an interrupt and bit0 set in the PI_REG_193.pi_update_error_status parameter. The suffix "_f0" of the parameter name is omitted when in non-DFS mode.

PI_REG_189
Address: Operational Base + offset (0x02f4)
DDR PHY Independent Register 189

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	pi_tdfi_ctrlupd_max_f1 Defines the DFI tCTRLUPD_MAX timing parameter (in DFI clocks), the maximum cycles that dfi_ctrlupd_req can be asserted. If programmed to a non-zero, a timing violation causes an interrupt and bit (1) set in the PI_REG_193.pi_update_error_status parameter. The suffix "_f1" of the parameter name is omitted when in non-DFS mode.

PI_REG_190
Address: Operational Base + offset (0x02f8)
DDR PHY Independent Register 190

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pi_tdfi_ctrlupd_interval_f1 Defines the DFI tCTRLUPD_INTERVAL timing parameter (in DFI clocks), the maximum cycles between dfi_ctrlupd_req assertions. If programmed to a non-zero, a timing violation causes an interrupt and bit0 set in the PI_REG_193.pi_update_error_status parameter. The suffix "_f1" of the parameter name is omitted when in non-DFS mode.

PI_REG_191
Address: Operational Base + offset (0x02fc)
DDR PHY Independent Register 191

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	pi_tdfi_ctrlupd_max_f2 Defines the DFI tCTRLUPD_MAX timing parameter (in DFI clocks), the maximum cycles that dfi_ctrlupd_req can be asserted. If programmed to a non-zero, a timing violation causes an interrupt and bit (1) set in the PI_REG_193.pi_update_error_status parameter. The suffix "_f2" of the parameter name is omitted when in non-DFS mode.

PI_REG_192
Address: Operational Base + offset (0x0300)
DDR PHY Independent Register 192

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pi_tdfi_ctrlupd_interval_f2 Defines the DFI tCTRLUPD_INTERVAL timing parameter (in DFI clocks), the maximum cycles between dfi_ctrlupd_req assertions. If programmed to a non-zero, a timing violation causes an interrupt and bit0 set in the PI_REG_193.pi_update_error_status parameter. The suffix "_f2" of the parameter name is omitted when in non-DFS mode.

PI_REG_193
Address: Operational Base + offset (0x0304)
DDR PHY Independent Register 193

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6:0	RO	0x00	pi_update_error_status Identifies the source of any DFI PI-initiated or PHY-initiated update errors. A value of 1 indicates a timing violation of the associated timing parameter. Bit 5-0: phyupd_resp_error, phyupd_type3_error, phyupd_type2_error, phyupd_type1_error, ctrlupd_max_error, ctrlupd_interval_error.

PI_REG_199
Address: Operational Base + offset (0x031c)
DDR PHY Independent Register 199

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x0	pi_col_diff Indicates the difference between the number of column pins available and the number being used.

3. CIC register
CIC_CTRL0
Address: Operational Base + offset (0x0000)
DDR Controller LP Interface Control Register 0

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software. When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software. When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software. When bit 31=0, bit 15 cannot be written by software;
15:12	RO	0x0	reserved
11	RW	0x0	ddr0_cntrl_freq_change_ack Channel 0 DDR controller frequency change acknowledge
10	RW	0x0	ddr0_cntrl_freq_change_ack Channel 0 DDR controller frequency change acknowledge
9	RW	0x0	Ddr1_freq_change_ack Channel 1 DDR PHY frequency change acknowledge
8	RW	0x0	ddr0_freq_change_ack Channel 0 DDR PHY frequency change acknowledge
7:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:4	RW	0x0	chg_fc_reg_copy Select the copy of timing parameters that will be used after frequency change.
3	RO	0x0	reserved
2	RW	0x0	fail_cont_en When frequency change fail, whether continue to enable change.
1	RW	0x0	chg_freq_finish Frequency change finish 1'b0: not finish 1'b1: finish
0	RW	0x0	chg_req Frequency change request 1'b0: not request 1'b1: request

CIC_CTRL1
Address: Operational Base + offset (0x0004)
DDR Controller LP Interface Control Register 1

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software. When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software. When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software. When bit 31=0, bit 15 cannot be written by software;
15:12	RO	0x0	reserved
11	RW	0x0	sref_memcg_ch1 Channel 1 memory clock gating in self-refresh 1'b0: memory is not clock gated in external self-refresh 1'b1: memory is clock gated in external self-refresh
10	RW	0x0	sref_memcg_ch0 Channel 0 memory clock gating in self-refresh 1'b0: memory is not clock gated in external self-refresh 1'b1: memory is clock gated in external self-refresh
9	RW	0x0	lp_cmd_prio_ch1 Channel 1 LP command priority in external self-refresh mode 1'b0: don't issue priority request when enter external self-refresh 1'b1: issue priority request when enter external self-refresh
8	RW	0x0	lp_cmd_prio_ch0 Channel 0 LP command priority in external self-refresh mode 1'b0: don't issue priority request when enter external self-refresh 1'b1: issue priority request when enter external self-refresh

Bit	Attr	Reset Value	Description
7:6	RO	0x0	reserved
5	RW	0x0	stdby_cmd_prio_ch1 Channel 1 LP command priority in standby mode 1'b0: don't issue priority request when enter standby mode 1'b1: issue priority request when enter standby mode
4	RW	0x0	stdby_cmd_prio_ch0 Channel 0 LP command priority in standby mode 1'b0: don't issue priority request when enter standby mode 1'b1: issue priority request when enter standby mode
3	RW	0x0	stdby_memcg_ch1 Channel 1 memory clock gating in standby mode 1'b0: memory is not clock gated when in standby mode 1'b1: memory is clock gated when in standby mode
2	RW	0x0	stdby_memcg_ch0 Channel 0 memory clock gating in standby mode 1'b0: memory is not clock gated when in standby mode 1'b1: memory is clock gated when in standby mode
1	RW	0x0	stdby_en_ch1 Channel 1 standby mode enable 1'b0: disable 1'b1: enable
0	RW	0x0	stdby_en_ch0 Channel 0 standby mode enable 1'b0: disable 1'b1: enable

CIC_IDLE_TH
Address: Operational Base + offset (0x0008)
DDR Controller LP Interface Idle Threshold in standby mode

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:0	RW	0x0000	idle_th Idle counter threshold in standby mode

CIC_CG_WAIT_TH
Address: Operational Base + offset (0x000c)
DDR Controller LP Interface CG Wait Threshold in standby mode

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	cg_exit_th Clock gating exit counter threshold in standby mode
15:0	RW	0x0000	cg_wait_th Clock gating wait counter threshold in standby mode

CIC_STATUS0
Address: Operational Base + offset (0x0010)

DDR Controller LP Interface Status Register 0

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13:8	RO	0x00	state_fc Frequency change state machine
7	RO	0x0	reserved
6	RO	0x0	sref_done_ext_ch1 Channel 1 external self-refresh done
5	RO	0x0	sref_req_ext_ch1 Channel 1 external self-refresh request
4	RO	0x0	sref_done_ext_ch0 Channel 0 external self-refresh done
3	RO	0x0	sref_req_ext_ch0 Channel 0 external self-refresh request
2	RO	0x0	chg_freq_wait Frequency change wait
1	RO	0x0	chg_fail Frequency change fail
0	RO	0x0	chg_done Frequency change done

CIC_STATUS1

Address: Operational Base + offset (0x0014)

DDR Controller LP Interface Status Register 1

Bit	Attr	Reset Value	Description
31:29	RO	0x0	reserved
28:16	RO	0x0000	state_ch1 Channel 1 external self-refresh and standby mode state machine
15:13	RO	0x0	reserved
12:0	RO	0x0000	state_ch0 Channel 0 external self-refresh and standby mode state machine

CIC_CTRL2

Address: Operational Base + offset (0x0018)

DDR Controller LP Interface Control Register 2

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software. When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software. When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software. When bit 31=0, bit 15 cannot be written by software;

Bit	Attr	Reset Value	Description
15:8	RW	0x0a	lp_cmd_cfg_ch1 Channel 1 external self-refresh enter command
7:0	RW	0x0a	lp_cmd_cfg_ch0 Channel 0 external self-refresh enter command

CIC_CTRL3
Address: Operational Base + offset (0x001c)
DDR Controller LP Interface Control Register 3

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software. When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software. When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software. When bit 31=0, bit 15 cannot be written by software;
15:8	RW	0x01	lp_cmd_exit_cfg_ch1 Channel 1 external self-refresh exit command
7:0	RW	0x01	lp_cmd_exit_cfg_ch0 Channel 0 external self-refresh exit command

CIC_CTRL4
Address: Operational Base + offset (0x0020)
DDR Controller LP Interface Control Register 4

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software. When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software. When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software. When bit 31=0, bit 15 cannot be written by software;
15:8	RW	0x8a	lp_cmd_fchg_cfg_ch1 Channel 1 frequency change enter command
7:0	RW	0x8a	lp_cmd_fchg_cfg_ch0 Channel 0 frequency change enter command

CIC_STATUS2
Address: Operational Base + offset (0x0040)
DDR Controller LP Interface Status Register 2

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:18	RO	0x0	reserved
17	RO	0x0	ddr1_cntrl_freq_change_req Channel 1 DDR controller frequency change request
16:15	RO	0x0	ddr1_cntrl_freq_change_req_type Channel 1 DDR controller frequency change request type
14	RO	0x0	ddr1_freq_change_req Channel 1 DDR PHY frequency change request
13:9	RO	0x00	ddr1_freq_change_req_type Channel 1 DDR PHY frequency change request type
8	RO	0x0	ddr0_cntrl_freq_change_req Channel 0 DDR controller frequency change request
7:6	RO	0x0	ddr0_cntrl_freq_change_req_type Channel 0 DDR controller frequency change request type
5	RO	0x0	ddr0_freq_change_req Channel 0 DDR PHY frequency change request
4:0	RO	0x00	ddr0_freq_change_req_type Channel 0 DDR PHY frequency change request type

4. DDR monitor register

DDRMON_IP_VERSION

Address: Operational Base + offset (0x0000)

DDR Monitor IP Version

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RO	0x20	ip_version DDR monitor IP version

DDRMON_CTRL

Address: Operational Base + offset (0x0004)

DDR Monitor Control Register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by softwar . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software. When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software. When bit 31=0, bit 15 cannot be written by software;
15:5	RO	0x0	reserved
4	RW	0x0	lpddr4_en LPDDR4 Mode Enable 1'b1: enable 1'b0: disable

Bit	Attr	Reset Value	Description
3	RW	0x1	hardware_en Hardware Mode Enable 1'b1: enable 1'b0: disable
2	RW	0x0	lpddr3_en LPDDR3 Mode Monitor Enable 1'b1: enable 1'b0: disable
1	RW	0x0	software_en Software Mode Enable 1'b1: enable 1'b0: disable
0	RW	0x0	timer_cnt_en DFI Timer Count Enable 1'b1: enable 1'b0: disable

DDRMON_INT_STATUS
Address: Operational Base + offset (0x0008)
Interrupt Status

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8	RO	0x0	ch1_rd_addr_hit This is the interrupt status of channel 1 read address hit the setting range
7	RO	0x0	ch1_wr_addr_hit This is the interrupt status of channel 1 write address hit the setting range
6	RO	0x0	ch0_rd_addr_hit This is the interrupt status of channel 0 read address hit the setting range
5	RO	0x0	ch0_wr_addr_hit This is the interrupt status of channel 0 write address hit the setting range
4	RO	0x0	reserved
3	RO	0x0	ch1_over_int This is the interrupt status of DDR read and write burst number more than high threshold in channel 0
2	RO	0x0	ch1_below_int This is the interrupt status of DDR read and write burst number less than low threshold in channel 0
1	RO	0x0	ch0_over_int This is the interrupt status of DDR read and write burst number more than high threshold in channel 0

Bit	Attr	Reset Value	Description
0	RO	0x0	ch0_below_int This is the interrupt status of DDR read and write burst number less than low threshold in channel 0

DDRMON_INT_MASK
Address: Operational Base + offset (0x000c)
Interrupt mask control

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8:0	RW	0x000	int_mask Interrupt mask control, when bit set to 1'b1, the corresponding interrupt will disable

DDRMON_TIMER_COUNT
Address: Operational Base + offset (0x0010)
The DFI Timer Threshold

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	timer_count The DFI timer threshold, the statistics of DDR access only be done when timer counter is less then this threshold in hardware mode

DDRMON_FLOOR_NUMBER
Address: Operational Base + offset (0x0014)
The Low Threshold in the Comparison of DDR Access

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	floor_number The low threshold in the comparison of DDR access

DDRMON_TOP_NUMBER
Address: Operational Base + offset (0x0018)
The High Threshold in the Comparison of DDR Access

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	top_number The high threshold in the comparison of DDR access

DDRMON_CH0_DFI_ACT_NUM
Address: Operational Base + offset (0x001c)
Channel 0 DFI Active Command Number

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ch0_dfi_act_num DFI active command number in the statistics range of the channel 0

DDRMON_CH0_DFI_WR_NUM

Address: Operational Base + offset (0x0020)
Channel 0 DFI write Command Number

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ch0_dfi_wr_num DFI write command number in the statistics range of the channel 0

DDRMON_CH0_DFI_RD_NUM
Address: Operational Base + offset (0x0024)
Channel 0 DFI read Command Number

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ch0_dfi_rd_num DFI read command number in the statistics range of the channel 0

DDRMON_CH0_COUNT_NUM
Address: Operational Base + offset (0x0028)
Channel 0 Timer Count Number

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ch0_dfi_count_num Timer count number in the statistics range of the channel 0, the value should be divided by 2 as actual timer count.

DDRMON_CH0_DFI_ACCESS_NUM
Address: Operational Base + offset (0x002c)
Channel 0 DFI Read and Write Command Number

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ch0_dfi_access_num DFI read and write command number in the statistics range of the channel 0

DDRMON_CH1_DFI_ACT_NUM
Address: Operational Base + offset (0x0030)
Channel 1 DFI Active Command Number

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ch1_dfi_act_num DFI active command number in the statistics range of the channel 1

DDRMON_CH1_DFI_WR_NUM
Address: Operational Base + offset (0x0034)
Channel 1 DFI write Command Number

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ch1_dfi_wr_num DFI write command number in the statistics range of the channel 1

DDRMON_CH1_DFI_RD_NUM
Address: Operational Base + offset (0x0038)
Channel 1 DFI read Command Number

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ch1_dfi_rd_num DFI read command number in the statistics range of the channel 1

DDRMON_CH1_COUNT_NUM
Address: Operational Base + offset (0x003c)
Channel 1 Timer Count Number

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ch1_dfi_count_num Timer count number in the statistics range of the channel 1, the value should be divided by 2 as actual timer count.

DDRMON_CH1_DFI_ACCESS_NUM
Address: Operational Base + offset (0x0040)
Channel 1 DFI Read and Write Command Number

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ch1_dfi_access_num DFI read and write command number in the statistics range of the channel 1

DDRMON_DDR_IF_CTRL
Address: Operational Base + offset (0x0200)
DDR interface Control Register

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software. When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software. When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software. When bit 31=0, bit 15 cannot be written by software;
15:3	RO	0x0	reserved
2	RW	0x0	if_mon_en DDR interface and DFI monitor enable 1'b1: enable 1'b0: disable
1	RW	0x0	ch1_direction Write or read monitor in channel 1 for command statistics 1'b1: read 1'b0: write
0	RW	0x0	ch0_direction Write or read monitor in channel 0 for command statistics 1'b1: read 1'b0: write

DDRMON_CH0_WR_START_ADDR
Address: Operational Base + offset (0x020c)
Channel 0 Write Start Address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ch0_wr_start_addr Channel 0 write start address for address comparison

DDRMON_CH0_WR_END_ADDR
Address: Operational Base + offset (0x0210)
Channel 0 Write End Address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ch0_wr_end_addr Channel 0 write end address for address comparison

DDRMON_CH0_RD_START_ADDR
Address: Operational Base + offset (0x0214)
Channel 0 Read Start Address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ch0_rd_start_addr Channel 0 read start address for address comparison

DDRMON_CH0_RD_END_ADDR
Address: Operational Base + offset (0x0218)
Channel 0 Read End Address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ch0_rd_end_addr Channel 0 read end address for address comparison

DDRMON_CH1_WR_START_ADDR
Address: Operational Base + offset (0x0224)
Channel 1 Write Start Address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ch1_wr_start_addr Channel 1 write start address for address comparison

DDRMON_CH1_WR_END_ADDR
Address: Operational Base + offset (0x0228)
Channel 1 Write End Address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ch1_wr_end_addr Channel 1 write end address for address comparison

DDRMON_CH1_RD_START_ADDR
Address: Operational Base + offset (0x022c)
Channel 1 Read Start Address

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ch1_rd_start_addr Channel 1 read start address for address comparison

DDRMON_CH1_RD_END_ADDR
Address: Operational Base + offset (0x0230)
Channel 1 Read End Address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	ch1_rd_end_addr Channel 1 read end address for address comparison

DDRMON_CH0_DDR_FIFO0_ADDR
Address: Operational Base + offset (0x0240)
DDR Channel 0 Controller Interface Address FIFO0

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ch0_ddr_fifo0_addr Channel 0 DDR controller interface address FIFO0

DDRMON_CH0_DDR_FIFO1_ADDR
Address: Operational Base + offset (0x0248)
DDR Channel 0 Controller Interface Address FIFO1

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ch0_ddr_fifo1_addr Channel 0 DDR controller interface address FIFO1

DDRMON_CH0_DDR_FIFO2_ADDR
Address: Operational Base + offset (0x0250)
DDR Channel 0 Controller Interface Address FIFO2

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ch0_ddr_fifo2_addr Channel 0 DDR controller interface address FIFO2

DDRMON_CH0_DDR_FIFO3_ADDR
Address: Operational Base + offset (0x0258)
DDR Channel 0 Controller Interface Address FIFO3

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ch0_ddr_fifo3_addr Channel 0 DDR controller interface address FIFO3

DDRMON_CH1_DDR_FIFO0_ADDR
Address: Operational Base + offset (0x0260)
DDR Channel 1 Controller Interface Address FIFO0

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ch1_ddr_fifo0_addr Channel 1 DDR controller interface address FIFO0

DDRMON_CH1_DDR_FIFO1_ADDR
Address: Operational Base + offset (0x0268)
DDR Channel 1 Controller Interface Address FIFO1

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ch1_ddr_fifo1_addr Channel 1 DDR controller interface address FIFO1

DDRMON_CH1_DDR_FIFO2_ADDR
Address: Operational Base + offset (0x0270)
DDR Channel 1 Controller Interface Address FIFO2

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ch1_ddr_fifo2_addr Channel 1 DDR controller interface address FIFO2

DDRMON_CH1_DDR_FIFO3_ADDR
Address: Operational Base + offset (0x0278)
DDR Channel 1 Controller Interface Address FIFO3

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	ch1_ddr_fifo3_addr Channel 1 DDR controller interface address FIFO3

9.5 Interface Description

DDR IOs are listed in following table for each channel.

Table 9-1 DDR IO description

Pin Name	Description
CKi (i=0,1)	Active-high clock signal to the memory device.
CKNi (i=0,1)	Active-low clock signal to the memory device.
CKEi (i=0,1)	Active-high clock enable signal to the memory device for two chip select.
CSNi (i=0,1,2,3)	Active-low chip select signal to the memory device. There are two chip select. For DDR3/DDR3L/LPDDR3, only CSN0 and CSN1 are valid; for LPDDR4, CSN2 is the copy of CSN0, and CSN3 is the copy of CSN1
RASN	Active-low row address strobe to the memory device.
CASN	Active-low column address strobe to the memory device.
WEN	Active-low write enable strobe to the memory device.
BA[2:0]	Bank address signal to the memory device.
ADDR[15:0]	Address signal to the memory device.
DQ[31:0]	Bidirectional data line to the memory device.
DQS[3:0]	Active-high bidirectional data strobes to the memory device.
DQSN[3:0]	Active-low bidirectional data strobes to the memory device.
DM[3:0]	Active-low data mask signal to the memory device.
ODTi (i=0,1)	On-Die Termination output signal for two chip select.
RESET	DDR3 reset signal.

9.6 Application Notes

9.6.1 Controller Interface control (CIC)

1. External self-refresh
The self-refresh can be enter or exit by programming controller related register, and also can

be controlled by external interface of controller and enable by PMU register.
The external self-refresh enter and exit of channel 0 DDR is controlled by the PMU register PMU_SFT_CON[8], enter when this bit asserted, and exit when this bit de-asserted. The PMU register PMU_DDR_SREF_ST[0] is the status of self-refresh which can be inquired.
The external self-refresh enter and exit of channel 1 DDR is controlled by the PMU register PMU_SFT_CON[12], enter when this bit asserted, and exit when this bit de-asserted. The PMU register PMU_DDR_SREF_ST[1] is the status of self-refresh which can be inquired.
The register CIC_CTRL1[11:10] is used to determine if DDR memory clock gating when external self-refresh, bit0 is used for channel 0, and bit1 is used for channel 1.

2. Standby mode
The standby mode is enable by register CIC_CTRL1[1:0], bit0 is used for channel 0, and bit1 is used for channel 1.
When DDR controller is idle, and after a period of waiting time, the standby mode will be activated, the clocks of DDR controller, PHY and memory scheduler can be gated.
The waiting time is determined by the register CIC_IDLE_TH. It is the counter threshold by controller clock.
The register CIC_CTRL1[3:2] is used to determine if DDR memory clock gating when standby mode, bit0 is used for channel 0, and bit1 is used for channel 1.
For the application flexibility, the GRF register can be selectively configured to disable the clock gating when standby mode, the correspondence between GRF register and the clock is as following table.

GRF register	Control gated clock
GRF_DDRC0_CON1[4]	Channel 0 controller clock
GRF_DDRC0_CON1[5]	Channel 0 PHY controller clock
GRF_DDRC0_CON1[6]	Channel 0 PHY clock
GRF_DDRC0_CON1[7]	Channel 0 memory scheduler clock
GRF_DDRC1_CON1[4]	Channel 1 controller clock
GRF_DDRC1_CON1[5]	Channel 1 PHY controller clock
GRF_DDRC1_CON1[6]	Channel 1 PHY clock
GRF_DDRC1_CON1[7]	Channel 1 memory scheduler clock

3. Fast frequency change
The DDR controller and PI have multi-set register to support fast frequency change, and CIC controls the DDR controller interface to manage the associated timing requirements, communicate with a PHY on the DFI, and complete training procedures (if enabled).
The two channel DDR change the frequency at the same time, and change to same frequency.
If system is in external self-refresh or standby mode, we must first exit the external self-refresh or standby mode.
The software flow of fast frequency change is as following figure.

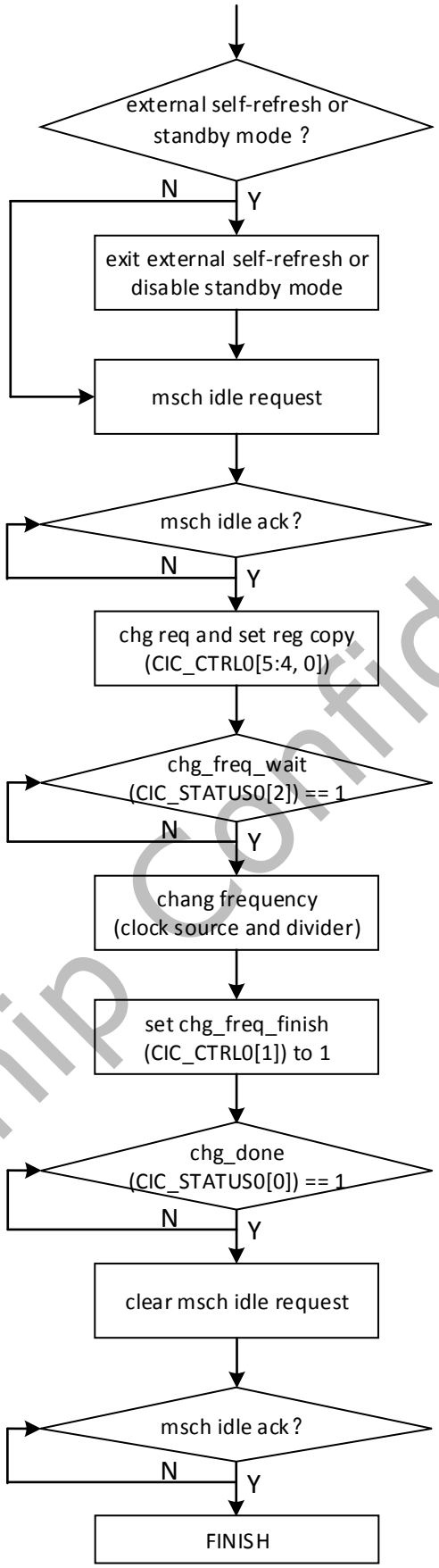


Fig. 9-3 DDR Fast Frequency Change Flow

9.6.2 DDR Monitor

1. DDR read or write address monitor

DDR monitor module can store 4 consecutive read or write addresses in real time. We can read

these addresses by APB bus for debug when system enters abnormal state.
The steps of configuration to monitor DDR read or write address:

- Configure DDRMON_DDR_IF_CTRL.ch0_direction and DDRMON_DDR_IF_CTRL.ch1_direction to select storing read or write address.
- Set DDRMON_DDR_IF_CTRL.if_mon_en to '1' to enable DDR monitor.
- When system is abnormal, we can read the register to get the current four addresses.

2. DDR access address monitor within a specified range

Sometimes we want to confirm whether DDR read or write within a specified address range, then we can configure the address range and enable this function.
The steps of configuration to monitor DDR access address within a specified range:

- Configure the channel 0 write address range registers DDRMON_CH0_WR_START_ADDR, DDRMON_CH0_WR_END_ADDR, and channel 0 read address registers DDRMON_CH0_RD_START_ADDR, DDRMON_CH0_RD_END_ADDR, and channel 1 so on.
- Enable interrupt by configure the register DDRMON_INT_MASK[8:5] to 0.
- Set DDRMON_DDR_IF_CTRL.if_mon_en to '1' to enable DDR address monitor.
- If the two channel read or write addresses hit the range, then interrupt will assert, and we can read the interrupt status register DDRMON_INT_STATUS.

3. DDR access command statistics

This module can do the statistics about DDR access command, like write, read and active by monitoring DFI interface. There are two mode to do statistics, hardware mode and software mode. Two threshold can be set, if read and write command number is more than high threshold, or less than low threshold, the interrupt will be asserted.

Hardware mode

In hardware mode, a dfi timer is used to specify a statistics period, the command statistics is done in the statistics period. The dfi timer is running in 24MHz. After dfi timer counts to the threshold, and update the statistics value, the dfi timer will restart automatically, and count again.
The steps of hardware mode of DDR access command statistics:

- Configure register DDRMON_CTRL.hardware_en as '1' to enable hardware mode.
- Configure register DDRMON_TIMER_COUNT to set the dfi timer count threshold, the statistics is done in the period of timer being less than the value of DDRMON_TIMER_COUNT.
- Configure register DDRMON_CTRL.lpddr3_en and DDRMON_CTRL.lpddr4_en to set the DDR mode:

DDRMON_CTRL.lpddr3_en	DDRMON_CTRL.lpddr4_en	DDR mode
1	0	LPDDR3
0	0	DDR3
0	1	LPDDR4

- Configure register DDRMON_FLOOR_NUMBER to specify the low threshold of interrupt, and configure register DDRMON_TOP_NUMBER to specify the high threshold of interrupt.
- Configure register DDRMON_CTRL.timer_cnt_en as '1' to start hardware mode.
- Wait for the interrupt to do following process. We also can read the read, write and active command number separately.

Software mode

In software mode, the statistics is controlled by software.
The steps of hardware mode of DDR access command statistics:

- Configure register DDRMON_CTRL.lpddr3_en and DDRMON_CTRL.lpddr4_en to set the DDR mode like hardware mode.
- Configure register DDRMON_CTRL.software_en as '1' to enable software mode statistics.
- Configure register DDRMON_CTRL.software_en as '0' to stop the statistics, and generate the statistics result. We can read the read, write and active command number separately.

Chapter 10 Embedded SRAM

10.1 Overview

The Embedded SRAM supports read and write access to provide system fast access data storage

10.1.1 Features supported

- Provide 8KB access space in PMU
- Provide 192KB access space in perilp
- Support security and non-security access
- Security or non-security space is software programmable for 192KB SRAM
- Security space is nx4KB(up to whole memory space)
- Support 32bit AHB bus for 8KB SRAM
- Support 64bit AXI bus for 192KB SRAM

10.1.2 Features not supported

- Don't support AXI lock transaction
- Don't support AXI exclusive transaction
- Don't support AXI cache function
- Don't support AXI protection function

10.2 Block Diagram

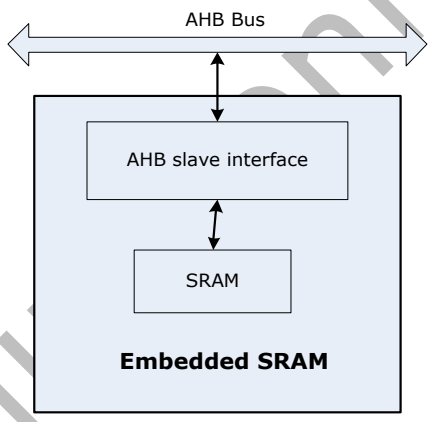


Fig. 10-1 8KB Embedded SRAM block diagram

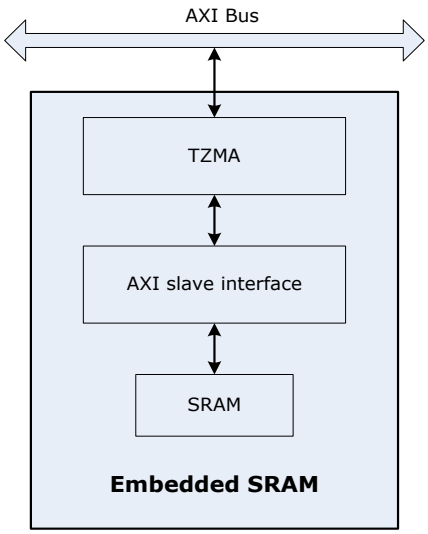


Fig. 10-2 192KB Embedded SRAM block diagram

10.3 Function Description

10.3.1 TZMA

Please refer to secure chapter for TZMA functional description

10.3.2 Embedded SRAM access path

The 8KB Embedded SRAM can only be accessed by Cortex-A72, Cortex-A53, Coresight, PMU Cortex-M0 and perilp Cortex-M0.
The 192KB Embedded SRAM can only be accessed by Cortex-A72, Cortex-A53,Coresight, PMU Cortex-M0,perilp Cortex-M0,DMAC0, DMAC1, CRYPTO0, CRYPTO1, DCF, GIC500, PCIE, USB-HOST and USB-OTG.

10.3.3 Remap

The 192KB Embedded SRAM support remap.
Before remap, the Embedded SRAM address range is 0xff8c_0000~0xff8e_ffff,
After set remap, (ref Security GRF register SGRF_SOC_CON3, bit[7]), the system can still access the Embedded SRAM by the old address. At same time, the system also can access the Embedded SRAM by the new address 0xffff_0000 ~ 0xffff_ffff (include the bootaddr).

Chapter 11 Power Management Unit (PMU)

11.1 Overview

In order to meet low power requirements, a power management unit (PMU) is designed for controlling power resources in RK3399. The RK3399 PMU is dedicated for managing the power of the whole chip.

11.1.1 Features

- Support 6 voltage domains including VD_CORE_L, VD_CORE_B, VD_CENTER, VD_GPU, VD_LOGIC and VD_PMU
- Support 31 separate power domains in the whole chip, which can be power up/down by software based on different application scenes
- In low power mode, PMU could power up/down pd_a53_0/pd_a72_0, vd_core_l/vd_core_b, pd_cci, pd_perilp, vd_center by hardware
- Support Cortex-A53/A72 core, pd_center, pd_perilp source clock gating in low power mode
- Support Cortex-A53 L2 flush request by hardware in low power mode
- Support power down/up all power domains by software
- Support core wfi auto power down by hardware

11.2 Block Diagram

11.2.1 power domain partition

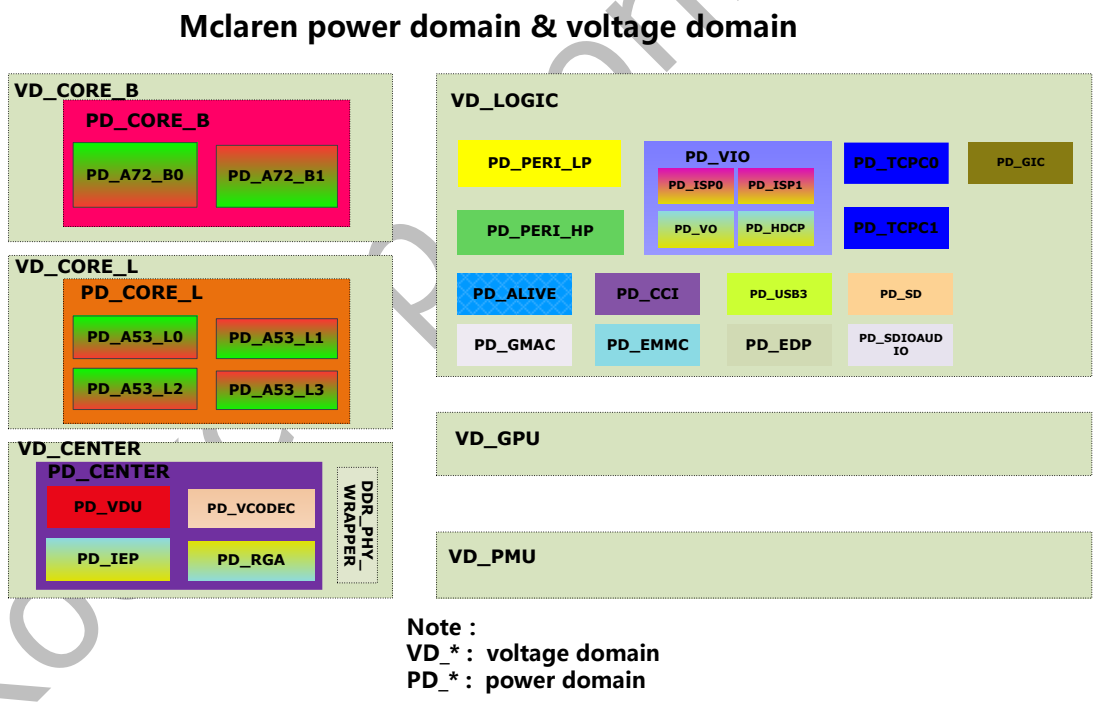


Fig. 11-1 RK3399 Power Domain Partition

The above diagram describes the power domain and voltage domain partition, and the following table lists all the power domains.

Table 11-1 RK3399 Power Domain and Voltage Domain Summary

Voltage Domain	Power Domain	Description
VD_CORE_L	pd_a53_l0	Cortex-A53 core 0, L1C and Neon
	pd_a53_l1	Cortex-A53 core 1, L1C and Neon
	pd_a53_l2	Cortex-A53 core 2, L1C and Neon
	pd_a53_l3	Cortex-A53 core 3, L1C and Neon
	pd_scu_l	SCU, L2

Voltage Domain	Power Domain	Description
VD_CORE_B	pd_a72_b0	Cortex-A72 core 0, L1C and Neon
	pd_a72_b1	Cortex-A72 core 1, L1C and Neon
	pd_scu_b	SCU, L2
VD_LOGIC	pd_perilp	cm0, crypto, dcf, imem, dmac, bootrom, efuse_con, spi, i2c, uart, saradc, tsadc
	pd_perihp	pcie, usb2, hsic
	pd_vio	include pd_isp0, pd_isp1, pd_vo, pd_hdcp, mipi dsi
	pd_isp0	isp0
	pd_isp1	isp1
	pd_vo	vopb, vopl
	pd_hdcp	hdcp, hdmi, dptx
	pd_tcpc0	tcpc0
	pd_tcpc1	tcpc1
	pd_alive	cru, grf, timer, gpio, wdt
	pd_gmac	gmac
	pd_cci	cci
	pd_emmc	emmc
	pd_usb3	usb3
	pd_edp	edp
	pd_sd	sdmmc
	pd_sdioaudio	sdio, spi, i2s, spdif
VD_CENTER	pd_rkvdec	VDPU,VEPU
	pd_vdu	rkvdec
	pd_rga	RGA
	pd_iep	IEP
	pd_center	DDR
VD_GPU	pd_gpu	GPU
VD_PMU	pd_pmu	cm0, PMU, SRAM(8K), Secure GRF, GPIO0, PVTM,i2c

11.2.2 PMU block diagram

The following figure is the PMU block diagram. The PMU includes the 3 following sections:

- APB interface and register, which can accept the system configuration
- Low Power State Control, which generate low power control signals.
- Power Switch Control, which control all power domain switch

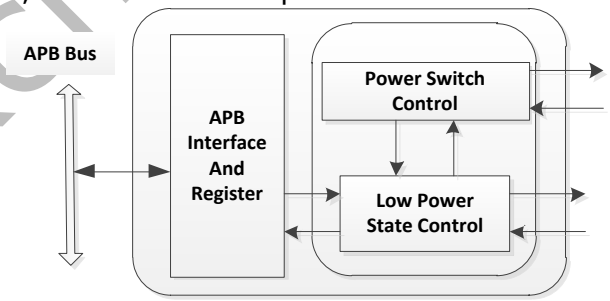


Fig. 11-2 PMU Bock Diagram

11.3 Function Description

First of all, we define two operation modes of PMU, normal mode and low power mode.
When operating at normal mode, that means software can manage power sources directly by accessing PMU register.
For example, Cortex-A53 CPU can write PMU_PWRDN_CON register to determine that power off/on which power domain independently.
When operating at low power mode, software manages power sources indirectly through FSM (Finite States Machine) in PMU and those settings always not take effect immediately.
That means software also can configure PMU registers to power down/up some power

resources, but these setting will not be executed immediately after configuration. They will delay to execute after FSM running in particular phase. The low power mode can support some functions that cannot support in normal mode. For example, some components inside RK3399 (e.g. Cortex-A53 core 0) can shut down itself through low power mode.
To entering low power mode, after setting some power configurations, the PMU_POWER_MODE[0] bit must be set 1 to enable PMU FSM. Then Cortex-A53 CPU needs to execute a WFI command to perform ready signal. After PMU detects all Cortex-A53 CPUs in WFI status, then the FSM will be fetched. And the specific power sources will be controlled during specific status in FSM. So the low power mode is a "delay affect" way to handle power sources inside the RK3399 chip.

11.4 Register Description

11.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
PMU_WAKEUP_CFG0	0x0000	W	0x00000000	pmu wakeup configure register 0
PMU_WAKEUP_CFG1	0x0004	W	0x00000000	pmu wakeup configure register 1
PMU_WAKEUP_CFG2	0x0008	W	0x00000000	pmu wakeup configure register 2
PMU_WAKEUP_CFG3	0x000c	W	0x00000000	pmu wakeup configure register 3
PMU_WAKEUP_CFG4	0x0010	W	0x00000000	pmu wakeup configure register 4
PMU_PWRDN_CON	0x0014	W	0x00000000	pmu power down configure register
PMU_PWRDN_ST	0x0018	W	0x00000000	pmu power down status register
PMU_PLL_CON	0x001c	W	0x00000000	PLL low power control register
PMU_PWRMODE_CON	0x0020	W	0x00000000	pmu power mode configure register of common resource
PMU_SFT_CON	0x0024	W	0x00000000	pmu software configure register
PMU_INT_CON	0x0028	W	0x00000000	pmu interrupt configure register
PMU_INT_ST	0x002c	W	0x00000000	pmu interrupt status register
PMU_GPIO0_POS_INT_CON	0x0030	W	0x00000000	pmu gpio0 posedge interrupt configure register
PMU_GPIO0_NEG_INT_CON	0x0034	W	0x00000000	pmu gpio0 negedge interrupt configure register
PMU_GPIO1_POS_INT_CON	0x0038	W	0x00000000	pmu gpio1 posedge interrupt configure register
PMU_GPIO1_NEG_INT_CON	0x003c	W	0x00000000	pmu gpio1 negedge interrupt configure register
PMU_GPIO0_POS_INT_ST	0x0040	W	0x00000000	pmu gpio0 posedge interrupt status register
PMU_GPIO0_NEG_INT_ST	0x0044	W	0x00000000	pmu gpio0 negedge interrupt status register
PMU_GPIO1_POS_INT_ST	0x0048	W	0x00000000	pmu gpio1 posedge interrupt status register
PMU_GPIO1_NEG_INT_ST	0x004c	W	0x00000000	pmu gpio1 negedge interrupt status register
PMU_PWRDN_INTEN	0x0050	W	0x00000000	pmu power down interrupt enable register

Name	Offset	Size	Reset Value	Description
PMU_PWRDN_STATUS	0x0054	W	0x00000000	pmu power down interrupt status register
PMU_WAKEUP_STATUS	0x0058	W	0x00000000	pmu interrupt wakeup status register
PMU_BUS_CLR	0x005c	W	0x00000000	pmu bus clear register
PMU_BUS_IDLE_REQ	0x0060	W	0x00000000	pmu bus idle request register
PMU_BUS_IDLE_ST	0x0064	W	0x00000000	pmu bus idle status register
PMU_BUS_IDLE_ACK	0x0068	W	0x00000000	pmu bus idle ack status register
PMU_CCI500_CON	0x006c	W	0x00000000	CCI-500 low power control register
PMU_ADB400_CON	0x0070	W	0x00000000	adb-400 low power control register
PMU_ADB400_ST	0x0074	W	0x00000000	adb-400 low power status register
PMU_POWER_ST	0x0078	W	0x00000000	pmu power status register
PMU_CORE_PWR_ST	0x007c	W	0x00000000	pmu core power status register
PMU_OSC_CNT	0x0080	W	0x00000000	pmu osc count register
PMU_PLLLOCK_CNT	0x0084	W	0x00000000	pmu pll lock count register
PMU_PLLRST_CNT	0x0088	W	0x00000000	pmu pll reset count register
PMU_STABLE_CNT	0x008c	W	0x00000000	pmu power stable count register
PMU_DDRIO_PWRON_CNT	0x0090	W	0x00000000	pmu ddrio power on count register
PMU_WAKEUP_RST_CLR_CNT	0x0094	W	0x00000000	pmu wakeup reset clear count register
PMU_DDR_SREF_ST	0x0098	W	0x00000000	pmu ddr self refresh status register
PMU_SCU_L_PWRDN_CNT	0x009c	W	0x00005dc0	pmu scu_l power down count register
PMU_SCU_L_PWRUP_CNT	0x00a0	W	0x00005dc0	pmu scu_l power up count register
PMU_SCU_B_PWRDN_CNT	0x00a4	W	0x00005dc0	pmu scu_b power down count register
PMU_SCU_B_PWRUP_CNT	0x00a8	W	0x00005dc0	pmu scu_b power up count register
PMU_GPU_PWRDN_CNT	0x00ac	W	0x00005dc0	pmu gpu power down count register
PMU_GPU_PWRUP_CNT	0x00b0	W	0x00005dc0	pmu gpu power up count register
PMU_CENTER_PWRDN_CNT	0x00b4	W	0x00005dc0	pmu center power down count register
PMU_CENTER_PWRUP_CNT	0x00b8	W	0x00005dc0	pmu center power up count register
PMU_TIMEOUT_CNT	0x00bc	W	0x00000000	pmu timeout count register
PMU_CPU0APM_CON	0x00c0	W	0x00000000	pmu cpu0 auto power down control register
PMU_CPU1APM_CON	0x00c4	W	0x00000000	pmu cpu1 auto power down control register
PMU_CPU2APM_CON	0x00c8	W	0x00000000	pmu cpu2 auto power down control register
PMU_CPU3APM_CON	0x00cc	W	0x00000000	pmu cpu3 auto power down control register

Name	Offset	Size	Reset Value	Description
PMU_CPU0BPM_CON	0x00d0	W	0x00000000	pmu cluster_b cpu0 auto power down control register
PMU_CPU1BPM_CON	0x00d4	W	0x00000000	pmu cluster_b cpu0 auto power down control register
PMU_NOC_AUTO_ENA	0x00d8	W	0x00000000	NOC auto domain clock gating disable enable register
PMU_PWRDN_CON1	0x00dc	W	0x00000000	pmu power down configure register1
PMU_SYS_REG0	0x00f0	W	0x00000000	pmu system register 0
PMU_SYS_REG1	0x00f4	W	0x00000000	pmu system register 1
PMU_SYS_REG2	0x00f8	W	0x00000000	pmu system register 2
PMU_SYS_REG3	0x00fc	W	0x00000000	pmu system register 3

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

11.4.2 Detail Register Description

PMU_WAKEUP_CFG0
Address: Operational Base + offset (0x0000)
pmu wakeup configure register 0

Bit	Attr	Reset Value	Description
31:24	RW	0x00	gpio0d_posedge_en gpio0d posedge pulse wakeup enable 0: disable 1: enable
23:16	RW	0x00	gpio0c_posedge_en gpio0c posedge pulse wakeup enable 0: disable 1: enable
15:8	RW	0x00	gpio0b_posedge_en gpio0b posedge pulse wakeup enable 0: disable 1: enable
7:0	RW	0x00	gpio0a_posedge_en gpio0a posedge pulse wakeup enable 0: disable 1: enable

PMU_WAKEUP_CFG1
Address: Operational Base + offset (0x0004)
pmu wakeup configure register 1

Bit	Attr	Reset Value	Description
31:24	RW	0x00	gpio0d_negedge_en gpio0d negedge pulse wakeup enable 0: disable 1: enable

Bit	Attr	Reset Value	Description
23:16	RW	0x00	gpio0c_negedge_en gpio0c negedge pulse wakeup enable 0: disable 1: enable
15:8	RW	0x00	gpio0b_negedge_en gpio0b negedge pulse wakeup enable 0: disable 1: enable
7:0	RW	0x00	gpio0a_negedge_en gpio0a negedge pulse wakeup enable 0: disable 1: enable

PMU_WAKEUP_CFG2
Address: Operational Base + offset (0x0008)
pmu wakeup configure register 2

Bit	Attr	Reset Value	Description
31:24	RW	0x00	gpio1d_posedge_en gpio1d posedge pulse wakeup enable 0: disable 1: enable
23:16	RW	0x00	gpio1c_posedge_en gpio1c posedge pulse wakeup enable 0: disable 1: enable
15:8	RW	0x00	gpio1b_posedge_en gpio1b posedge pulse wakeup enable 0: disable 1: enable
7:0	RW	0x00	gpio1a_posedge_en gpio1a posedge pulse wakeup enable 0: disable 1: enable

PMU_WAKEUP_CFG3
Address: Operational Base + offset (0x000c)
pmu wakeup configure register 3

Bit	Attr	Reset Value	Description
31:24	RW	0x00	gpio1d_negedge_en gpio1d negedge pulse wakeup enable 0: disable 1: enable

Bit	Attr	Reset Value	Description
23:16	RW	0x00	gpio1c_negedge_en gpio1c negedge pulse wakeup enable 0: disable 1: enable
15:8	RW	0x00	gpio1b_negedge_en gpio1b negedge pulse wakeup enable 0: disable 1: enable
7:0	RW	0x00	gpio1a_negedge_en gpio1a negedge pulse wakeup enable 0: disable 1: enable

PMU_WAKEUP_CFG4
Address: Operational Base + offset (0x0010)
pmu wakeup configure register 4

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13	RW	0x0	pcie_en pcie interrupt wakeup enable 0: disable 1: enable
12	RO	0x0	reserved
11	RW	0x0	pwm_en pwm interrupt wakeup enable 0: disable 1: enable
10	RW	0x0	timeout_en pmu time out wakeup enable 0: disable 1: enable
9	RW	0x0	wdt_m0_en m3 watch dog wakeup enable 0: disable 1: enable
8	RW	0x0	sft_en software wakeup enable 0: disable 1: enable
7	RW	0x0	usbdev_en usb device detect wakeup enable 0: disable 1: enable

Bit	Attr	Reset Value	Description
6	RW	0x0	timer_en timer wakeup enable 0: disable 1: enable
5	RO	0x0	reserved
4	RW	0x0	sdmmc_en sdmmc detect wakeup enable 0: disable 1: enable
3	RW	0x0	sdio_en sdio detect wakeup enable 0: disable 1: enable
2	RW	0x0	gpio_int_en gpio interrupt wakeup enable 0: disable 1: enable
1	RW	0x0	int_cluster_b_en cluster_b interrupt wakeup enable 0: disable 1: enable
0	RW	0x0	int_cluster_l_en cluster_l interrupt wakeup enable 0: disable 1: enable

PMU_PWRDN_CON

Address: Operational Base + offset (0x0014)

pmu power down configure register

Bit	Attr	Reset Value	Description
31	RW	0x0	pd_sdioaudio_pwrdwn_en pd_sdioaudio power down enable 0: disable 1: enable
30	RW	0x0	pd_sd_pwrdwn_en pd_sd power down enable 0: disable 1: enable
29	RW	0x0	pd_gic_pwrdwn_en pd_gic power down enable 0: disable 1: enable

Bit	Attr	Reset Value	Description
28	RW	0x0	pd_edp_pwrdwn_en pd_edp power down enable 0: disable 1: enable
27	RW	0x0	pd_usb3_pwrdwn_en pd_usb3 power down enable 0: disable 1: enable
26	RW	0x0	pd_emmc_pwrdwn_en pd_emmc power down enable 0: disable 1: enable
25	RW	0x0	pd_gmac_pwrdwn_en pd_gmac power down enable 0: disable 1: enable
24	RW	0x0	pd_hdcp_pwrdwn_en pd_hdcp power down enable 0: disable 1: enable
23	RW	0x0	pd_isp1_pwrdwn_en pd_isp1 power down enable 0: disable 1: enable
22	RW	0x0	pd_isp0_pwrdwn_en pd_isp0 power down enable 0: disable 1: enable
21	RO	0x0	reserved
20	RW	0x0	pd_vo_pwrdwn_en pd_vo power down enable 0: disable 1: enable
19	RW	0x0	pd_iep_pwrdwn_en pd_perihp power down enable 0: disable 1: enable
18	RW	0x0	pd_rga_pwrdwn_en pd_rga power down enable 0: disable 1: enable
17	RW	0x0	pd_vdu_pwrdwn_en pd_vdu power down enable 0: disable 1: enable

Bit	Attr	Reset Value	Description
16	RW	0x0	pd_vcodec_pwrdwn_en pd_perihp power down enable 0: disable 1: enable
15	RW	0x0	pd_gpu_pwrdwn_en pd_gpu power down enable 0: disable 1: enable
14	RW	0x0	pd_vio_pwrdwn_en pd_vio power down enable 0: disable 1: enable
13	RW	0x0	pd_center_pwrdwn_en pd_center power down enable 0: disable 1: enable
12	RW	0x0	pd_perihp_pwrdwn_en pd_perihp power down enable 0: disable 1: enable
11	RW	0x0	pd_perilp_pwrdwn_en pd_perilp power down enable 0: disable 1: enable
10	RW	0x0	pd_cci_pwrdwn_en pd_cci power down enable 0: disable 1: enable
9	RW	0x0	pd_tcpd1_pwrdwn_en pd_tcpd1 power down enable 0: disable 1: enable
8	RW	0x0	pd_tcpd0_pwrdwn_en pd_tcpd0 power down enable 0: disable 1: enable
7	RW	0x0	pd_scu_b_pwrdwn_en pd_scu_b power down enable 0: disable 1: enable
6	RW	0x0	pd_scu_l_pwrdwn_en pd_scu_l power down enable 0: disable 1: enable

Bit	Attr	Reset Value	Description
5	RW	0x0	pd_a72_b1_pwrdwn_en pd_a72_b0 power down enable 0: disable 1: enable
4	RW	0x0	pd_a72_b0_pwrdwn_en pd_a72_b0 power down enable 0: disable 1: enable
3	RW	0x0	pd_a53_l3_pwrdwn pd_a53_l3 power down enable 0: disable 1: enable
2	RW	0x0	pd_a53_l2_pwrdwn pd_a53_l2 power down enable 0: disable 1: enable
1	RW	0x0	pd_a53_l1_pwrdwn pd_a53_l1 power down enable 0: disable 1: enable
0	RW	0x0	pd_a53_l0_pwrdwn_en pd_a53_l0 power down enable 0: disable 1: enable

PMU_PWRDN_ST
Address: Operational Base + offset (0x0018)
pmu power down status register

Bit	Attr	Reset Value	Description
31	RW	0x0	pd_sdioaudio_pwr_stat pd_sdioaudio power state 0: powered up 1: powered down
30	RW	0x0	pd_sd_pwr_stat pd_sd power state 0: powered up 1: powered down
29	RW	0x0	pd_gic_pwr_stat pd_gic power state 0: powered up 1: powered down
28	RW	0x0	pd_edp_pwr_stat pd_edp power state 0: powered up 1: powered down

Bit	Attr	Reset Value	Description
27	RW	0x0	pd_usb3_pwr_stat pd_usb3 power state 0: powered up 1: powered down
26	RW	0x0	pd_emmc_pwr_stat pd_emmc power state 0: powered up 1: powered down
25	RW	0x0	pd_gmac_pwr_stat pd_gmac power state 0: powered up 1: powered down
24	RW	0x0	pd_hdcp_pwr_stat pd_hdcp power state 0: powered up 1: powered down
23	RW	0x0	pd_isp1_pwr_stat pd_isp1 power state 0: powered up 1: powered down
22	RW	0x0	pd_isp0_pwr_stat pd_isp0 power state 0: powered up 1: powered down
21	RO	0x0	reserved
20	RW	0x0	pd_vo_pwr_stat pd_vo power state 0: powered up 1: powered down
19	RW	0x0	pd_iep_pwr_stat pd_iep power state 0: powered up 1: powered down
18	RW	0x0	pd_rga_pwr_stat pd_rga power state 0: powered up 1: powered down
17	RW	0x0	pd_vdu_pwr_stat pd_vdu power state 0: powered up 1: powered down
16	RW	0x0	pd_vcodec_pwr_stat pd_vcodec power state 0: powered up 1: powered down

Bit	Attr	Reset Value	Description
15	RW	0x0	pd_gpu_pwr_stat pd_gpu power state 0: powered up 1: powered down
14	RW	0x0	pd_vio_pwr_stat pd_vio power state 0: powered up 1: powered down
13	RW	0x0	pd_center_pwr_stat pd_center power state 0: powered up 1: powered down
12	RW	0x0	pd_perihp_pwr_stat pd_peri power state 0: powered up 1: powered down
11	RW	0x0	pd_perilp_pwr_stat pd_bus power stat 0: powered up 1: powered down
10	RW	0x0	pd_cci_pwr_stat pd_core power state 0: powered up 1: powered down
9	RW	0x0	pd_tcpd1_pwr_stat pd_tcpd1 power state 0: powered up 1: powered down
8	RW	0x0	pd_tcpd0_pwr_stat pd_tcpd0 power state 0: powered up 1: powered down
7	RO	0x0	pd_scu_b_pwr_stat pd_scu_b power state 0: powered up 1: powered down
6	RO	0x0	pd_scu_l_pwr_stat pd_scu_l power state 0: powered up 1: powered down
5	RO	0x0	pd_a72_b1_pwr_stat pd_a72_b1 power state 0: powered up 1: powered down

Bit	Attr	Reset Value	Description
4	RO	0x0	pd_a72_b0_pwr_stat pd_a72_b0 power state 0: powered up 1: powered down
3	RO	0x0	pd_a53_l3_pwr_stat pd_a53_l3 power state 0: powered up 1: powered down
2	RO	0x0	pd_a53_l2_pwr_stat pd_a53_l2 power state 0: powered up 1: powered down
1	RO	0x0	pd_a53_l1_pwr_stat pd_a53_l1 power state 0: powered up 1: powered down
0	RO	0x0	pd_a53_l0_pwr_stat pd_a53_l0 power state 0: powered up 1: powered down

PMU_PLL_CON
Address: Operational Base + offset (0x001c)

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:8	RW	0x00	sft_pll_pd pll power down configured by sftware.
7:0	RW	0x00	pll_pd_cfg pll power down configured by hardware

PMU_PWRMODE_CON
Address: Operational Base + offset (0x0020)
pmu power mode configure register of common resource

Bit	Attr	Reset Value	Description
31	RW	0x0	main_cluster use core big for main cluster. 0: core_l ; 1: core_b.
30	RW	0x0	sleep_output_cfg output pmu_sleep instead of ap_pwroff to IO.
29	RW	0x0	ddrio_ret_hw_de_req hardware ddrio retention de-assert request

Bit	Attr	Reset Value	Description
28	RW	0x0	clk_core_src_gate_en cpu clock gate enable when in power mode 0: disable 1: enable
27	RW	0x0	clk_perilp_src_gate_en pd_perilp clock gate enable when in power mode 0: disable 1: enable
26	RW	0x0	clk_center_src_gate_en pd_center clock gate enable when in power mode 0: disable 1: enable
25:24	RO	0x0	reserved
23	W1C	0x0	ddrio1_ret_de_req ddrio1 retention de-assert request write one clear
22	RW	0x0	ddrio1_ret_en ddrio1 retention enable when in power mode 0: disable 1: enable
21	RW	0x0	ddrc1_gating_en ddr1 controller auto gating when in power mode 0: disable 1: enable
20	RW	0x0	sref1_enter_en ddr1 self_refresh by hardware when in power mode 0: disable 1: enable
19	W1C	0x0	ddrio0_ret_de_req ddrio0 retention de-assert request write one clear
18	RW	0x0	ddrio0_ret_en ddrio0 retention enable when in power mode 0: disable 1: enable
17	RW	0x0	ddrc0_gating_en ddr0 controller auto gating when in power mode 0: disable 1: enable
16	RW	0x0	sref0_enter_en ddr0 self_refresh by hardware when in power mode 0: disable 1: enable

Bit	Attr	Reset Value	Description
15	RW	0x0	center_pd_en power down pd_center when power mode 0: disable 1: enable
14	RW	0x0	perilp_pd_en power down pd_perilp when power mode 0: disable 1: enable
13	RW	0x0	cci_pd_en power down pd_cci when power mode 0: disable 1: enable
12	RW	0x0	scu_pd_en power down main cluster scu when in power mode 0: disable 1: enable
11	RW	0x0	l2_idle_en wait l2 idle when in power mode 0: disable 1: enable
10	RW	0x0	l2_flush_en flush l2 by hardware when in power mode 0: disable 1: enable
9	RW	0x0	cpu0_pd_en power down core0 of cluster_l in power mode 0: disable 1: enable
8	RW	0x0	pll_pd_en power down pll when in power mode 0: disable 1: enable
7	RW	0x0	chip_pd_en chip power down enable 0: disable 1: enable
6	RW	0x0	power_off_req_cfg send power off request to PMIC when in power mode 0: disable 1: enable
5	RW	0x0	pmu_use_lf pmu low frequency mode enable when in power mode 0: disable 1: enable

Bit	Attr	Reset Value	Description
4	RW	0x0	alive_use_lf alive low frequency mode when in power mode 0: disable 1: enable
3	RW	0x0	osc_disable osc disable when in power mode 1: disable 0: enable
2	RW	0x0	input_clamp_en clamp vd_logic when in power mode 0: disable 1: enable
1	RW	0x0	wakeup_reset_en wakeup reset enable when in power mode 0: disable 1: enable
0	RW	0x0	power_mode_en enter power mode enable, will auto self-clear when in power mode 0: disable 1: enable

PMU_SFT_CON
Address: Operational Base + offset (0x0024)
pmu software configure register

Bit	Attr	Reset Value	Description
31	RW	0x0	acinactm_cluster_b_cfg acinactm indicate to cluster_b 0: acinactm to cluster_b is 0 1: acinactm to cluster_b is 1
30	RW	0x0	l2flushreq_cluster_b send l2 flush request to cluster_l by software 0: disable 1: enable
29	RW	0x0	cluster_b_clk_src_gating_cfg cluster_b clock source gating configure 0: disable 1: enable
28	RW	0x0	dbgpwrupreq_b_en dbg powered up request function of cluster_b enable 0: disable 1: enable
27:26	RO	0x0	reserved

Bit	Attr	Reset Value	Description
25:24	RW	0x0	dbgnopwrdwn_b_enable dbgnopowerdown function of cluster_b enable 0: disable 1: enable
23	RW	0x0	acinactm_cluster_l_cfg acinactm indicate to cluster_l 0: acinactm to cluster_l is 0 1: acinactm to cluster_l is 1
22	RW	0x0	l2flushreq_cluster_l send l2 flush request to cluster_l by software 0: disable 1: enable
21	RW	0x0	cluster_l_clk_src_gating_cfg cluster_l clock source gating configure 0: disable 1: enable
20	RW	0x0	dbgpwrupreq_l_en dbg powered up request function of cluster_l enable 0: disable 1: enable
19:16	RW	0x0	dbgnopwrdwn_l_enable dbgnopowerdown function of cluster_l enable 0: disable 1: enable
15	RW	0x0	dbgpwrdup_b0_cfg dbg powered up of pd_a72_b0 enable when in power mode 0: disable 1: enable
14	RO	0x0	reserved
13	RW	0x0	ddr1_io_ret_cfg ddr1 io retention configure by software 0: disable 1: enable
12	RW	0x0	ddrctl1_c_sysreq_cfg ddrctl1 idle request configure 0: disable 1: enable
11:10	RO	0x0	reserved
9	RW	0x0	ddr0_io_ret_cfg ddr0 io retention configure by software 0: disable 1: enable

Bit	Attr	Reset Value	Description
8	RW	0x0	ddrctl0_c_sysreq_cfg ddrctl idle request configure 0: disable 1: enable
7	RW	0x0	wakeup_sft_m0 m0 configure this bit to wakeup PMU state machine.
6	RW	0x0	dbgpwrdup_l0_cfg dbg powered up of pd_a53_l0 enable when in power mode 0: disable 1: enable
5	RW	0x0	pmu_24m_ena_cfg configure PD_PMU use 24M clock
4	RW	0x0	alive_lf_ena_cfg pd_alive low frequency mode configure by software 0: disable 1: enable
3	RW	0x0	pmu_lf_ena_cfg pd_pmu low frequency mode configure by software 0: disable 1: enable
2	RW	0x0	osc_disable_cfg osc disable configure by software 1: disable osc 0: enable psc
1	RW	0x0	input_clamp_cfg software control of input clamp signal
0	RW	0x0	wakeup_sft software wakeup request bit A 0 to 1 pulse posedge will wakeup pmu when in low power mode

PMU_INT_CON

Address: Operational Base + offset (0x0028)

pmu interrupt configure register

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5	RW	0x0	wakeup_gpio1_pos_int_en gpio1 posedge wakeup interrupt enable 0: disable 1: enable
4	RW	0x0	wakeup_gpio1_neg_int_en gpio1 negedge wakeup interrupt enable 0: disable 1: enable

Bit	Attr	Reset Value	Description
3	RW	0x0	wakeup_gpio0_pos_int_en gpio posedge wakeup interrupt enable 0: disable 1: enable
2	RW	0x0	wakeup_gpio0_neg_int_en gpio0 negedge wakeup interrupt enable 0: disable 1: enable
1	RW	0x0	pwrmode_wakeup_int_en power mode wakeup interrupt enable 0: disable 1: enable
0	RW	0x0	pmu_int_en global interrupt enable 0: disable 1: enable

PMU_INT_ST
Address: Operational Base + offset (0x002c)
pmu interrupt status register

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5	RW	0x0	wakeup_gpio1_neg_status gpio1 negedge pulse wakeup status 0: not wakeup by gpio1 negedge pulse 1: wakeup by gpio1 negedge pulse
4	RW	0x0	wakeup_gpio1_pos_status gpio1 posedge pulse wakeup status 0: not wakeup by gpio1 posedge pulse 1: wakeup by gpio1 posedge pulse
3	RW	0x0	wakeup_gpio0_pos_status gpio0 posedge pulse wakeup status 0: not wakeup by gpio0 posedge pulse 1: wakeup by gpio0 posedge pulse
2	RW	0x0	wakeup_gpio0_neg_status gpio0 negedge pulse wakeup status 0: not wakeup by gpio negedge pulse 1: wakeup by gpio negedge pulse
1	RW	0x0	pwrmode_wakeup_status power mode wakeup status 0: not wakeup from power mode 1: wakeup from power mode
0	RO	0x0	reserved

PMU_GPIO0_POS_INT_CON

Address: Operational Base + offset (0x0030)
pmu gpio0 posedge interrupt configure register

Bit	Attr	Reset Value	Description
31:24	RW	0x00	gpio0d_pos_int_en gpio0d posedge pulse interrupt enable 0: disable 1: enable
23:16	RW	0x00	gpio0c_pos_int_en gpio0c posedge pulse interrupt enable 0: disable 1: enable
15:8	RW	0x00	gpio0b_pos_int_en gpio0b posedge pulse interrupt enable 0: disable 1: enable
7:0	RW	0x00	gpio0a_pos_int_en gpio0a posedge pulse interrupt enable 0: disable 1: enable

PMU_GPIO0_NEG_INT_CON
Address: Operational Base + offset (0x0034)
pmu gpio0 negedge interrupt configure register

Bit	Attr	Reset Value	Description
31:24	RW	0x00	gpio0d_neg_int_en gpio0d negedge pulse interrupt enable 0: disable 1: enable
23:16	RW	0x00	gpio0c_neg_int_en gpio0c negedge pulse interrupt enable 0: disable 1: enable
15:8	RW	0x00	gpio0b_neg_int_en gpio0b negedge pulse interrupt enable 0: disable 1: enable
7:0	RW	0x00	gpio0a_neg_int_en gpio0a negedge pulse interrupt enable 0: disable 1: enable

PMU_GPIO1_POS_INT_CON
Address: Operational Base + offset (0x0038)
pmu gpio1 posedge interrupt configure register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:24	RW	0x00	gpio1d_pos_int_en gpio1d posedge pulse interrupt enable 0: disable 1: enable
23:16	RW	0x00	gpio1c_pos_int_en gpio1c posedge pulse interrupt enable 0: disable 1: enable
15:8	RW	0x00	gpio1b_pos_int_en gpio1b posedge pulse interrupt enable 0: disable 1: enable
7:0	RW	0x00	gpio1a_pos_int_en gpio1a posedge pulse interrupt enable 0: disable 1: enable

PMU_GPIO1_NEG_INT_CON
Address: Operational Base + offset (0x003c)
pmu gpio1 negedge interrupt configure register

Bit	Attr	Reset Value	Description
31:24	RW	0x00	gpio1d_neg_int_en gpio1d negedge pulse interrupt enable 0: disable 1: enable
23:16	RW	0x00	gpio1c_neg_int_en gpio1c negedge pulse interrupt enable 0: disable 1: enable
15:8	RW	0x00	gpio1b_neg_int_en gpio1b negedge pulse interrupt enable 0: disable 1: enable
7:0	RW	0x00	gpio1a_neg_int_en gpio1a negedge pulse interrupt enable 0: disable 1: enable

PMU_GPIO0_POS_INT_ST
Address: Operational Base + offset (0x0040)
pmu gpio0 posedge interrupt status register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:24	RW	0x00	gpio0d_pos_int_status gpio0d posedge pulse interrupt status 0: not wakeup by gpio0d posedge pulse 1: wakeup by gpio0d posedge pulse
23:16	RW	0x00	gpio0c_pos_int_status gpio0c posedge pulse interrupt status 0: not wakeup by gpio0c posedge pulse 1: wakeup by gpio0c posedge pulse
15:8	RW	0x00	gpio0b_pos_int_status gpio0b posedge pulse interrupt status 0: not wakeup by gpio0b posedge pulse 1: wakeup by gpio0b posedge pulse
7:0	RW	0x00	gpio0a_pos_int_status gpio0a posedge pulse interrupt status 0: not wakeup by gpio0a posedge pulse 1: wakeup by gpio0a posedge pulse

PMU_GPIO0_NEG_INT_ST
Address: Operational Base + offset (0x0044)
pmu gpio0 negedge interrupt status register

Bit	Attr	Reset Value	Description
31:24	RW	0x00	gpio0d_neg_int_status gpio0d negedge pulse interrupt status 0: not wakeup by gpio0d negedge pulse 1: wakeup by gpio0d negedge pulse
23:16	RW	0x00	gpio0c_neg_int_status gpio0c negedge pulse interrupt status 0: not wakeup by gpio0c negedge pulse 1: wakeup by gpio0c negedge pulse
15:8	RW	0x00	gpio0b_neg_int_status gpio0b negedge pulse interrupt status 0: not wakeup by gpio0b negedge pulse 1: wakeup by gpio0b negedge pulse
7:0	RW	0x00	gpio0a_neg_int_status gpio0a negedge pulse interrupt status 0: not wakeup by gpio0a negedge pulse 1: wakeup by gpio0a negedge pulse

PMU_GPIO1_POS_INT_ST
Address: Operational Base + offset (0x0048)
pmu gpio1 posedge interrupt status register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:24	RW	0x00	gpio1d_pos_int_status gpio1d posedge pulse interrupt status 0: not wakeup by gpio1d posedge pulse 1: wakeup by gpio1d posedge pulse
23:16	RW	0x00	gpio1c_pos_int_status gpio1c posedge pulse interrupt status 0: not wakeup by gpio1c posedge pulse 1: wakeup by gpio1c posedge pulse
15:8	RW	0x00	gpio1b_pos_int_status gpio1b posedge pulse interrupt status 0: not wakeup by gpio1b posedge pulse 1: wakeup by gpio1b posedge pulse
7:0	RW	0x00	gpio1a_pos_int_status gpio1a posedge pulse interrupt status 0: not wakeup by gpio1a posedge pulse 1: wakeup by gpio1a posedge pulse

PMU_GPIO1_NEG_INT_ST
Address: Operational Base + offset (0x004c)
pmu gpio1 negedge interrupt status register

Bit	Attr	Reset Value	Description
31:24	RW	0x00	gpio1d_neg_int_status gpio1d negedge pulse interrupt status 0: not wakeup by gpio1d negedge pulse 1: wakeup by gpio1d negedge pulse
23:16	RW	0x00	gpio1c_neg_int_status gpio1c negedge pulse interrupt status 0: not wakeup by gpio1c negedge pulse 1: wakeup by gpio1c negedge pulse
15:8	RW	0x00	gpio1b_neg_int_status gpio1b negedge pulse interrupt status 0: not wakeup by gpio1b negedge pulse 1: wakeup by gpio1b negedge pulse
7:0	RW	0x00	gpio1a_neg_int_status gpio1a negedge pulse interrupt status 0: not wakeup by gpio1a negedge pulse 1: wakeup by gpio1a negedge pulse

PMU_PWRDN_INTEN
Address: Operational Base + offset (0x0050)
pmu power down configure register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31	RW	0x0	pd_sdioaudio_pwr_switch_int_en pd_sdioaudio power switch interrupt enable 0: disable 1: enable
30	RW	0x0	pd_sd_pwr_switch_int_en pd_sd power switch interrupt enable 0: disable 1: enable
29	RW	0x0	pd_gic_pwr_switch_int_en pd_gic power switch interrupt enable 0: disable 1: enable
28	RW	0x0	pd_edp_pwr_switch_int_en pd_edp power switch interrupt enable 0: disable 1: enable
27	RW	0x0	pd_usb3_pwr_switch_interrupt_en pd_usb3 power switch interrupt enable 0: disable 1: enable
26	RW	0x0	pd_emmc_pwr_switch_interrupt_en pd_emmc power switch interrupt enable 0: disable 1: enable
25	RW	0x0	pd_gmac_pwr_switch_int_en pd_gmac power switch interrupt enable 0: disable 1: enable
24	RW	0x0	pd_hdcp_pwr_switch_int_en pd_hdcp power switch interrupt enable 0: disable 1: enable
23	RW	0x0	pd_isp1_pwr_switch_int_en pd_isp1 power switch interrupt enable 0: disable 1: enable
22	RW	0x0	pd_isp0_pwr_switch_int_en pd_isp0 power switch interrupt enable 0: disable 1: enable
21	RO	0x0	reserved
20	RW	0x0	pd_vo_pwr_switch_int_en pd_vo power switch interrupt enable 0: disable 1: enable

Bit	Attr	Reset Value	Description
19	RW	0x0	pd_iep_pwr_switch_int_en pd_perihp power switch interrupt enable 0: disable 1: enable
18	RW	0x0	pd_rga_pwr_switch_int_en pd_rga power switch interrupt enable 0: disable 1: enable
17	RW	0x0	pd_vdu_pwr_switch_int_en pd_vdu power switch interrupt enable 0: disable 1: enable
16	RW	0x0	pd_vcodec_pwr_switch_inten pd_perihp power switch interrupt enable 0: disable 1: enable
15	RW	0x0	pd_gpu_pwr_switch_int_en pd_gpu power interrupt enable 0: disable 1: enable
14	RW	0x0	pd_vio_pwr_switch_int_en pd_vio power switch interrupt enable 0: disable 1: enable
13	RW	0x0	pd_center_pwr_switch_int_en pd_center power switch interrupt enable 0: disable 1: enable
12	RW	0x0	pd_perihp_pwr_switch_int_en pd_perihp power switch interrupt enable 0: disable 1: enable
11	RW	0x0	pd_perilp_pwr_switch_int_en pd_perilp power switch interrupt enable 0: disable 1: enable
10	RW	0x0	pd_cci_pwr_switch_int_en pd_cci power switch interrupt enable 0: disable 1: enable
9	RW	0x0	pd_tcpd1_pwr_switch_int_en pd_tcpd1 power switch interrupt enable 0: disable 1: enable

Bit	Attr	Reset Value	Description
8	RW	0x0	pd_tcpd0_pwr_switch_int_en pd_tcpd0 power switch interrupt enable 0: disable 1: enable
7	RW	0x0	pd_scu_b_pwr_switch_int_en pd_scu_b power switch interrupt enable 0: disable 1: enable
6	RW	0x0	pd_scu_l_pwr_switch_int_en pd_scu_l power switch interrupt enable 0: disable 1: enable
5	RW	0x0	pd_a72_b1_pwr_switch_int_en pd_a72_b1 power switch interrupt enable 0: disable 1: enable
4	RW	0x0	pd_a72_b0_pwr_switch_int_en pd_a72_b0 power enable 0: disable 1: enable
3	RW	0x0	pd_a53_l3_pwr_switch_int_en pd_a53_l3 power switch int enable 0: disable 1: enable
2	RW	0x0	pd_a53_l2_pwr_switch_int_en pd_a53_l2 power switch interrupt enable 0: disable 1: enable
1	RW	0x0	pd_a53_l1_pwr_switch_int_en pd_a53_l1 power switch interrupt enable 0: disable 1: enable
0	RW	0x0	pd_a53_l0_pwr_switch_int_en pd_a53_l0 power switch interrupt enable 0: disable 1: enable

PMU_PWRDN_STATUS

Address: Operational Base + offset (0x0054)

pmu power down status register

Bit	Attr	Reset Value	Description
31	W1C	0x0	pd_sdioaudio_pwr_stat pd_sdioaudio power state 0: powered up 1: powered down

Bit	Attr	Reset Value	Description
30	W1C	0x0	pd_sd_pwr_stat pd_sd power state 0: powered up 1: powered down
29	W1C	0x0	pd_gic_pwr_stat pd_gic power state 0: powered up 1: powered down
28	W1C	0x0	pd_edp_pwr_stat pd_edp power state 0: powered up 1: powered down
27	W1C	0x0	pd_usb3_pwr_stat pd_usb3 power state 0: powered up 1: powered down
26	W1C	0x0	pd_emmc_pwr_stat pd_emmc power state 0: powered up 1: powered down
25	W1C	0x0	pd_gmac_pwr_stat pd_gmac power state 0: powered up 1: powered down
24	W1C	0x0	pd_hdcp_pwr_stat pd_hdcp power state 0: powered up 1: powered down
23	W1C	0x0	pd_isp1_pwr_stat pd_isp1 power state 0: powered up 1: powered down
22	W1C	0x0	pd_isp0_pwr_stat pd_isp0 power state 0: powered up 1: powered down
21	RO	0x0	reserved
20	W1C	0x0	pd_vo_pwr_stat pd_vo power state 0: powered up 1: powered down
19	W1C	0x0	pd_iep_pwr_stat pd_iep power state 0: powered up 1: powered down

Bit	Attr	Reset Value	Description
18	W1C	0x0	pd_rga_pwr_stat pd_rga power state 0: powered up 1: powered down
17	W1C	0x0	pd_vdu_pwr_stat pd_vdu power state 0: powered up 1: powered down
16	W1C	0x0	pd_vcodec_pwr_stat pd_vcodec power state 0: powered up 1: powered down
15	W1C	0x0	pd_gpu_pwr_stat pd_gpu power state 0: powered up 1: powered down
14	W1C	0x0	pd_vio_pwr_stat pd_vio power state 0: powered up 1: powered down
13	W1C	0x0	pd_center_pwr_stat pd_center power state 0: powered up 1: powered down
12	W1C	0x0	pd_perihp_pwr_stat pd_perihp power state 0: powered up 1: powered down
11	W1C	0x0	pd_perilp_pwr_stat pd_perilp power stat 0: powered up 1: powered down
10	W1C	0x0	pd_cci_pwr_stat pd_core power state 0: powered up 1: powered down
9	W1C	0x0	pd_tcpd1_pwr_stat pd_tcpd1 power state 0: powered up 1: powered down
8	W1C	0x0	pd_tcpd0_pwr_stat pd_tcpd0 power state 0: powered up 1: powered down

Bit	Attr	Reset Value	Description
7	W1C	0x0	pd_scu_b_pwr_stat pd_scu_b power state 0: powered up 1: powered down
6	W1C	0x0	pd_scu_l_pwr_stat pd_scu_l power state 0: powered up 1: powered down
5	W1C	0x0	pd_a72_b1_pwr_stat pd_a72_b1 power state 0: powered up 1: powered down
4	W1C	0x0	pd_a72_b0_pwr_stat pd_a72_b0 power state 0: powered up 1: powered down
3	W1C	0x0	pd_a53_l3_pwr_stat pd_a53_l3 power state 0: powered up 1: powered down
2	W1C	0x0	pd_a53_l2_pwr_stat pd_a53_l2 power state 0: powered up 1: powered down
1	W1C	0x0	pd_a53_l1_pwr_stat pd_a53_l1 power state 0: powered up 1: powered down
0	W1C	0x0	pd_a53_l0_pwr_stat pd_a53_l0 power state 0: powered up 1: powered down

PMU_WAKEUP_STATUS

Address: Operational Base + offset (0x0058)

pmu interrupt status register

Bit	Attr	Reset Value	Description
31:14	RO	0x0	reserved
13	RW	0x0	wakeup_pcie_status pcie wakeup status 0: not wakeup by pcie 1: wakeup by pcie
12	RO	0x0	reserved

Bit	Attr	Reset Value	Description
11	RW	0x0	wakeup_pwm_status pwm wakeup status 0: not wakeup by pwm 1: wakeup by pwm
10	RW	0x0	wakeup_timeout_status timeout wakeup status 0: not wakeup by timeout 1: wakeup by timeout
9	RW	0x0	wakeup_wdt_m0_status m0 wdt interrupt wakeup status 0: not wakeup by m0 wdt interrupt 1: wakeup by m0 wdt interrupt
8	RW	0x0	wakeup_sft_m0_status m0 software control wakeup status 0: not wakeup by software 1: wakeup by software
7	RW	0x0	wakeup_usbdev_status usbdev detect wakeup status 0: not wakeup by usbdev detect 1: wakeup by usbdev detect
6	RW	0x0	wakeup_timer_status timer wakeup status 0: not wakeup by timer 1: wakeup by timer
5	RO	0x0	reserved
4	RW	0x0	wakeup_sdmmc_status sdmmc wakeup status 0: not wakeup by sdmmc detect 1: wakeup by sdmmc detect
3	RW	0x0	wakeup_sdio_status sdio wakeup status 0: not wakeup by sdio detect 1: wakeup by sdio detect
2	RW	0x0	wakeup_gpio_int_status gpio interrupt wakeup status 0: not wakeup by gpio int 1: wakeup by gpio int
1	RW	0x0	wakeup_int_cluster_b_status cluster_b interrupt wakeup status 0: not wakeup by interrupt cluster_b 1: wakeup by interrupt cluster_b
0	RW	0x0	wakeup_int_cluster_l_status cluster_l interrupt wakeup status 0: not wakeup by interrupt cluster_l 1: wakeup by interrupt cluster_l

PMU_BUS_CLR
Address: Operational Base + offset (0x005c)
pmu bus clear register

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	clr_sdioaudio send idle request to sdioaudio low power interface 0: disable 1: enable
28	RW	0x0	clr_sd send idle request to sd low power interface 0: disable 1: enable
27	RW	0x0	clr_gic send idle request to gic low power interface 0: disable 1: enable
26	RW	0x0	clr_pmum0 send idle request to pmu m0 low power interface 0: disable 1: enable
25	RW	0x0	clr_center1 send idle request to center1 low power interface 0: disable 1: enable
24	RW	0x0	clr_emmc send idle request to emmc low power interface 0: disable 1: enable
23	RW	0x0	clr_gmac send idle request to gmac low power interface 0: disable 1: enable
22	RW	0x0	clr_edp send idle request to edp low power interface 0: disable 1: enable
21	RW	0x0	clr_pmu send idle request to pmu low power interface 0: disable 1: enable
20	RW	0x0	clr_alive send idle request to alive low power interface 0: disable 1: enable

Bit	Attr	Reset Value	Description
19	RW	0x0	clr_msch1 send idle request to msch1 low power interface 0: disable 1: enable
18	RW	0x0	clr_msch0 send idle request to msch0 low power interface 0: disable 1: enable
17	RW	0x0	clr_vio send idle request to vio low power interface 0: disable 1: enable
16	RW	0x0	clr_ccim0 send idle request to ccim0 low power interface 0: disable 1: enable
15	RW	0x0	clr_ccim1 send idle request to ccim1 low power interface 0: disable 1: enable
14	RW	0x0	clr_center send idle request to center niu 0: disable 1: enable
13	RW	0x0	clr_perilpm0 send idle request to perilp m0 niu 0: disable 1: enable
12	RW	0x0	clr_usb3 send idle request to usb3 niu 0: disable 1: enable
11	RW	0x0	clr_hdcp send idle request to hdcp niu 0: disable 1: enable
10	RW	0x0	clr_isp1 send idle request to isp1 niu 0: disable 1: enable
9	RW	0x0	clr_isp0 send idle request to isp0 niu 0: disable 1: enable

Bit	Attr	Reset Value	Description
8	RW	0x0	clr_vopl send idle request to vopl niu 0: disable 1: enable
7	RW	0x0	clr_vopb send idle request to vopb niu 0: disable 1: enable
6	RW	0x0	clr_iep send idle request to iep niu 0: disable 1: enable
5	RW	0x0	clr_rga send idle request to rga niu 0: disable 1: enable
4	RW	0x0	clr_vdu send idle request to vdu niu 0: disable 1: enable
3	RW	0x0	clr_vcodec send idle request to vcodec niu 0: disable 1: enable
2	RW	0x0	clr_perihp send idle request to perihp niu 0: disable 1: enable
1	RW	0x0	clr_perilp send idle request to perilp niu 0: disable 1: enable
0	RW	0x0	clr_gpu send idle request to gpu niu 0: disable 1: enable

PMU_BUS_IDLE_REQ
Address: Operational Base + offset (0x0060)
pmu bus idle request register

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

Bit	Attr	Reset Value	Description
29	RW	0x0	idle_req_sdioaudio send idle request to sdioaudio low power interface 0: disable 1: enable
28	RW	0x0	idle_req_sd send idle request to sd low power interface 0: disable 1: enable
27	RW	0x0	idle_req_gic send idle request to gic low power interface 0: disable 1: enable
26	RW	0x0	idle_req_pmum0 send idle request to pmu m0 low power interface 0: disable 1: enable
25	RW	0x0	idle_req_center1 send idle request to center1 low power interface 0: disable 1: enable
24	RW	0x0	idle_req_emmc send idle request to emmc low power interface 0: disable 1: enable
23	RW	0x0	idle_req_gmac send idle request to gmac low power interface 0: disable 1: enable
22	RW	0x0	idle_req_edp send idle request to edp low power interface 0: disable 1: enable
21	RW	0x0	idle_req_pmu send idle request to pmu low power interface 0: disable 1: enable
20	RW	0x0	idle_req_alive send idle request to alive low power interface 0: disable 1: enable
19	RW	0x0	idle_req_msch1 send idle request to msch1 low power interface 0: disable 1: enable

Bit	Attr	Reset Value	Description
18	RW	0x0	idle_req_msch0 send idle request to msch0 low power interface 0: disable 1: enable
17	RW	0x0	idle_req_vio send idle request to vio low power interface 0: disable 1: enable
16	RW	0x0	idle_req_ccim1 send idle request to ccim1 low power interface 0: disable 1: enable
15	RW	0x0	idle_req_ccim0 send idle request to ccim0 low power interface 0: disable 1: enable
14	RW	0x0	idle_req_center send idle request to center niu 0: disable 1: enable
13	RW	0x0	idle_req_perilpm0 send idle request to perilp m0 niu 0: disable 1: enable
12	RW	0x0	idle_req_usb3 send idle request to usb3 niu 0: disable 1: enable
11	RW	0x0	idle_req_hdcp send idle request to hdcp niu 0: disable 1: enable
10	RW	0x0	idle_req_isp1 send idle request to isp1 niu 0: disable 1: enable
9	RW	0x0	idle_req_isp0 send idle request to isp0 niu 0: disable 1: enable
8	RW	0x0	idle_req_vopl send idle request to vopl niu 0: disable 1: enable

Bit	Attr	Reset Value	Description
7	RW	0x0	idle_req_vopb send idle request to vopb niu 0: disable 1: enable
6	RW	0x0	idle_req_iep send idle request to iep niu 0: disable 1: enable
5	RW	0x0	idle_req_rga send idle request to rga niu 0: disable 1: enable
4	RW	0x0	idle_req_vdu send idle request to vdu niu 0: disable 1: enable
3	RW	0x0	idle_req_vcodec send idle request to vcodec niu 0: disable 1: enable
2	RW	0x0	idle_req_perihp send idle request to perihp niu 0: disable 1: enable
1	RW	0x0	idle_req_perilp send idle request to perilp niu 0: disable 1: enable
0	RW	0x0	idle_req_gpu send idle request to gpu niu 0: disable 1: enable

PMU_BUS_IDLE_ST
Address: Operational Base + offset (0x0064)
pmu bus idle status register

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RO	0x0	idle_sdioaudio send idle request to sdioaudio low power interface 0: disable 1: enable

Bit	Attr	Reset Value	Description
28	RO	0x0	idle_sd send idle request to sd low power interface 0: disable 1: enable
27	RO	0x0	idle_gic idle status of gic niu 0: idle status of niu is 0 1: idle status of niu is 1
26	RO	0x0	idle_pmum0 idle status of pmu m0 niu 0: idle status of niu is 0 1: idle status of niu is 1
25	RO	0x0	idle_center1 idle status of center1 niu 0: idle status of niu is 0 1: idle status of niu is 1
24	RO	0x0	idle_emmc idle status of emmc niu 0: idle status of niu is 0 1: idle status of niu is 1
23	RO	0x0	idle_gmac idle status of gmac niu 0: idle status of niu is 0 1: idle status of niu is 1
22	RO	0x0	idle_edp idle status of edp niu 0: idle status of niu is 0 1: idle status of niu is 1
21	RO	0x0	idle_pmu idle status of pmu niu 0: idle status of niu is 0 1: idle status of niu is 1
20	RO	0x0	idle_alive idle status of alive niu 0: idle status of niu is 0 1: idle status of niu is 1
19	RO	0x0	idle_msch1 idle status of msch1 niu 0: idle status of niu is 0 1: idle status of niu is 1
18	RO	0x0	idle_msch0 idle status of msch0 niu 0: idle status of niu is 0 1: idle status of niu is 1

Bit	Attr	Reset Value	Description
17	RO	0x0	idle_vio idle status of vio niu 0: idle status of niu is 0 1: idle status of niu is 1
16	RO	0x0	idle_ccim1 idle status of ccim1 niu 0: idle status of niu is 0 1: idle status of niu is 1
15	RO	0x0	idle_ccim0 idle status of ccim0 niu 0: idle status of niu is 0 1: idle status of niu is 1
14	RO	0x0	idle_center idle status of center niu 0: idle status of niu is 0 1: idle status of niu is 1
13	RO	0x0	idle_perilpm0 idle status of perilpm0 niu 0: idle status of niu is 0 1: idle status of niu is 1
12	RO	0x0	idle_usb3 idle status of usb3 niu 0: idle status of niu is 0 1: idle status of niu is 1
11	RO	0x0	idle_hdcp idle status of hdcp niu 0: idle status of niu is 0 1: idle status of niu is 1
10	RO	0x0	idle_isp1 idle status of isp1 niu 0: idle status of niu is 0 1: idle status of niu is 1
9	RO	0x0	idle_isp0 idle status of isp0 niu 0: idle status of niu is 0 1: idle status of niu is 1
8	RO	0x0	idle_vopl idle status of vopl niu 0: idle status of niu is 0 1: idle status of niu is 1
7	RO	0x0	idle_vopb idle status of vopb niu 0: idle status of niu is 0 1: idle status of niu is 1

Bit	Attr	Reset Value	Description
6	RO	0x0	idle_iep idle status of iep niu 0: idle status of niu is 0 1: idle status of niu is 1
5	RO	0x0	idle_rga idle status of rga niu 0: idle status of niu is 0 1: idle status of niu is 1
4	RO	0x0	idle_vdu idle status of vdu niu 0: idle status of niu is 0 1: idle status of niu is 1
3	RO	0x0	idle_vcodec idle status of vcodec niu 0: idle status of niu is 0 1: idle status of niu is 1
2	RO	0x0	idle_perihp idle status of perihp niu 0: idle status of niu is 0 1: idle status of niu is 1
1	RO	0x0	idle_perilp idle status of perilp niu 0: idle status of niu is 0 1: idle status of niu is 1
0	RO	0x0	idle_gpu idle status of gpu niu 0: idle status of gpu_niu is 0 1: idle status of gpu_niu is 1

PMU_BUS_IDLE_ACK
Address: Operational Base + offset (0x0068)
pmu bus idle ack status register

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RO	0x0	idle_ack_sdioaudio idle acknowledge status from sdioaudio niu 0: idle acknowledge status of niu is 0 1: idle acknowledge status of niu is 1
28	RO	0x0	idle_ack_sd idle acknowledge status from sd niu 0: idle acknowledge status of niu is 0 1: idle acknowledge status of niu is 1

Bit	Attr	Reset Value	Description
27	RO	0x0	idle_ack_gic idle acknowledge status from gic niu 0: idle acknowledge status of niu is 0 1: idle acknowledge status of niu is 1
26	RO	0x0	idle_ack_pmum0 idle acknowledge status from pmu m0 niu 0: idle acknowledge status of niu is 0 1: idle acknowledge status of niu is 1
25	RO	0x0	idle_ack_center1 idle acknowledge status from center1 niu 0: idle acknowledge status of niu is 0 1: idle acknowledge status of niu is 1
24	RO	0x0	idle_ack_emmc idle acknowledge status from emmc niu 0: idle acknowledge status of niu is 0 1: idle acknowledge status of niu is 1
23	RO	0x0	idle_ack_gmac idle acknowledge status from gmac niu 0: idle acknowledge status of niu is 0 1: idle acknowledge status of niu is 1
22	RO	0x0	idle_ack_edp idle acknowledge status from edp niu 0: idle acknowledge status of niu is 0 1: idle acknowledge status of niu is 1
21	RO	0x0	idle_ack_pmu idle acknowledge status from pmu niu 0: idle acknowledge status of niu is 0 1: idle acknowledge status of niu is 1
20	RO	0x0	idle_ack_alive idle acknowledge status from alive niu 0: idle acknowledge status of niu is 0 1: idle acknowledge status of niu is 1
19	RO	0x0	idle_ack_msch1 idle acknowledge status from msch1 niu 0: idle acknowledge status of niu is 0 1: idle acknowledge status of niu is 1
18	RO	0x0	idle_ack_msch0 idle acknowledge status from msch0 niu 0: idle acknowledge status of niu is 0 1: idle acknowledge status of niu is 1
17	RO	0x0	idle_ack_vio idle acknowledge status from vio niu 0: idle acknowledge status of niu is 0 1: idle acknowledge status of niu is 1

Bit	Attr	Reset Value	Description
16	RO	0x0	idle_ack_ccim1 idle acknowledge status from ccim1 niu 0: idle acknowledge status of niu is 0 1: idle acknowledge status of niu is 1
15	RO	0x0	idle_ack_ccim0 idle acknowledge status from ccim0 niu 0: idle acknowledge status of niu is 0 1: idle acknowledge status of niu is 1
14	RO	0x0	idle_ack_center idle acknowledge status from center niu 0: idle acknowledge status of niu is 0 1: idle acknowledge status of niu is 1
13	RO	0x0	idle_ack_perilpm0 idle acknowledge status from perilp m0 niu 0: idle acknowledge status of niu is 0 1: idle acknowledge status of niu is 1
12	RO	0x0	idle_ack_usb3 idle acknowledge status from usb3 niu 0: idle acknowledge status of niu is 0 1: idle acknowledge status of niu is 1
11	RO	0x0	idle_ack_hdcp idle acknowledge status from hdcp niu 0: idle acknowledge status of niu is 0 1: idle acknowledge status of niu is 1
10	RO	0x0	idle_ack_isp1 idle acknowledge status from isp1 niu 0: idle acknowledge status of niu is 0 1: idle acknowledge status of niu is 1
9	RO	0x0	idle_ack_isp0 idle acknowledge status from isp0 niu 0: idle acknowledge status of niu is 0 1: idle acknowledge status of niu is 1
8	RO	0x0	idle_ack_vopl idle acknowledge status from vopl niu 0: idle acknowledge status of niu is 0 1: idle acknowledge status of niu is 1
7	RO	0x0	idle_ack_vopb idle acknowledge status from vopb niu 0: idle acknowledge status of niu is 0 1: idle acknowledge status of niu is 1
6	RO	0x0	idle_ack_iep idle acknowledge status from iep niu 0: idle acknowledge status of niu is 0 1: idle acknowledge status of niu is 1

Bit	Attr	Reset Value	Description
5	RO	0x0	idle_ack_rga idle acknowledge status from rga niu 0: idle acknowledge status of niu is 0 1: idle acknowledge status of niu is 1
4	RO	0x0	idle_ack_vdu idle acknowledge status from vdu niu 0: idle acknowledge status of niu is 0 1: idle acknowledge status of niu is 1
3	RO	0x0	idle_ack_vcodec idle acknowledge status from vcodec niu 0: idle acknowledge status of niu is 0 1: idle acknowledge status of niu is 1
2	RO	0x0	idle_ack_perihp idle acknowledge status from perihp niu 0: idle acknowledge status of niu is 0 1: idle acknowledge status of niu is 1
1	RO	0x0	idle_ack_perilp idle acknowledge status from perilp niu 0: idle acknowledge status of niu is 0 1: idle acknowledge status of niu is 1
0	RO	0x0	idle_ack_gpu idle acknowledge status from gpu niu 0: idle acknowledge status of niu is 0 1: idle acknowledge status of niu is 1

PMU_CCI500_CON
Address: Operational Base + offset (0x006c)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RO	0x0	reserved
7	RW	0x0	qgating_cci500_cfg CCI-500 Q-channel clock gating enable.
6	RW	0x0	clr_qreq_cci500 CCI-500 Q-channel request sent by hardware.
5	RW	0x0	qreq_cci500_cfg CCI-500 Q-channel request sent by software.

Bit	Attr	Reset Value	Description
4:2	RW	0x0	pstate_cci500 CCI-500 P-channel pstate .
1	RW	0x0	clr_preq_cci500 CCI-500 P-channel request sent by hardware .
0	RW	0x0	preq_cci500_cfg CCI-500 P-channel request sent by software

PMU_ADB400_CON
Address: Operational Base + offset (0x0070)

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RO	0x0	reserved
14	RW	0x0	clr_gic2_core_b hardware send idle request to path from gic to core_b low power interface 0: disable 1: enable
13	RW	0x0	clr_core_b_2gic hardware send idle request to path from core_b to gic low power interface 0: disable 1: enable
12	RW	0x0	clr_core_b hardware send idle request from core_b to cci low power interface 0: disable 1: enable
11	RW	0x0	clr_gic2_core_l hardware send idle request to path from gic to core_l low power interface 0: disable 1: enable
10	RW	0x0	clr_core_l_2gic hardware send idle request to path from core_l to gic low power interface 0: disable 1: enable

Bit	Attr	Reset Value	Description
9	RW	0x0	clr_core_l software send idle request from core_l to cci low power interface 0: disable 1: enable
8	RW	0x0	clr_cxcs hardware send idle request to cxcs low power interface 0: disable 1: enable
7	RO	0x0	reserved
6	RW	0x0	pwrdwn_req_gic2_core_b send idle request to path from gic to core_b low power interface 0: disable 1: enable
5	RW	0x0	pwrdwn_req_core_b_2gic software send idle request to path from core_b to gic low power interface 0: disable 1: enable
4	RW	0x0	pwrdwn_req_core_b software send idle request from core_b to cci low power interface 0: disable 1: enable
3	RW	0x0	pwrdwn_req_gic2_core_l send idle request to path from gic to core_l low power interface 0: disable 1: enable
2	RW	0x0	pwrdwn_req_core_l_2gic software send idle request to path from core_l to gic low power interface 0: disable 1: enable
1	RW	0x0	pwrdwn_req_core_l software send idle request from core_l to cci low power interface 0: disable 1: enable
0	RW	0x0	pwrdwn_req_cxcs software send idle request to cxcs low power interface 0: disable 1: enable

PMU_ADB400_ST
Address: Operational Base + offset (0x0074)

Bit	Attr	Reset Value	Description
31:15	RO	0x0	reserved

Bit	Attr	Reset Value	Description
14	RO	0x0	idle_gic2_core_b active status of cxcs low power interface 0: active status is 0 (inactive) 1: active status is 1 (active)
13	RO	0x0	idle_core_b_2gic active status of cxcs low power interface 0: active status is 0 (inactive) 1: active status is 1 (active)
12	RO	0x0	idle_core_b active status of cxcs low power interface 0: active status is 0 (inactive) 1: active status is 1 (active)
11	WO	0x0	idle_gic2_core_l active status of cxcs low power interface 0: active status is 0 (inactive) 1: active status is 1 (active)
10	RO	0x0	idle_core_l_2gic active status of cxcs low power interface 0: active status is 0 (inactive) 1: active status is 1 (active)
9	RO	0x0	idle_core_l active status of cxcs low power interface 0: active status is 0 (inactive) 1: active status is 1 (active)
8	RO	0x0	active_cxcs active status of cxcs low power interface 0: active status is 0 (inactive) 1: active status is 1 (active)
7	RO	0x0	reserved
6	RO	0x0	pwrdwn_ack_gic2_core_b idle acknowledge status from cxcs 0: idle acknowledge status of adb is 0 1: idle acknowledge status of adb is 1
5	RO	0x0	pwrdwn_ack_core_b_2gic idle acknowledge status from cxcs 0: idle acknowledge status of adb is 0 1: idle acknowledge status of adb is 1
4	RO	0x0	pwrdwn_ack_core_b idle acknowledge status from cxcs 0: idle acknowledge status of adb is 0 1: idle acknowledge status of adb is 1
3	RO	0x0	pwrdwn_ack_gic2_core_l idle acknowledge status from cxcs 0: idle acknowledge status of adb is 0 1: idle acknowledge status of adb is 1

Bit	Attr	Reset Value	Description
2	RO	0x0	pwrdwn_ack_core_l_2gic idle acknowledge status from cxcs 0: idle acknowledge status of adb is 0 1: idle acknowledge status of adb is 1
1	RO	0x0	pwrdwn_ack_core_l idle acknowledge status from cxcs 0: idle acknowledge status of adb is 0 1: idle acknowledge status of adb is 1
0	RO	0x0	pwrdwn_ack_cxcs idle acknowledge status from cxcs 0: idle acknowledge status of adb is 0 1: idle acknowledge status of adb is 1

PMU_POWER_ST
Address: Operational Base + offset (0x0078)
pmu power status register

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6:0	RW	0x00	power_state power state of pmu FSM

PMU_CORE_PWR_ST
Address: Operational Base + offset (0x007c)
pmu core power status register

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RO	0x0	qacceptn_cci500 CCI-500 Q-channel accept signal, active low
28	RO	0x0	qdeny_cci500 CCI-500 Q-channel deny signal, active high
27	RO	0x0	qactive_cci500 CCI-500 Q-channel active signal, active high
26	RO	0x0	paccept_cci500 CCI-500 P-channel accept signal, active high
25	RO	0x0	pdeny_cci500 CCI-500 P-channel deny signal, active high
24:20	RO	0x00	pactive_cci500 CCI-500 P-channel active signal, active high
19:18	RO	0x0	reserved
17:16	RO	0x0	standbywfi_cluster_b standbywfi status of cluster_b 0: cluster_b standbywfi status is 0 1: cluster_b standbywfi status is 1
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13:12	RO	0x0	standbywfe_cluster_b standbywfe status of cluster_b 0: cluster_b standbywfe status is 0 1: cluster_b standbywfe status is 1
11	RO	0x0	standbywfil2_cluster_b standbywfil2 status of cluster_b 0: cluster_b standbywfil2 status is 0 1: cluster_b standbywfil2 status is 1
10	RO	0x0	l2flushdone_cluster_b l2flushdone status of cluster_b 0: cluster_b l2flushdone status is 0 1: cluster_b l2flushdone status is 1
9:6	RO	0x0	standbywfi_cluster_l standbywfi status of cluster_l 0: cluster_l standbywfi status is 0 1: cluster_l standbywfi status is 1
5:2	RO	0x0	standbywfe_cluster_l standbywfe status of cluster_l 0: cluster_l standbywfe status is 0 1: cluster_l standbywfe status is 1
1	RO	0x0	standbywfil2_cluster_l standbywfil2 status of cluster_l 0: cluster_l standbywfil2 status is 0 1: cluster_l standbywfil2 status is 1
0	RO	0x0	l2flushdone_cluster_l l2flushdone status of cluster_l 0: cluster_l l2flushdone status is 0 1: cluster_l l2flushdone status is 1

PMU_OSC_CNT
Address: Operational Base + offset (0x0080)
pmu osc count register

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x00000	pmu_osc_cnt pmu osc stable counter value

PMU_PLLLOCK_CNT
Address: Operational Base + offset (0x0084)
pmu pll lock count register

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x00000	pmu_plllock_cnt pmu pll lock counter value

PMU_PLLRST_CNT
Address: Operational Base + offset (0x0088)
pmu pll reset count register

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x00000	pmu_pllrst_cnt pmu pll reset counter value

PMU_STABLE_CNT
Address: Operational Base + offset (0x008c)
pmu power stable count register

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x00000	pmu_stable_cnt pmu PMIC stable counter value

PMU_DDRIO_PWRON_CNT
Address: Operational Base + offset (0x0090)
pmu ddrio power on count register

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x00000	pmu_ddrio_pwron_cnt pmu ddrio power on counter value

PMU_WAKEUP_RST_CLR_CNT
Address: Operational Base + offset (0x0094)
pmu wakeup reset clear count register

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x00000	pmu_wakeup_rst_cnt pmu wakeup reset counter value

PMU_DDR_SREF_ST
Address: Operational Base + offset (0x0098)
pmu ddr self refresh status register

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2	RW	0x0	ddrc1_sref_done_ext ddr controller 1 self re-fresh done, active high
1	RO	0x0	reserved
0	RW	0x0	ddrc0_sref_done_ext ddr controller 0 self re-fresh done, active high

PMU_SCU_L_PWRDN_CNT
Address: Operational Base + offset (0x009c)

pmu scu_l power down count register

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x05dc0	pmu_scu_l_pwrdn_cnt pmu scu_l power down counter value

PMU_SCU_L_PWRUP_CNT
Address: Operational Base + offset (0x00a0)
pmu scu_l power up count register

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x05dc0	pmu_scu_l_pwrup_cnt pmu scu_l power up counter value

PMU_SCU_B_PWRDN_CNT
Address: Operational Base + offset (0x00a4)
pmu scu_b power down count register

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x05dc0	pmu_scu_b_pwrdn_cnt pmu scu_b power down counter value

PMU_SCU_B_PWRUP_CNT
Address: Operational Base + offset (0x00a8)
pmu scu_b power up count register

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x05dc0	pmu_scu_b_pwrup_cnt pmu scu_b power up counter value

PMU_GPU_PWRDN_CNT
Address: Operational Base + offset (0x00ac)
pmu gpu power down count register

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x05dc0	pmu_gpu_pwrdn_cnt pmu gpu power down counter value

PMU_GPU_PWRUP_CNT
Address: Operational Base + offset (0x00b0)
pmu gpu power up count register

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x05dc0	pmu_gpu_pwrup_cnt pmu gpu power up counter value

PMU_CENTER_PWRDN_CNT
Address: Operational Base + offset (0x00b4)
pmu center power down count register

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x05dc0	pmu_center_pwrdn_cnt pmu center power down counter value

PMU_CENTER_PWRUP_CNT
Address: Operational Base + offset (0x00b8)
pmu center power up count register

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x05dc0	pmu_center_pwrup_cnt pmu center power up counter value

PMU_TIMEOUT_CNT
Address: Operational Base + offset (0x00bc)
pmu timeout count register

Bit	Attr	Reset Value	Description
31:20	RO	0x0	reserved
19:0	RW	0x00000	timeout_count timeout wakeup counter value

PMU_CPU0APM_CON
Address: Operational Base + offset (0x00c0)
pmu cpu0 auto power down control register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	RW	0x0	cpu_l0_sft_wakeup cpu l0 software wakeup source. 1: wakeup ; 0: nothing ;
2	RW	0x0	reserved
1	RW	0x0	cpu_l0_int_wakeup_en cpu l0 interrupt wake enable. 0: disable ; 1: enable ;
0	RW	0x0	cpu_l0_wfi_pwrdn_en cpu_l0 wfi power down enable. 0: disable ; 1: enable ;

PMU_CPU1APM_CON
Address: Operational Base + offset (0x00c4)

pmu cpu1 auto power down control register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	RW	0x0	cpu_l1_sft_wakeup cpu l1 software wakeup source. 1: wakeup ; 0: nothing ;
2	RW	0x0	reserved
1	RW	0x0	cpu_l1_int_wakeup_en cpu l1 interrupt wake enable. 0: disable ; 1: enable ;
0	RW	0x0	cpu_l1_wfi_pwrdn_en cpu_l1 wfi power down enable. 0: disable ; 1: enable ;

PMU_CPU2APM_CON

Address: Operational Base + offset (0x00c8)

pmu cpu2 auto power down control register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	RW	0x0	cpu_l2_sft_wakeup cpu l2 software wakeup source. 1: wakeup ; 0: nothing ;
2	RW	0x0	reserved
1	RW	0x0	cpu_l2_int_wakeup_en cpu l2 interrupt wake enable. 0: disable ; 1: enable ;
0	RW	0x0	cpu_l2_wfi_pwrdn_en cpu_l2 wfi power down enable. 0: disable ; 1: enable ;

PMU_CPU3APM_CON

Address: Operational Base + offset (0x00cc)

pmu cpu3 auto power down control register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	RW	0x0	cpu_l3_sft_wakeup cpu l3 software wakeup source. 1: wakeup ; 0: nothing ;
2	RW	0x0	reserved

Bit	Attr	Reset Value	Description
1	RW	0x0	cpu_l3_int_wakeup_en cpu l3 interrupt wake enable. 0: disable ; 1: enable ;
0	RW	0x0	cpu_l3_wfi_pwrdn_en cpu_l3 wfi power down enable. 0: disable ; 1: enable ;

PMU_CPU0BPM_CON
Address: Operational Base + offset (0x00d0)
pmu cluster_b cpu0 auto power down control register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	RW	0x0	cpu_b0_sft_wakeup cpu b0 software wakeup source. 1: wakeup ; 0: nothing ;
2	RW	0x0	reserved
1	RW	0x0	cpu_b0_int_wakeup_en cpu b0 interrupt wake enable. 0: disable ; 1: enable ;
0	RW	0x0	cpu_b0_wfi_pwrdn_en cpu_b0 wfi power down enable. 0: disable ; 1: enable ;

PMU_CPU1BPM_CON
Address: Operational Base + offset (0x00d4)
pmu cluster_b cpu0 auto power down control register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	RW	0x0	cpu_b0_sft_wakeup cpu b0 software wakeup source. 1: wakeup ; 0: nothing ;
2	RW	0x0	reserved
1	RW	0x0	cpu_b0_int_wakeup_en cpu b0 interrupt wake enable. 0: disable ; 1: enable ;

Bit	Attr	Reset Value	Description
0	RW	0x0	cpu_b0_wfi_pwrdn_en cpu_b0 wfi power down enable. 0: disable ; 1: enable ;

PMU_NOC_AUTO_ENA
Address: Operational Base + offset (0x00d8)

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved
29	RW	0x0	sdioaudio_gating_disable 0: nothing 1: clock gating disable.
28	RW	0x0	sd_gating_disable 0: nothing 1: clock gating disable.
27	RW	0x0	gic_gating_disable 0: nothing ; 1: clock gating disable.
26	RW	0x0	gpu_gating_disable 0: nothing ; 1: clock gating disable.
25	RW	0x0	perilp_gating_disable 0: nothing ; 1: clock gating disable.
24	RW	0x0	perihp_gating_disable 0: nothing ; 1: clock gating disable.
23	RW	0x0	vcodec_gating_disable 0: nothing 1: clock gating disable.
22	RW	0x0	vdu_gating_disable 0: nothing ; 1: clock gating disable.
21	RW	0x0	rga_gating_disable 0: nothing ; 1: clock gating disable.
20	RW	0x0	iep_gating_disable 0: nothing ; 1: clock gating disable.
19	RW	0x0	vopb_gating_disable 0: nothing ; 1: clock gating disable.

Bit	Attr	Reset Value	Description
18	RW	0x0	vopl_gating_disable 0: nothing ; 1: clock gating disable.
17	RW	0x0	isp0_gating_disable 0: nothing ; 1: clock gating disable.
16	RW	0x0	isp1_gating_disable 0: nothing ; 1: clock gating disable.
15	RW	0x0	hdcp_gating_disable 0: nothing ; 1: clock gating disable.
14	RW	0x0	usb3_gating_disable 0: nothing 1: clock gating disable.
13	RW	0x0	perilpm0_gating_disable 0: nothing ; 1: clock gating disable.
12	RW	0x0	center_gating_disable 0: noting 1: clock gating disable.
11	RW	0x0	ccim0_gating_disable 0: nothing ; 1: clock gating disable.
10	RW	0x0	ccim1_gating_disable 0: nothing ; 1: clock gating disable.
9	RW	0x0	vio_gating_disable 0: nothing ; 1: clock gating disable.
8	RW	0x0	msch0_gating_disable 0: nothing ; 1: clock gating disable.
7	RW	0x0	msch1_gating_disable 0: nothing ; 1: clock gating disable.
6	RW	0x0	alive_gating_disable 0: nothing ; 1: clock gating disable.
5	RW	0x0	pmu_gating_disable 0: nothing ; 1: clock gating disable.
4	RW	0x0	edp_gating_disable 0: nothing ; 1: clock gating disable.

Bit	Attr	Reset Value	Description
3	RW	0x0	gmac_gating_disable 0: nothing ; 1: gmac clock gating disable.
2	RW	0x0	emmc_gating_disable 0: nothing ; 1: clock gating disable.
1	RW	0x0	center1_gating_disable 0: nothing 1: clock gating disable.
0	RW	0x0	pmum0_gating_disable 0: noting ; 1: clock gating disable.

PMU_PWRDN_CON1
Address: Operational Base + offset (0x00dc)
pmu power down configure register1

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2	RW	0x0	vd_center_pwrdwn vd_center power down enable 0: disable 1: enable
1	RW	0x0	vd_scu_b_pwrdwn vd_scu_b power down enable 0: disable 1: enable
0	RW	0x0	vd_scu_l_enable vd_scu_l power down enable 0: disable 1: enable

PMU_SYS_REG0
Address: Operational Base + offset (0x00f0)
pmu system register 0

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_sys_reg0 system register 0

PMU_SYS_REG1
Address: Operational Base + offset (0x00f4)
pmu system register 1

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_sys_reg1 system register 1

PMU_SYS_REG2
Address: Operational Base + offset (0x00f8)
pmu system register 2

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_sys_reg2 system register 2

PMU_SYS_REG3
Address: Operational Base + offset (0x00fc)
pmu system register 3

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	pmu_sys_reg3 system register 3

11.5 Timing Diagram

11.5.1 Each domain power switch timing

The following figure is the each domain power down and power up timing.

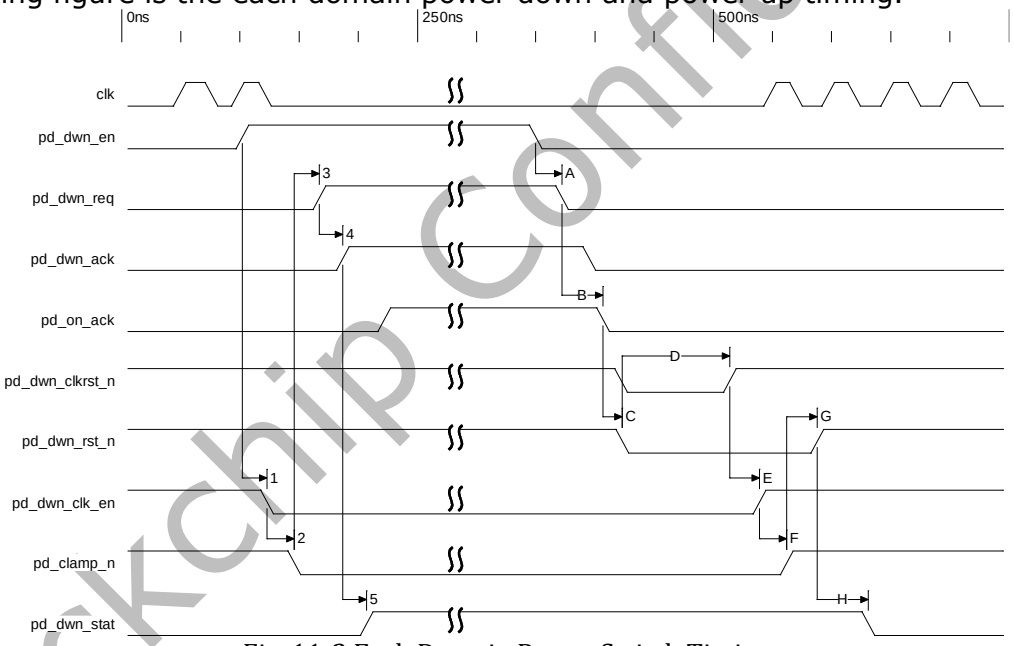


Fig. 11-3 Each Domain Power Switch Timing

11.5.2 External wakeup PAD timing

The PMU supports a lot of external wakeup sources, such as SD/MMDC, USBDEV, SIM detect wakeup, GPIO0 wakeup source and so on. All these external wakeup sources must meet the timing requirement (at least 200us) when the wakeup event is asserted. The following figure gives the timing information.

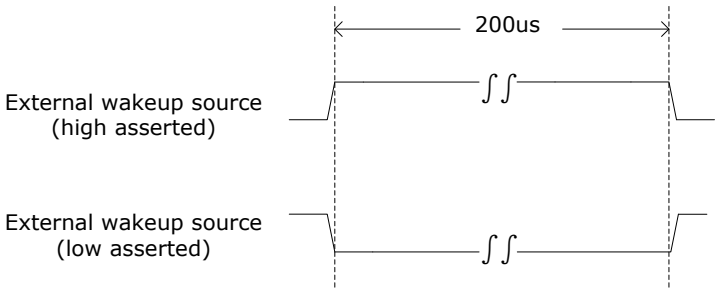


Fig. 11-4 External Wakeup Source PAD Timing

Chapter 12 Memory-Management-Unit (MMU)

12.1 Overview

An MMU controls address translation, access permissions, memory attribute determination, and checking at a memory system level.

12.2 Block Diagram

The MMU divides memory into 4KB pages, where each page can be individually configured. The MMU uses a 2-level page table structure:
1. The first level, the Page Directory consists of 1024 Directory Table Entries (DTEs), each pointing to a Page Table.
2. The second level, the Page Table consists of 1024 Page Table Entries (PTEs), each pointing to a page in memory.
Fig. 14-1 shows the structure of the two-level page table.

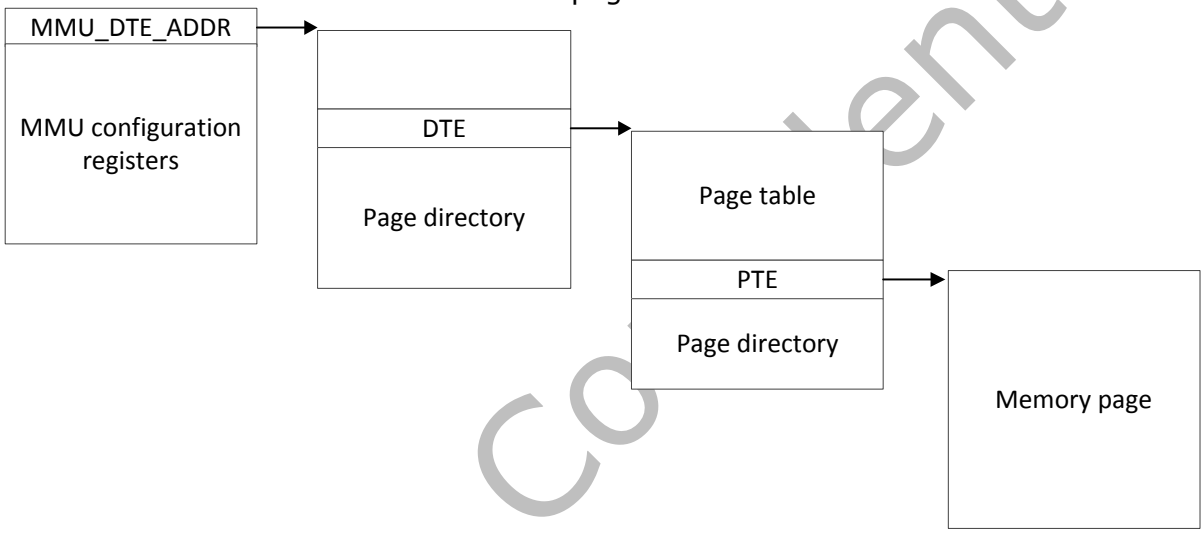


Fig. 11-5 MMU Structure

Fig. 14-2 shows the arrangement of the MMU address bits.

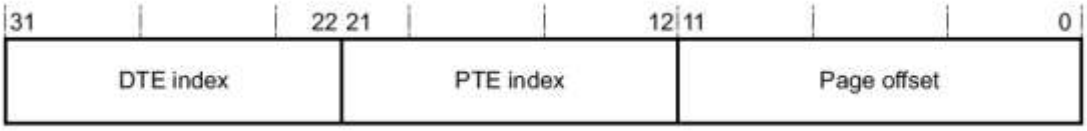


Fig. 11-6 MMU Address Bits

The MMU uses the following algorithm to translate an address:
1. Find the DTE at address given by:
MMU_DTE_ADDR + (4 * DTE index)
2. Find the PTE at address given by:
Page table address from DTE + (4 * PTE index)
3. Calculate effective address as follows:
Page address from PTE + Page offset.

The page directory is a 4KB data structure that contains 1024 32-bit DTEs. The page directory must align at a 4KB boundary in memory.
Each DTE contains the address of a page table and a page table present bit. The system:

- initializes the entire page directory before use
- clear the page table present bit for any DTE that does not point to a valid page table.

The following table shows the page bit assignments.

Table 11-2 Page directory entry detail

Bits	Name	Function

Bits	Name	Function
[31:12]	Page table address	This field stores bits [31:12] of the address for a page table
[11:1]	Reserved	Reserved, write as zero
[0]	Page table present	This bit indicates when the page table address points to a valid page table. 0 = page table not valid 1= page table valid.

The page table is a 4KB data structure containing 1024 32-bit PTEs. The page table must be aligned at a 4KB boundary in memory.
Each PTE contains the address of a page of memory, a Page Table present bit, and Read/Write Permission bits. The entire Page Table must be initialized before use, and any PTE not pointing to a valid page must clear the Page Present bit.
The following table shows the page table entry bit assignments.

Table 11-3 Page directory entry detail

Bits	Name	Function
[31:12]	Page table address	This field stores bits [31:12] of the address for a page table
[11:9]	Reserved	Reserved, write as zero
[8]	Read allocate	If set, allocate cache space on read misses. Must not be set if the Read cacheable bit is not set. Only used for reads, if the Override cache attributes bit is set.
[7]	Read cacheable	If set, enable caching or prefetching of data. Only used for reads, if the Override cache attributes bit is set.
[6]	Write bufferable	If set, enable write to be delayed on their way to memory. Only used for writes, if the Override cache attributes bit is set.
[5]	Write allocate	If set, allocate cache space on write misses. Must not be set if the Write cacheable bit is not set. Only used for writes, if the Override cache attributes is set.
[4]	Write cacheable	If set, enable different writes to be merged together. Only used for writes, if the Override cache attributes bit is set.
[3]	Override cache attributes	If set, the cacheability attributes specified in bits [8:4] are used to control the cache attribytes used on the memory bus. If cleared, the default cacheability attributes from the specific processors are used on the system bus.
[2]	Write permission	Enable write accesses to the page, if present.
[1]	Read permission	Enable read accesses from the page, if present.
[0]	Page present	This bit indicates when the page table field points to a valid page. 0 = page not valid 1 = page valid.

Block Descriptions:

- APB Interface

The APB Interface implements the APB slave operation. Its data bus width is 32 bits.

- Register Block

A register block that read coherence for the current count register.

- Interrupt & system reset control

An interrupt/system reset generation block is comprised of a decrementing counter and control logic.

12.3 Register Description

This section describes the control/status registers of the design.

12.3.1 Registers Summary

Name	Offset	Size	Reset Value	Description
MMU_DTE_ADDR	0x0000	W	0x00000000	MMU current page table address
MMU_STATUS	0x0004	W	0x00000018	MMU status register
MMU_CMD	0x0008	W	0x00000000	MMU command register
MMU_PAGE_FAULT_ADDR	0x000c	W	0x00000000	MMU logic address of last page fault register
MMU_ZAP_ONE_LINE	0x0010	W	0x00000000	MMU zap cache line register
MMU_INT_RAWSTAT	0x0014	W	0x00000000	MMU raw interrupt status register
MMU_INT_CLEAR	0x0018	W	0x00000000	MMU interrupt clear register
MMU_INT_MASK	0x001c	W	0x00000000	MMU interrupt mask register
MMU_INT_STATUS	0x0020	W	0x00000000	MMU interrupt status register
MMU_AUTO_GATING	0x0024	W	0x00000000	clock atuo gating register

12.3.2 Detail Register Description

MMU_DTE_ADDR

Address: Operational Base + offset (0x0000)

MMU current page table address

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mmu_dte_addr page table address

MMU_STATUS

Address: Operational Base + offset (0x0004)

MMU status register

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10:6	RO	0x00	mmu_page_fault_bus_id Index of master responsible for the last page fault
5	RO	0x0	mmu_page_fault_is_write The direction of access for last page fault: 0: read 1:write
4	RO	0x1	mmu_replay_buffer_empty 1：The MMU replay buffer is empty.

Bit	Attr	Reset Value	Description
3	RO	0x1	mmu_idle the MMu is idle when accesses are being translated and there are no unfinished translated access. The MMU_IDLE signal only reports idle when the MMU processor is idle and accesses are active on the external bus. Note: the MMU can be idle in page fault mode. 1: MMU is idle
2	RO	0x0	mmu_stall_active MMU stall mode currently enabled. The mode is enabled by command. 1: MMU is in stall active status
1	RO	0x0	mmu_page_fault_active MMU page fault mode currently enabled.The mode is enabled by command 1: page fault is active
0	RO	0x0	mmu_paging_enabled 0: paging is disabled 1: Paging is enabled

MMU_CMD
Address: Operational Base + offset (0x0008)
MMU command register

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2:0	RW	0x0	mmu_cmd 0: MMU_ENABLE_PAGING. enable paging. 1: MMU_DISABLE_PAGING. disable paging. 2: MMU_ENABLE_STALL. turn on stall mode. 3: MMU_DISABLE_STALL. turn off stall mode. 4: MMU_ZAP_CACHE. zap the entire page table cache. 5: MMU_PAGE_FAULT_DONE. leave page fault mode. 6: MMU_FORCE_RESET. reset the mmu. The MMU_ENABLE_STALL command can always be issued. Other commands are ignored unless the MMU is idle or stalled.

MMU_PAGE_FAULT_ADDR
Address: Operational Base + offset (0x000c)
MMU logic address of last page fault register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	mmu_page_fault_addr address of last page fault

MMU_ZAP_ONE_LINE

Address: Operational Base + offset (0x0010)
MMU zap cache line register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	mmu_zap_one_line address to be invalidated from the page table cache.

MMU_INT_RAWSTAT
Address: Operational Base + offset (0x0014)
MMU raw interrupt status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RO	0x0	read_bus_error read bus error
0	RO	0x0	page_fault page fault

MMU_INT_CLEAR
Address: Operational Base + offset (0x0018)
MMU interrupt clear register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	read_bus_error_clear read bus error interrupt clear. write 1 to this register can clear read bus error interrupt.
0	RW	0x0	page_fault_clear page fault interrupt clear, write 1 to this register can clear page fault interrupt.

MMU_INT_MASK
Address: Operational Base + offset (0x001c)
MMU interrupt mask register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	read_bus_error_int_en read bus error interrupt enable
0	RW	0x0	page_fault_int_en page fault interrupt enable

MMU_INT_STATUS
Address: Operational Base + offset (0x0020)
MMU interrupt status register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1	RW	0x0	read_bus_error read bus error interrupt
0	RO	0x0	page_fault page fault interrupt

MMU_AUTO_GATING
Address: Operational Base + offset (0x0024)
clock atuo gating register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	mmu_atuo_gating mmu clock auto gating when it is 1, the mmu will auto gating itself

12.4 MMU Base Address

The table below shows the MMU base address in different modules.

ISP0_MMU0_BASE	ISP0_BASEADDR + 0x4000
ISP0_MMU1_BASE	ISP0_BASEADDR + 0x5000
ISP1_MMU0_BASE	ISP1_BASEADDR + 0x4000
ISP1_MMU1_BASE	ISP1_BASEADDR + 0x5000
VOPL_MMU_BASE	VOPL_BASEADDR + 0x300
VOPB_MMU_BASE	VOPB_BASEADDR + 0x300
IEP_MMU_BASE	IEP_BASE + 0x800
HDCP_MMU_BASE	0xff930000

Chapter 13 Timer

13.1 Overview

Timer is a programmable timer peripheral. This component is an APB slave device. In RK3399 there are 12 Timers(timer0~timer11), 12 Secure Timers(stimer0~stimer11) in ALIVE and 2 Timers(pmutimer0~pmutimer1) in PMU.
All timers count up from a lower programmed value to a higher programmed value and generate an interrupt when the counter reaches the programmed value.
Timer supports the following features:

- Timer0~Timer11 and pmutimer0~pmutimer1 are used for no-secure, stimer0~stimer11 are used for secure.
- Two operation modes: free-running and user-defined count.
- Maskable for each individual interrupt.

13.2 Block Diagram

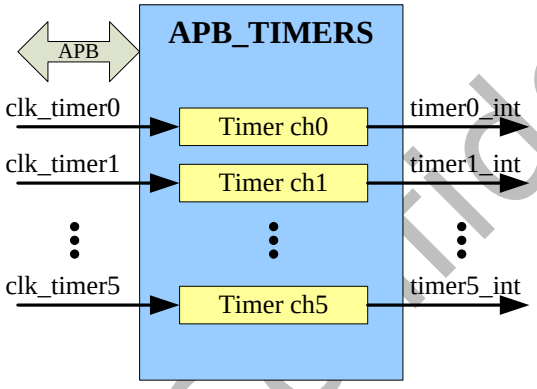


Fig. 11-7 Timer Block Diagram

The above figure shows the architecture of the APB timers (include six programmable timer channels) that in the bus subsystem. The Stimers that in the bus subsystem only include two programmable timer channels.

13.3 Function Description

13.3.1 Timer clock

The timer clock is 24MHz OSC.

13.3.2 Programming sequence

1. Initialize the timer by the TIMERn_CONTROLREG register:

- Disable the timer by writing a "0" to the timer enable bit (bit 0). Accordingly, the timer_en output signal is de-asserted.
- Program the timer mode—user-defined or free-running—by writing a "0" or "1" respectively, to the timer mode bit (bit 1).
- Set the interrupt mask as either masked or not masked by writing a "0" or "1" respectively, to the timer interrupt mask bit (bit 2).

2. Load the timer count value into the TIMERn_LOAD_COUNT0 ~TIMERn_ LOAD_COUNT03 register.

3. Enable the timer by writing a "1" to bit 0 of TIMERn_CONTROLREG.

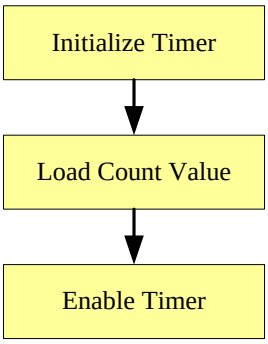


Fig. 11-8 Timer Usage Flow

13.3.3 Loading a timer count value

The initial value for each timer is TIMERn_LOAD_COUNT3 and TIMERn_ LOAD_COUNT2. The count register will count up to the value loaded in the register TIMERn_LOAD_COUNT1 and TIMERn_ LOAD_COUNT0. Two events can cause a timer to load zero:

- Timer is enabled after reset or disabled.
- Timer counts up to the value stored in TIMERn_LOAD_COUNT1 and TIMERn_ LOAD_COUNT0, when timer is configured into free-running mode.

13.3.4 Timer mode selection

- User-defined count mode – Timer loads TIMERn_LOAD_COUNT3 and TIMERn_ LOAD_COUNT2 as initial value. When the timer counts up to the value in TIMERn_LOAD_COUNT1 and TIMERn_LOAD_COUNT0, it will not automatically reload the count register. User need to disable timer firstly and follow the programming sequence to make timer work again.
- Free-running mode – Timer loads the TIMERn_LOAD_COUNT3 and TIMERn_LOAD_COUNT2 register as initial value. Timer will automatically reload the count register, when timer counts up to the value in TIMERn_LOAD_COUNT1 and TIMERn_LOAD_COUNT0.

13.4 Register Description

This section describes the control/status registers of the design. Software should read and write these registers using 32-bits accesses.

13.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
TIMER_n_LOAD_COUNT0	0x0000	W	0x00000000	Timer n higher Load Count Register
TIMER_n_LOAD_COUNT1	0x0004	W	0x00000000	Timer n higher Load Count Register
TIMER_n_CURRENT_VALUE0	0x0008	W	0x00000000	Timer n Current Value Register
TIMER_n_CURRENT_VALUE1	0x000c	W	0x00000000	Timer n Current Value Register
TIMER_n_LOAD_COUNT2	0x0010	W	0x00000000	Timer n lower Load Count Register
TIMER_n_LOAD_COUNT3	0x0014	W	0x00000000	Timer n lower Load Count Register
TIMER_n_INTSTATUS	0x0018	W	0x00000000	Timer Interrupt Stauts Register
TIMER_n_CONTROLREG	0x001c	W	0x00000000	Timer n Control Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

13.4.2 Detail Register Description

TIMER_n_LOAD_COUNT0
Address: Operational Base + offset (0x00)
Timer n High Load Count Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	load_count_low bits Low 32 bits value to be loaded into Timer n.

TIMER_n_LOAD_COUNT1
Address: Operational Base + offset (0x04)
Timer n High Load Count Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	load_count_high bits High 32 bits value to be loaded into Timer n.

TIMER_n_CURRENT_VALUE0
Address: Operational Base + offset (0x08)
Timer n Current Value Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	current_cnt_lowbits Low 32 bits of current value of timer n.

TIMER_n_CURRENT_VALUE1
Address: Operational Base + offset (0x0c)
Timer n Current Value Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	current_cnt_highbits High 32 bits of current value of timer n.

TIMER_n_LOAD_COUNT2
Address: Operational Base + offset (0x10)
Timer n Low Load Count Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	load_count_low bits Low 32 bits value to be loaded into Timer n.

TIMER_n_LOAD_COUNT3
Address: Operational Base + offset (0x14)
Timer n Low Load Count Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	load_count_high bits High 32 bits value to be loaded into Timer n.

TIMER_n_INTSTATUS
Address: Operational Base + offset (0x18)
Timer Interrupt Stauts Register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	W1C	0x0	int_pd This register contains the interrupt status for timer n. Write 1 to this register will clear the interrupt.

TIMER_n_CONTROLREG
Address: Operational Base + offset (0x1c)
Timer n Control Register

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2	RW	0x0	int_en Timer interrupt mask 0: mask 1: not mask
1	RW	0x0	timer_mode Timer mode. 0: free-running mode 1: user-defined count mode
0	RW	0x0	timer_en Timer enable. 0: disable 1: enable

13.5 Application Notes

In the chip, the timer_clk is from 24MHz OSC, asynchronous to the pclk. When user disables the timer enables bit, the timer en output signal is de-asserted, and timer_clk will stop. When user enables the timer, the timer_en signal is asserted and timer_clk will start running.
The application is only allowed to re-config registers when timer_en is low.

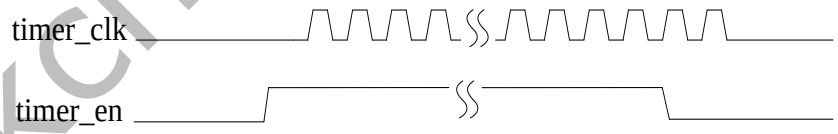


Fig. 11-9 Timing between timer_en and timer_clk

Please refer to function description section for the timer usage flow.

Chapter 14 GIC500

14.1 Overview

The GIC-500 in RK3399 provides registers for managing interrupt sources, interrupt behavior, and interrupt routing to one or more cores.
The configuration of GIC500 is shown below:

Configuration item	Value
num_clusters	2
gic_num_rid_bits	4
num_spis	256
disable_security	false
gic_num_wid_bits	4
lpi_support	true
cpus_per_clsuter_0	4
are_option	false
lpi_size	256
cpus_per_cluster_1	2
did_size	16

Table 15-1 GIC500 configuration

The GIC in RK3399 supports following feature:

- Support 2 clusters
- Support cluster 0 with 4 cpus
- Support cluster 1 with 2 cpus
- The following interrupt types:
  - Locality-specific Peripheral Interrupts (LPIs). These interrupts are generated by a peripheral writing to a memory-mapped register in the GIC-500. See Configurable options for the GIC-500 RTL on page 1-9.
  - 256 Shared Peripheral Interrupts (SPIs).
  - 16 Private Peripheral Interrupts (PPIs), that are independent for each core and can be programmed to support either edge-triggered or level-sensitive interrupts.
  - 16 SGIs, that are generated either by using software to write to GICD_SGIR or through the GIC CPU interface of a core.
- Interrupt Translation Service (ITS). This provides device isolation and ID translation for message-based interrupts, which allows virtual machines to program devices directly.
- Memory-mapped access to all registers.
- Interrupt masking and prioritization.
- Programmable interrupt routing that is based on affinity.
- Three different interrupt groups, which allow interrupts to target different Exception levels:
  - Group 0.
  - Non-secure Group 1.
  - Secure Group 1.
- A global Disable Security (DS) bit. This allows support for systems with and without security.
- 32 priority values, five bits for each interrupt.

14.2 Block Diagram

The GIC500 in the RK3399 is connected with CPU clusters through AXI Stream bus, as shown below:

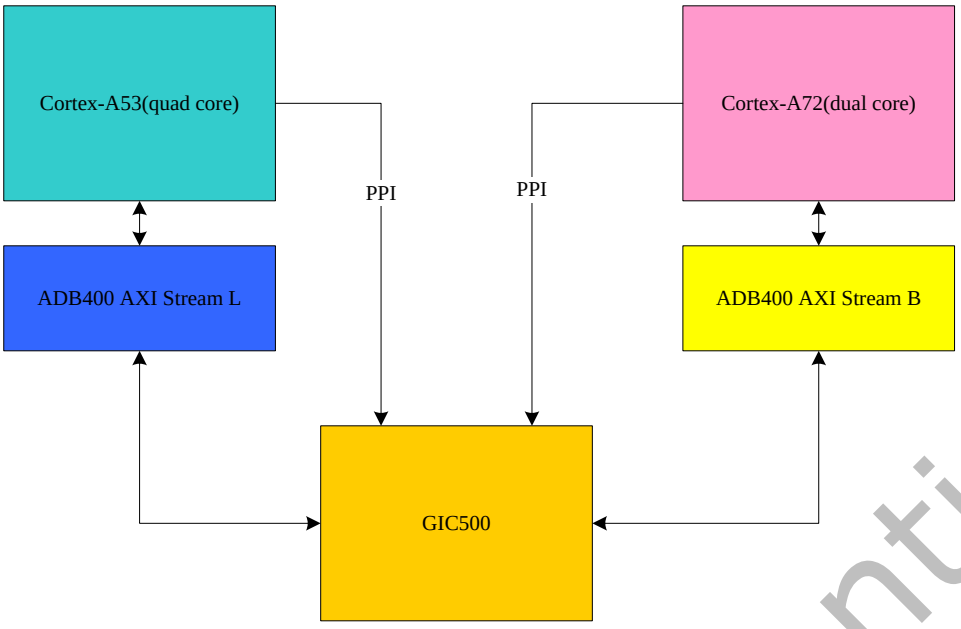


Fig. 14-1 Block Diagram

Chapter 15 DMA Controller (DMAC)

15.1 Overview

This device supports 2 Direct Memory Access (DMA) Controllers, DMAC0 and DMAC1. Both of these two DMAC support transfers between memory and memory, peripheral and memory. DMAC is under Non-secure state after reset, and the secure state can be changed by configuring SGRF module.

DMAC0 supports the following features:

- Supports Trustzone technology
- Supports 12 peripheral request
- Up to 64bits data size
- 6 channel at the same time
- Up to burst 16
- 12 interrupts output and 1 abort output
- Supports 32 MFIFO depth

Following table shows the DMAC0 request mapping scheme.

Table 15-1 DMAC0 Request Mapping Table

Req number	Source	Polarity
0	I2S0 tx	High level
1	I2S0 rx	High level
2	I2S1 tx	High level
3	I2S1 rx	High level
4	I2S2 tx	High level
5	I2S2 rx	High level
6	PWM	High level
7	SPDIF tx	High level
8	SPI5 tx	High level
9	SPI5 rx	High level
10	Reserved	
11	Reserved	

DMAC1 supports the following features:

- Supports Trustzone technology
- Supports 20 peripheral request
- Up to 64bits data size
- 8 channel at the same time
- Up to burst 16
- 16 interrupts output and 1 abort output
- Supports 128 MFIFO depth

Following table shows the DMAC1 request mapping scheme.

Table 15-2 DMAC1 Request Mapping Table

Req number	Source	Polarity
0	UART0 tx	High level
1	UART0 rx	High level
2	UART1 tx	High level
3	UART1 rx	High level
4	UART2 tx	High level
5	UART2 rx	High level
6	UART3 tx	High level
7	UART3 rx	High level
8	UART4 tx	High level
9	UART4 rx	High level
10	SPI0 tx	High level
11	SPI0 rx	High level
12	SPI1 tx	High level

Req number	Source	Polarity
13	SPI1 rx	High level
14	SPI2 tx	High level
15	SPI2 rx	High level
16	SPI3 tx	High level
17	SPI3 rx	High level
18	SPI4 tx	High level
19	SPI4 rx	High level

DMAC support incrementing-address burst and fixed-address burst. But in the case of access SPI and UART at byte or halfword size, DMAC only support fixed-address burst and the address must be aligned to word.

15.2 Block Diagram

Following figure shows the block diagram of DMAC.

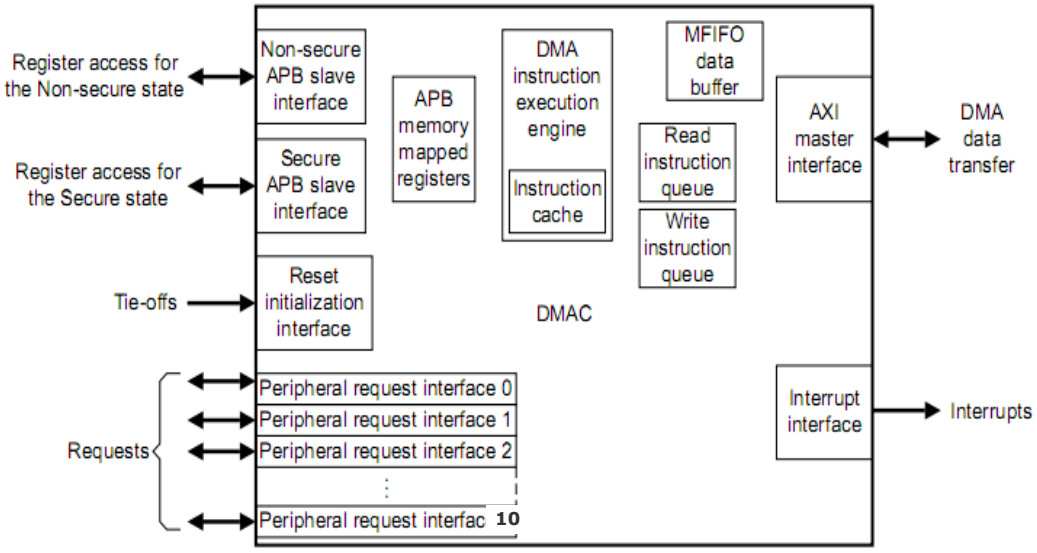


Fig. 15-1 Block diagram of DMAC

As the DMAC supports Trustzone technology, so dual APB interfaces enable the operation of the DMAC to be partitioned into the secure state and Non-secure state. You can use the APB interfaces to access status registers and also directly execute instructions in the DMAC. The default interface after reset is Non-secure apb interface.

15.3 Function Description

15.3.1 Introduction

The DMAC contains an instruction processing block that enables it to process program code that controls a DMA transfer. The program code is stored in a region of system memory that the DMAC accesses using its AXI interface. The DMAC stores instructions temporarily in a cache.

DMAC0 supports 6 channels and DMAC1 supports 8 channels, each channel capable of supporting a single concurrent thread of DMA operation. In addition, a single DMA manager thread exists, and you can use it to initialize the DMA channel threads. The DMAC executes up to one instruction for each AXI clock cycle. To ensure that it regularly executes each active thread, it alternates by processing the DMA manager thread and then a DMA channel thread. It uses a round-robin process when selecting the next active DMA channel thread to execute. The DMAC uses variable-length instructions that consist of one to six bytes. It provides a separate Program Counter (PC) register for each DMA channel. When a thread requests an instruction from an address, the cache performs a look-up. If a cache hit occurs, then the cache immediately provides the data. Otherwise, the thread is stalled while the DMAC uses the AXI interface to perform a cache line fill. If an instruction is greater than 4 bytes, or spans the end of a cache line, the DMAC performs multiple cache accesses to fetch the instruction.

When a cache line fill is in progress, the DMAC enables other threads to access the cache, but if another cache miss occurs, this stalls the pipeline until the first line fill is complete.
When a DMA channel thread executes a load or store instruction, the DMAC adds the instruction to the relevant read or write queue. The DMAC uses these queues as an instruction storage buffer prior to it issuing the instructions on the AXI bus. The DMAC also contains a Multi First-In-First-Out (MFIFO) data buffer that it uses to store data that it reads, or writes, during a DMA transfer.

15.3.2 Operating states

Following figure shows the operating states for the DMA manager thread and DMA channel threads.

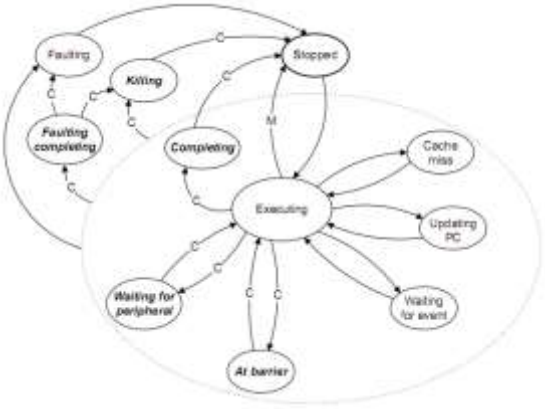


Fig. 15-2 DMAC operation states

Notes:arcs with no letter designator indicate state transitions for the DMA manager and DMA channel threads, otherwise use is restricted as follows:
C DMA channel threads only.
M DMA manager thread only.

After the DMAC exits from reset, it sets all DMA channel threads to the stopped state, and the status of boot_from_pc(tie-off interface of dmac) controls the DMA manager thread state:
boot_from_pc is LOW :DMA manager thread moves to the Stopped state.
boot_from_pc is HIGH :DMA manager thread moves to the Executing state.

15.4 Register Description

15.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
DMAC_DSR	0x0000	W	0x00000000	DMA Manager Status Register
DMAC_DPC	0x0004	W	0x00000000	DMA Program Counter Register
DMAC_INTEN	0x0020	W	0x00000000	Interrupt Enable Register
DMAC_EVENT_RIS	0x0024	W	0x00000000	Event-Interrupt Raw Status Register
DMAC_INTMIS	0x0028	W	0x00000000	Interrupt Status Register
DMAC_INTCLR	0x002c	W	0x00000000	Interrupt Clear Register
DMAC_FSRD	0x0030	W	0x00000000	Fault Status DMA Manager Register
DMAC_FSRC	0x0034	W	0x00000000	Fault Status DMA Channel Register
DMAC_FTRD	0x0038	W	0x00000000	Fault Type DMA Manager Register
DMAC_FTR0	0x0040	W	0x00000000	Fault Type DMA Channel Register
DMAC_FTR1	0x0044	W	0x00000000	Fault Type DMA Channel Register
DMAC_FTR2	0x0048	W	0x00000000	Fault Type DMA Channel Register
DMAC_FTR3	0x004c	W	0x00000000	Fault Type DMA Channel Register

Name	Offset	Size	Reset Value	Description
DMAC_FTR4	0x0050	W	0x00000000	Fault Type DMA Channel Register
DMAC_FTR5	0x0054	W	0x00000000	Fault Type DMA Channel Register
DMAC_FTR6	0x0058	W	0x00000000	Fault Type DMA Channel Register
DMAC_FTR7	0x005c	W	0x00000000	Fault Type DMA Channel Register
DMAC_CSR0	0x0100	W	0x00000000	Channel Status Registers
DMAC_CPC0	0x0104	W	0x00000000	Channel Program Counter Registers
DMAC_CSR1	0x0108	W	0x00000000	Channel Status Registers
DMAC_CPC1	0x010c	W	0x00000000	Channel Program Counter Registers
DMAC_CSR2	0x0110	W	0x00000000	Channel Status Registers
DMAC_CPC2	0x0114	W	0x00000000	Channel Program Counter Registers
DMAC_CSR3	0x0118	W	0x00000000	Channel Status Registers
DMAC_CPC3	0x011c	W	0x00000000	Channel Program Counter Registers
DMAC_CSR4	0x0120	W	0x00000000	Channel Status Registers
DMAC_CPC4	0x0124	W	0x00000000	Channel Program Counter Registers
DMAC_CSR5	0x0128	W	0x00000000	Channel Status Registers
DMAC_CPC5	0x012c	W	0x00000000	Channel Program Counter Registers
DMAC_CSR6	0x0130	W	0x00000000	Channel Status Registers
DMAC_CPC6	0x0134	W	0x00000000	Channel Program Counter Registers
DMAC_CSR7	0x0138	W	0x00000000	Channel Status Registers
DMAC_CPC7	0x013c	W	0x00000000	Channel Program Counter Registers
DMAC_SAR0	0x0400	W	0x00000000	Source Address Registers
DMAC_DAR0	0x0404	W	0x00000000	Destination Address Registers
DMAC_CCR0	0x0408	W	0x00000000	Channel Control Registers
DMAC_LC0_0	0x040c	W	0x00000000	Loop Counter 0 Registers
DMAC_LC1_0	0x0410	W	0x00000000	Loop Counter 1 Registers
DMAC_SAR1	0x0420	W	0x00000000	Source Address Registers
DMAC_DAR1	0x0424	W	0x00000000	Destination Address Registers
DMAC_CCR1	0x0428	W	0x00000000	Channel Control Registers
DMAC_LC0_1	0x042c	W	0x00000000	Loop Counter 0 Registers
DMAC_LC1_1	0x0430	W	0x00000000	Loop Counter 1 Registers
DMAC_SAR2	0x0440	W	0x00000000	Source Address Registers
DMAC_DAR2	0x0444	W	0x00000000	Destination Address Registers
DMAC_CCR2	0x0448	W	0x00000000	Channel Control Registers
DMAC_LC0_2	0x044c	W	0x00000000	Loop Counter 0 Registers
DMAC_LC1_2	0x0450	W	0x00000000	Loop Counter 1 Registers
DMAC_SAR3	0x0460	W	0x00000000	Source Address Registers

Name	Offset	Size	Reset Value	Description
DMAC_DAR3	0x0464	W	0x00000000	Destination Address Registers
DMAC_CCR3	0x0468	W	0x00000000	Channel Control Registers
DMAC_LC0_3	0x046c	W	0x00000000	Loop Counter 0 Registers
DMAC_LC1_3	0x0470	W	0x00000000	Loop Counter 1 Registers
DMAC_SAR4	0x0480	W	0x00000000	Source Address Registers
DMAC_DAR4	0x0484	W	0x00000000	Destination Address Registers
DMAC_CCR4	0x0488	W	0x00000000	Channel Control Registers
DMAC_LC0_4	0x048c	W	0x00000000	Loop Counter 0 Registers
DMAC_LC1_4	0x0490	W	0x00000000	Loop Counter 1 Registers
DMAC_SAR5	0x04a0	W	0x00000000	Source Address Registers
DMAC_DAR5	0x04a4	W	0x00000000	Destination Address Registers
DMAC_CCR5	0x04a8	W	0x00000000	Channel Control Registers
DMAC_LC0_5	0x04ac	W	0x00000000	Loop Counter 0 Registers
DMAC_LC1_5	0x04b0	W	0x00000000	Loop Counter 1 Registers
DMAC_SAR6	0x04c0	W	0x00000000	Source Address Registers
DMAC_DAR6	0x04c4	W	0x00000000	Destination Address Registers
DMAC_CCR6	0x04c8	W	0x00000000	Channel Control Registers
DMAC_LC0_6	0x04cc	W	0x00000000	Loop Counter 0 Registers
DMAC_LC1_6	0x04d0	W	0x00000000	Loop Counter 1 Registers
DMAC_SAR7	0x04e0	W	0x00000000	Source Address Registers
DMAC_DAR7	0x04e4	W	0x00000000	Destination Address Registers
DMAC_CCR7	0x04e8	W	0x00000000	Channel Control Registers
DMAC_LC0_7	0x04ec	W	0x00000000	Loop Counter 0 Registers
DMAC_LC1_7	0x04f0	W	0x00000000	Loop Counter 1 Registers
DMAC_DBGSTATUS	0x0d00	W	0x00000000	Debug Status Register
DMAC_DBGCMD	0x0d04	W	0x00000000	Debug Command Register
DMAC_DBGINST0	0x0d08	W	0x00000000	Debug Instruction-0 Register
DMAC_DBGINST1	0x0d0c	W	0x00000000	Debug Instruction-1 Register
DMAC_CR0	0x0e00	W	0x00047051	Configuration Register 0
DMAC_CR1	0x0e04	W	0x00000057	Configuration Register 1
DMAC_CR2	0x0e08	W	0x00000000	Configuration Register 2
DMAC_CR3	0x0e0c	W	0x00000000	Configuration Register 3
DMAC_CR4	0x0e10	W	0x00000006	Configuration Register 4
DMAC_CRDn	0x0e14	W	0x02094733	DMA Configuration Register
DMAC_WD	0x0e80	W	0x00000000	DMA Watchdog Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access.*
For DMAC0 channel register, only the channel 0~5 is valid.

15.4.2 Detail Register Description

DMAC_DSR
Address: Operational Base + offset (0x0000)
DMA Manager Status Register

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved

Bit	Attr	Reset Value	Description
9	RO	0x0	Provides the security status of the DMA manager thread: 0 = DMA manager operates in the Secure state 1 = DMA manager operates in the Non-secure state.
8:4	RO	0x00	When the DMA manager thread executes a DMAWFE instruction, it waits for the following event to occur: b00000 = event[0] b00001 = event[1] b00010 = event[2] … b11111 = event[31].
3:0	RO	0x0	The operating state of the DMA manager: b0000 = Stopped b0001 = Executing b0010 = Cache miss b0011 = Updating PC b0100 = Waiting for event b0101-b1110 = reserved b1111 = Faulting.

DMAC_DPC
Address: Operational Base + offset (0x0004)
DMA Program Counter Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	Program counter for the DMA manager thread

DMAC_INTEN
Address: Operational Base + offset (0x0020)
Interrupt Enable Register

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	Program the appropriate bit to control how the DMAC responds when it executes DMASEV: Bit [N] = 0 If the DMAC executes DMASEV for the event-interrupt resource N then the DMAC signals event N to all of the threads. Set bit [N] to 0 if your system design does not use irq[N] to signal an interrupt request. Bit [N] = 1 If the DMAC executes DMASEV for the event-interrupt resource N then the DMAC sets irq[N] HIGH. Set bit [N] to 1 if your system designer requires irq[N] to signal an interruptrequest.

DMAC_EVENT_RIS
Address: Operational Base + offset (0x0024)
Event-Interrupt Raw Status Register

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	Returns the status of the event-interrupt resources: Bit [N] = 0 Event N is inactive or irq[N] is LOW. Bit [N] = 1 Event N is active or irq[N] is HIGH.

DMAC_INTMIS
Address: Operational Base + offset (0x0028)
Interrupt Status Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	Provides the status of the interrupts that are active in the DMAC: Bit [N] = 0 Interrupt N is inactive and therefore irq[N] is LOW. Bit [N] = 1 Interrupt N is active and therefore irq[N] is HIGH

DMAC_INTCLR
Address: Operational Base + offset (0x002c)
Interrupt Clear Register

Bit	Attr	Reset Value	Description
31:0	WO	0x00000000	Controls the clearing of the irq outputs: Bit [N] = 0 The status of irq[N] does not change. Bit [N] = 1 The DMAC sets irq[N] LOW if the INTEN Register programs the DMAC to signal an interrupt. Otherwise, the status of irq[N] does not change.

DMAC_FSRD
Address: Operational Base + offset (0x0030)
Fault Status DMA Manager Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	Provides the fault status of the DMA manager. Read as: 0 = the DMA manager thread is not in the Faulting state 1 = the DMA manager thread is in the Faulting state.

DMAC_FSRC
Address: Operational Base + offset (0x0034)
Fault Status DMA Channel Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	Each bit provides the fault status of the corresponding channel. Read as: Bit [N] = 0 No fault is present on DMA channel N. Bit [N] = 1 DMA channel N is in the Faulting or Faulting completing state.

DMAC_FTRD
Address: Operational Base + offset (0x0038)
Fault Type DMA Manager Register

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved

Bit	Attr	Reset Value	Description
30	RO	0x0	If the DMA manager aborts, this bit indicates if the erroneous instruction was read from the system memory or from the debug interface: 0 = instruction that generated an abort was read from system memory 1 = instruction that generated an abort was read from the debug interface.
29:17	RO	0x0	reserved
16	RO	0x0	Indicates the AXI response that the DMAC receives on the RRESP bus, after the DMA manager performs an instruction fetch: 0 = OKAY response 1 = EXOKAY, SLVERR, or DECERR response
15:6	RO	0x0	reserved
5	RO	0x0	Indicates if the DMA manager was attempting to execute DMAWFE or DMASEV with inappropriate security permissions: 0 = DMA manager has appropriate security to execute DMAWFE or DMASEV 1 = a DMA manager thread in the Non-secure state attempted to execute either: DMAWFE to wait for a secure event DMASEV to create a secure event or secure interrupt
4	RO	0x0	Indicates if the DMA manager was attempting to execute DMAGO with inappropriate security permissions: 0 = DMA manager has appropriate security to execute DMAGO 1 = DMA manager thread in the Non-secure state attempted to execute DMAGO to create a DMA channel operating in the Secure state.
3:2	RO	0x0	reserved
1	RO	0x0	Indicates if the DMA manager was attempting to execute an instruction operand that was not valid for the configuration of the DMAC: 0 = valid operand 1 = invalid operand.
0	RW	0x0	Indicates if the DMA manager was attempting to execute an undefined instruction: 0 = defined instruction 1 = undefined instruction.

DMAC_FTR0~DMAC_FTR7

Address: Operational Base + offset (0x0040)
Operational Base+0x44
Operational Base+0x48
Operational Base+0x4C
Operational Base+0x50
Operational Base+0x54

Operational Base+0x58
Operational Base+0x5C
Fault Type DMA Channel Register

Bit	Attr	Reset Value	Description
31	RO	0x0	Indicates if the DMA channel has locked-up because of resource starvation: 0 = DMA channel has adequate resources 1 = DMA channel has locked-up because of insufficient resources. This fault is an imprecise abort
30	RO	0x0	If the DMA channel aborts, this bit indicates if the erroneous instruction was read from the system memory or from the debug interface: 0 = instruction that generated an abort was read from system memory 1 = instruction that generated an abort was read from the debug interface. This fault is an imprecise abort but the bit is only valid when a precise abort occurs.
29:19	RO	0x0	reserved
18	RO	0x0	Indicates the AXI response that the DMAC receives on the RRESP bus, after the DMA channel thread performs a data read: 0 = OKAY response 1 = EXOKAY, SLVERR, or DECERR response. This fault is an imprecise abort
17	RO	0x0	Indicates the AXI response that the DMAC receives on the BRESP bus, after the DMA channel thread performs a data write: 0 = OKAY response 1 = EXOKAY, SLVERR, or DECERR response. This fault is an imprecise abort.
16	RO	0x0	Indicates the AXI response that the DMAC receives on the RRESP bus, after the DMA channel thread performs an instruction fetch: 0 = OKAY response 1 = EXOKAY, SLVERR, or DECERR response. This fault is a precise abort.
15:14	RO	0x0	reserved
13	RO	0x0	Indicates if the MFIFO did not contain the data to enable the DMAC to perform the DMAST: 0 = MFIFO contains all the data to enable the DMAST to complete 1 = previous DMALDs have not put enough data in the MFIFO to enable the DMAST to complete. This fault is a precise abort.

Bit	Attr	Reset Value	Description
12	RO	0x0	Indicates if the MFIFO prevented the DMA channel thread from executing DMALD or DMAST. Depending on the instruction: DMALD 0 = MFIFO contains sufficient space 1 = MFIFO is too small to hold the data that DMALD requires. DMAST 0 = MFIFO contains sufficient data 1 = MFIFO is too small to store the data to enable DMAST to complete. This fault is an imprecise abort
11:8	RO	0x0	reserved
7	RO	0x0	Indicates if a DMA channel thread, in the Non-secure state, attempts to program the CCRn Register to perform a secure read or secure write: 0 = a DMA channel thread in the Non-secure state is not violating the security permissions 1 = a DMA channel thread in the Non-secure state attempted to perform a secure read or secure write. This fault is a precise abort
6	RO	0x0	Indicates if a DMA channel thread, in the Non-secure state, attempts to execute DMAWFP, DMALDP, DMASTP, or DMAFLUSHP with inappropriate security permissions: 0 = a DMA channel thread in the Non-secure state is not violating the security permissions 1 = a DMA channel thread in the Non-secure state attempted to execute either: o DMAWFP to wait for a secure peripheral o DMALDP or DMASTP to notify a secure peripheral o DMAFLUSHP to flush a secure peripheral. This fault is a precise abort.
5	RO	0x0	Indicates if the DMA channel thread attempts to execute DMAWFE or DMASEV with inappropriate security permissions: 0 = a DMA channel thread in the Non-secure state is not violating the security permissions 1 = a DMA channel thread in the Non-secure state attempted to execute either: DMAWFE to wait for a secure event DMASEV to create a secure event or secure interrupt. This fault is a precise abort.
4:2	RO	0x0	reserved
1	RO	0x0	Indicates if the DMA channel thread was attempting to execute an instruction operand that was not valid for the configuration of the DMAC: 0 = valid operand 1 = invalid operand. This fault is a precise abort.

Bit	Attr	Reset Value	Description
0	RO	0x0	Indicates if the DMA channel thread was attempting to execute an undefined instruction: 0 = defined instruction 1 = undefined instruction. This fault is a precise abort

DMAC_CSR0~DMAC_CSR7

Address:Operational Base+0x100
Operational Base+0x108
Operational Base+0x110
Operational Base+0x118
Operational Base+0x120
Operational Base+0x128
Operational Base+0x130
Operational Base+0x138

Channel Status Registers

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21	RO	0x0	The channel non-secure bit provides the security of the DMA channel: 0 = DMA channel operates in the Secure state 1 = DMA channel operates in the Non-secure state
20:16	RO	0x0	reserved
15	RO	0x0	When the DMA channel thread executes DMAWFP this bit indicates if the periph operand was set: 0 = DMAWFP executed with the periph operand not set 1 = DMAWFP executed with the periph operand set
14	RO	0x0	When the DMA channel thread executes DMAWFP this bit indicates if the burst or single operand were set: 0 = DMAWFP executed with the single operand set 1 = DMAWFP executed with the burst operand set.
13:9	RO	0x0	reserved
8:4	RO	0x00	If the DMA channel is in the Waiting for event state or the Waiting for peripheral state then these bits indicate the event or peripheral number that the channel is waiting for: b00000 = DMA channel is waiting for event, or peripheral, 0 b00001 = DMA channel is waiting for event, or peripheral, 1 b00010 = DMA channel is waiting for event, or peripheral, 2 … b11111 = DMA channel is waiting for event, or peripheral, 31

Bit	Attr	Reset Value	Description
3:0	RO	0x0	The channel status encoding is: b0000 = Stopped b0001 = Executing b0010 = Cache miss b0011 = Updating PC b0100 = Waiting for event b0101 = At barrier b0110 = reserved b0111 = Waiting for peripheral b1000 = Killing b1001 = Completing b1010-b1101 = reserved b1110 = Faulting completing b1111 = Faulting

DMAC_CPC0~DMAC_CPC7

Address:Operational Base+0x104
Operational Base+0x10C
Operational Base+0x114
Operational Base+0x11c
Operational Base+0x124
Operational Base+0x12C
Operational Base+0x134
Operational Base+0x13C

Channel Program Counter Registers

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	Program counter for the DMA channel 0 thread

DMAC_SAR0~DMAC_SAR7

Address:Operational Base+0x400
Operational Base+0x420
Operational Base+0x440
Operational Base+0x460
Operational Base+0x480
Operational Base+0x4A0
Operational Base+0x4C0
Operational Base+0x4E0

Source Address Registers

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	Address of the source data for DMA channel 0

DMAC_DAR0~DMAC_DAR7

Address:Operational Base+0x404
Operational Base+0x424
Operational Base+0x444
Operational Base+0x464
Operational Base+0x484
Operational Base+0x4A4
Operational Base+0x4C4
Operational Base+0x4E4

DestinationAddress Registers

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	Address of the Destination data for DMA channel 0

DMAC_CCR0~DMAC_CCR7

Address: Operational Base+0x408
Operational Base+0x428
Operational Base+0x448
Operational Base+0x468
Operational Base+0x488
Operational Base+0x4A8
Operational Base+0x4C8
Operational Base+0x4E8

Channel Control Registers

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:25	RO	0x0	Programs the state of AWCACHE[3,1:0]a when the DMAC writes the destination data. Bit [27] 0 = AWCACHE[3] is LOW 1 = AWCACHE[3] is HIGH. Bit [26] 0 = AWCACHE[1] is LOW 1 = AWCACHE[1] is HIGH. Bit [25] 0 = AWCACHE[0] is LOW 1 = AWCACHE[0] is HIGH
24:22	RO	0x0	Programs the state of AWPROT[2:0]a when the DMAC writes the destination data. Bit [24] 0 = AWPROT[2] is LOW 1 = AWPROT[2] is HIGH. Bit [23] 0 = AWPROT[1] is LOW 1 = AWPROT[1] is HIGH. Bit [22] 0 = AWPROT[0] is LOW 1 = AWPROT[0] is HIGH
21:18	RO	0x0	For each burst, these bits program the number of data transfers that the DMAC performs when it writes the destination data: b0000 = 1 data transfer b0001 = 2 data transfers b0010 = 3 data transfers … b1111 = 16 data transfers. The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size

Bit	Attr	Reset Value	Description
17:15	RO	0x0	For each beat within a burst, it programs the number of bytes that the DMAC writes to the destination: b000 = writes 1 byte per beat b001 = writes 2 bytes per beat b010 = writes 4 bytes per beat b011 = writes 8 bytes per beat b100 = writes 16 bytes per beat b101-b111 = reserved. The total number of bytes that the DMAC writes out of the MFIFO when it executes a DMAST instruction is the product of dst_burst_len and dst_burst_size.
14	RO	0x0	Programs the burst type that the DMAC performs when it writes the destination data: 0 = Fixed-address burst. The DMAC signals AWBURST[0] LOW. 1 = Incrementing-address burst. The DMAC signals AWBURST[0] HIGH.
13:11	RO	0x0	Set the bits to control the state of ARCACHE[2:0]a when the DMAC reads the source data. Bit [13] 0 = ARCACHE[2] is LOW 1 = ARCACHE[2] is HIGH. Bit [12] 0 = ARCACHE[1] is LOW 1 = ARCACHE[1] is HIGH. Bit [11] 0 = ARCACHE[0] is LOW 1 = ARCACHE[0] is HIGH.
10:8	RO	0x0	Programs the state of ARPROT[2:0]a when the DMAC reads the source data. Bit [10] 0 = ARPROT[2] is LOW 1 = ARPROT[2] is HIGH. Bit [9] 0 = ARPROT[1] is LOW 1 = ARPROT[1] is HIGH. Bit [8] 0 = ARPROT[0] is LOW 1 = ARPROT[0] is HIGH.
7:4	RO	0x0	For each burst, these bits program the number of data transfers that the DMAC performs when it reads the source data: b0000 = 1 data transfer b0001 = 2 data transfers b0010 = 3 data transfers … b1111 = 16 data transfers. The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size

Bit	Attr	Reset Value	Description
3:1	RO	0x0	For each beat within a burst, it programs the number of bytes that the DMAC reads from the source: b000 = reads 1 byte per beat b001 = reads 2 bytes per beat b010 = reads 4 bytes per beat b011 = reads 8 bytes per beat b100 = reads 16 bytes per beat b101-b111 = reserved. The total number of bytes that the DMAC reads into the MFIFO when it executes a DMALD instruction is the product of src_burst_len and src_burst_size
0	RO	0x0	Programs the burst type that the DMAC performs when it reads the source data: 0 = Fixed-address burst. The DMAC signals ARBURST[0] LOW. 1 = Incrementing-address burst. The DMAC signals ARBURST[0] HIGH

DMAC_LC0_0~DMAC_LC0_7

Address: Operational Base+0x40c
Operational Base+0x42C
Operational Base+0x44C
Operational Base+0x46C
Operational Base+0x48C
Operational Base+0x4AC
Operational Base+0x4CC
Operational Base+0x4EC

Loop Counter 0 Registers

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RO	0x00	Loop counter 0 iterations

DMAC_LC1_0~DMAC_LC1_7

Address: Operational Base+0x410
Operational Base+0x430
Operational Base+0x450
Operational Base+0x470
Operational Base+0x490
Operational Base+0x4B0
Operational Base+0x4D0
Operational Base+0x4F0

Loop Counter 1 Registers

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RO	0x00	Loop counter 1 iterations

DMAC_DBGSTATUS

Address: Operational Base + offset (0x0d00)

Debug Status Register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved

Bit	Attr	Reset Value	Description
1:0	RO	0x0	The debug encoding is as follows: b00 = execute the instruction that the DBGINST [1:0] Registers contain b01 = reserved b10 = reserved b11 = reserved.

DMAC_DBGCMD
Address: Operational Base + offset (0x0d04)
Debug Command Register

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1:0	WO	0x0	The debug encoding is as follows: b00 = execute the instruction that the DBGINST [1:0] Registers contain b01 = reserved b10 = reserved b11 = reserved

DMAC_DBGINST0
Address: Operational Base + offset (0x0d08)
Debug Instruction-0 Register

Bit	Attr	Reset Value	Description
31:24	WO	0x00	Instruction byte 1
23:16	WO	0x00	Instruction byte 0
15:11	RO	0x0	reserved
10:8	WO	0x0	DMA channel number: b000 = DMA channel 0 b001 = DMA channel 1 b010 = DMA channel 2 … b111 = DMA channel 7
7:1	RO	0x0	reserved
0	WO	0x0	The debug thread encoding is as follows: 0 = DMA manager thread 1 = DMA channel.

DMAC_DBGINST1
Address: Operational Base + offset (0x0d0c)
Debug Instruction-1 Register

Bit	Attr	Reset Value	Description
31:24	WO	0x00	Instruction byte 5
23:16	WO	0x00	Instruction byte 4
15:8	WO	0x00	Instruction byte 3
7:0	WO	0x00	Instruction byte 2

DMAC_CR0
Address: Operational Base + offset (0x0e00)
Configuration Register 0

Bit	Attr	Reset Value	Description
31:22	RO	0x0	reserved
21:17	RO	0x02	Number of interrupt outputs that the DMAC provides: b00000 = 1 interrupt output, irq[0] b00001 = 2 interrupt outputs, irq[1:0] b00010 = 3 interrupt outputs, irq[2:0] … b11111 = 32 interrupt outputs, irq[31:0].
16:12	RO	0x07	Number of peripheral request interfaces that the DMAC provides: b00000 = 1 peripheral request interface b00001 = 2 peripheral request interfaces b00010 = 3 peripheral request interfaces … b11111 = 32 peripheral request interfaces.
11:7	RO	0x0	reserved
6:4	RO	0x5	Number of DMA channels that the DMAC supports: b000 = 1 DMA channel b001 = 2 DMA channels b010 = 3 DMA channels … b111 = 8 DMA channels.
3	RO	0x0	reserved
2	RO	0x0	Indicates the status of the boot_manager_ns signal when the DMAC exited from reset: 0 = boot_manager_ns was LOW 1 = boot_manager_ns was HIGH.
1	RO	0x0	Indicates the status of the boot_from_pc signal when the DMAC exited from reset: 0 = boot_from_pc was LOW 1 = boot_from_pc was HIGH
0	RO	0x1	Supports peripheral requests: 0 = the DMAC does not provide a peripheral request interface 1 = the DMAC provides the number of peripheral request interfaces that the num_periph_req field specifies.

DMAC_CR1
Address: Operational Base + offset (0x0e04)
Configuration Register 1

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved

Bit	Attr	Reset Value	Description
7:4	RO	0x5	[7:4] num_i-cache_lines Number of i-cache lines: b0000 = 1 i-cache line b0001 = 2 i-cache lines b0010 = 3 i-cache lines … b1111 = 16 i-cache lines.
3	RO	0x0	reserved
2:0	RO	0x7	The length of an i-cache line: b000-b001 = reserved b010 = 4 bytes b011 = 8 bytes b100 = 16 bytes b101 = 32 bytes b110-b111 = reserved

DMAC_CR2
Address: Operational Base + offset (0x0e08)
Configuration Register 2

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	Provides the value of boot_addr[31:0] when the DMAC exited from reset

DMAC_CR3
Address: Operational Base + offset (0x0e0c)
Configuration Register 3

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	Provides the security state of an event-interrupt resource: Bit [N] = 0 Assigns event<N> or irq[N] to the Secure state. Bit [N] = 1 Assigns event<N> or irq[N] to the Non-secure state.

DMAC_CR4
Address: Operational Base + offset (0x0e10)
Configuration Register 4

Bit	Attr	Reset Value	Description
31:0	RO	0x00000006	Provides the security state of the peripheral request interfaces: Bit [N] = 0 Assigns peripheral request interface N to the Secure state. Bit [N] = 1 Assigns peripheral request interface N to the Non-secure state

DMAC_CRDn
Address: Operational Base + offset (0x0e14)
DMA Configuration Register

Bit	Attr	Reset Value	Description
31:30	RO	0x0	reserved

Bit	Attr	Reset Value	Description
29:20	RO	0x020	The number of lines that the data buffer contains: b000000000 = 1 line b000000001 = 2 lines … b111111111 = 1024 lines
19:16	RO	0x9	The depth of the read queue: b0000 = 1 line b0001 = 2 lines … b1111 = 16 lines.
15	RO	0x0	reserved
14:12	RO	0x4	Read issuing capability that programs the number of outstanding read transactions: b000 = 1 b001 = 2 … b111 = 8
11:8	RO	0x7	The depth of the write queue: b0000 = 1 line b0001 = 2 lines … b1111 = 16 lines.
7	RO	0x0	reserved
6:4	RO	0x3	Write issuing capability that programs the number of outstanding write transactions: b000 = 1 b001 = 2 … b111 = 8
3	RO	0x0	reserved
2:0	RO	0x3	The data bus width of the AXI interface: b000 = reserved b001 = reserved b010 = 32-bit b011 = 64-bit b100 = 128-bit b101-b111 = reserved.

DMAC_WD

Address: Operational Base + offset (0x0e80)

DMA Watchdog Register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	Controls how the DMAC responds when it detects a lock-up condition: 0 = the DMAC aborts all of the contributing DMA channels and sets irq_abort HIGH 1 = the DMAC sets irq_abort HIGH.

15.5 Timing Diagram

Following picture shows the relationship between dma_req and dma_ack.

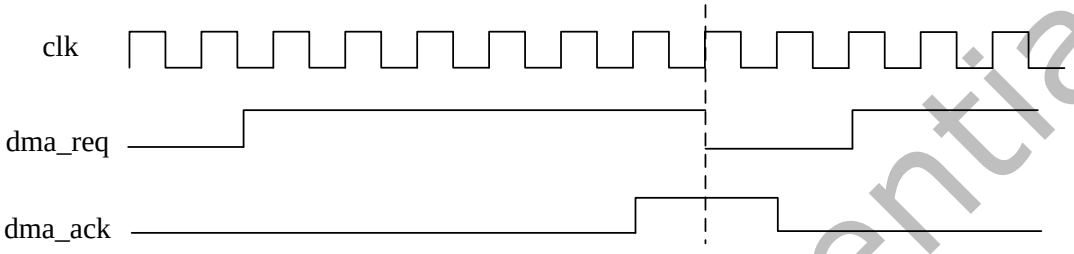


Fig. 15-3 DMAC request and acknowledge timing

15.6 Interface Description

DMAC has the following tie-off signals. It can be configured by SGRF register. (Please refer to the chapter to find how to configure)

Table 15-3 DMAC0 boot interface

Interface	Reset value	Control source
boot_addr	0x0	SGRF
boot_from_pc	0x0	SGRF
boot_manager_ns	0x1	SGRF
boot_irq_ns	0xfff	SGRF
boot_periph_ns	0xfff	SGRF

Table 15-4 DMAC1 boot interface

Interface	Reset value	Control source
boot_addr	0x0	SGRF
boot_from_pc	0x0	SGRF
boot_manager_ns	0x1	SGRF
boot_irq_ns	0xffff	SGRF
boot_periph_ns	0xfffff	SGRF

boot_addr
Configures the address location that contains the first instruction the DMAC executes, when it exits from reset.
boot_from_pc
Controls the location in which the DMAC executes its initial instruction, after it exits from reset:
0 = DMAC waits for an instruction from either APB interface
1 = DMA manager thread executes the instruction that is located at the address that
boot_manager_ns
When the DMAC exits from reset, this signal controls the security state of the DMA manager thread:
0 = assigns DMA manager to the Secure state
1 = assigns DMA manager to the Non-secure state.

boot_irq_ns
Controls the security state of an event-interrupt resource, when the DMAC exits from reset:
boot_irq_ns[x] is LOW
The DMAC assigns event<x> or irq[x] to the Secure state.
boot_irq_ns[x] is HIGH
The DMAC assigns event<x> or irq[x] to the Non-secure state.
boot_periph_ns
Controls the security state of a peripheral request interface, when the DMAC exits from reset:
boot_periph_ns[x] is LOW
The DMAC assigns peripheral request interface x to the Secure state.
boot_periph_ns[x] is HIGH
The DMAC assigns peripheral request interface x to the Non-secure state.

15.7 Application Notes

15.7.1 Using the APB slave interfaces

You must ensure that you use the appropriate APB interface, depending on the security state in which the boot_manager_ns initializes the DMAC to operate. For example, if the DMAC is in the secure state, you must issue the instruction using the secure APB interface, otherwise the DMAC ignores the instruction. You can use the secure APB interface, or the non-secure APB interface, to start or restart a DMA channel when the DMAC is in the Non-secure state.
The necessary steps to start a DMA channel thread using the debug instruction registers as following:
1. Create a program for the DMA channel.
2. Store the program in a region of system memory.
3. Poll the DBGSTATUS Register to ensure that debug is idle, that is, the dbgstatus bit is 0.
4. Write to the DBGINST0 Register and enter the:
- Instruction byte 0 encoding for DMAGO.
- Instruction byte 1 encoding for DMAGO.
- Debug thread bit to 0. This selects the DMA manager thread.

5. Write to the DBGINST1 Register with the DMAGO instruction byte [5:2] data, see Debug Instruction-1 Register o. You must set these four bytes to the address of the first instruction in the program, that was written to system memory in step 2.
6. Writing zero to the DBGCMD Register. The DMAC starts the DMA channel thread and sets the dbgstatus bit to 1.

15.7.2 Security usage

DMA manager thread is in the secure state
If the DNS bit is 0, the DMA manager thread operates in the secure state and it only performs secure instruction fetches. When a DMA manager thread in the secure state processes:
DMAGO
It uses the status of the ns bit, to set the security state of the DMA channel thread by writing to the CNS bit for that channel.
DMAWFE
It halts execution of the thread until the event occurs. When the event occurs, the DMAC continues execution of the thread, irrespective of the security state of the corresponding INS bit.
DMASEV
It sets the corresponding bit in the INT_EVENT_RIS Register, irrespective of the security state of the corresponding INS bit.
DMA manager thread is in the Non-secure state
If the DNS bit is 1, the DMA manager thread operates in the Non-secure state, and it only performs non-secure instruction fetches. When a DMA manager thread in the Non-secure state processes:
DMAGO
The DMAC uses the status of the ns bit, to control if it starts a DMA channel thread. If:
ns = 0

The DMAC does not start a DMA channel thread and instead it:
1. Executes a NOP.
2. Sets the FSRD Register, see Fault Status DMA Manager
3. Sets the dmago_err bit in the FTRD Register, see Fault Type DMA Manager Register.
4. Moves the DMA manager to the Faulting state.

ns = 1

The DMAC starts a DMA channel thread in the Non-secure state and programs the CNS bit to be non-secure.

DMAWFE

The DMAC uses the status of the corresponding INS bit, in the CR3 Register, to control if it waits for the event. If:

INS = 0

The event is in the Secure state. The DMAC:
1. Executes a NOP.
2. Sets the FSRD Register, see Fault Status DMA Manager Register.
3. Sets the mgr_evnt_err bit in the FTRD Register, see Fault Type DMA Manager Register.
4. Moves the DMA manager to the Faulting state.

INS = 1

The event is in the Non-secure state. The DMAC halts execution of the thread and waits for the event to occur.

DMASEV

The DMAC uses the status of the corresponding INS bit, in the CR3Register, to control if it creates the event-interrupt. If:

INS = 0

The event-interrupt resource is in the secure state. The DMAC:
1. Executes a NOP.
2. Sets the FSRD Register, see Fault Status DMA Manager Register.
3. Sets the mgr_evnt_err bit in the FTRD Register, see Fault Type DMA Manager Register.
4. Moves the DMA manager to the Faulting state.

INS = 1

The event-interrupt resource is in the Non-secure state. The DMAC creates the event-interrupt.

DMA channel thread is in the secure state

When the CNS bit is 0, the DMA channel thread is programmed to operate in the Secure state and it only performs secure instruction fetches.

When a DMA channel thread in the secure state processes the following instructions:

DMAWFE

The DMAC halts execution of the thread until the event occurs. When the event occurs, the DMAC continues execution of the thread, irrespective of the security state of the corresponding INS bit, in the CR3 Register.

DMASEV

The DMAC creates the event-interrupt, irrespective of the security state of the corresponding INS bit, in the CR3 Register.

DMAWFP

The DMAC halts execution of the thread until the peripheral signals a DMA request. When this occurs, the DMAC continues execution of the thread, irrespective of the security state of the corresponding PNS bit, in the CR4 Register.

DMALDP, DMASTP

The DMAC sends a message to the peripheral to communicate that data transfer is complete, irrespective of the security state of the corresponding PNS bit, in the CR4 Register.

DMAFLUSHP

The DMAC clears the state of the peripheral and sends a message to the peripheral to resend its level status, irrespective of the security state of the corresponding PNS bit, in the CR4 Register.

When a DMA channel thread is in the Secure state, it enables the DMAC to perform secure and non-secure AXI accesses

DMA channel thread is in the Non-secure state

When the CNS bit is 1, the DMA channel thread is programmed to operate in the Non-secure state and it only performs non-secure instruction fetches.

When a DMA channel thread in the Non-secure state processes the following instructions:

DMAWFE

The DMAC uses the status of the corresponding INS bit, in the CR3 Register, to control if it waits for the event. If:

INS = 0

The event is in the Secure state. The DMAC:

1. Executes a NOP.
2. Sets the appropriate bit in the FSRC Register that corresponds to the DMA channel number. See Fault Status DMA Channel Register.
3. Sets the ch_evnt_err bit in the FTRn Register, see Fault Type DMA Channel Registers.
4. Moves the DMA channel to the Faulting completing state.

INS = 1

The event is in the Non-secure state. The DMAC halts execution of the thread and waits for the event to occur.

DMASEV

The DMAC uses the status of the corresponding INS bit, in the CR3 Register, to control if it creates the event. If:

INS = 0

The event-interrupt resource is in the Secure state. The DMAC:

1. Executes a NOP.
2. Sets the appropriate bit in the FSRC Register that corresponds to the DMA channel number. See Fault Status DMA Channel Register.
3. Sets the ch_evnt_err bit in the FTRn Register, see Fault Type DMA Channel Registers .
4. Moves the DMA channel to the Faulting completing state.

INS = 1

The event-interrupt resource is in the Non-secure state. The DMAC creates the event-interrupt.

DMAWFP

The DMAC uses the status of the corresponding PNS bit, in the CR4 Register, to control if it waits for the peripheral to signal a request. If:

PNS = 0

The peripheral is in the Secure state. The DMAC:

1. Executes a NOP.
2. Sets the appropriate bit in the FSRC Register that corresponds to the DMA channel number. See Fault Status DMA Channel Register.
3. Sets the ch_periph_err bit in the FTRn Register, see Fault Type DMA Channel Registers.
4. Moves the DMA channel to the Faulting completing state.

PNS = 1

The peripheral is in the Non-secure state. The DMAC halts execution of the thread and waits for the peripheral to signal a request.

DMALDP, DMASTP

The DMAC uses the status of the corresponding PNS bit, in the CR4 Register, to control if it sends an acknowledgement to the peripheral. If:

PNS = 0

The peripheral is in the secure state. The DMAC:

1. Executes a NOP.
2. Sets the appropriate bit in the FSRC Register that corresponds to the DMA channel number. See Fault Status DMA Channel Register.
3. Sets the ch_periph_err bit in the FTRn Register, see Fault Type DMA Channel Registers.
4. Moves the DMA channel to the Faulting completing state.

PNS = 1

The peripheral is in the Non-secure state. The DMAC sends a message to the peripheral to communicate when the data transfer is complete.

DMAFLUSHP

The DMAC uses the status of the corresponding PNS bit, in the CR4 Register, to control if it sends a flush request to the peripheral. If:
PNS = 0
The peripheral is in the secure state. The DMAC:
1. Executes a NOP.
2. Sets the appropriate bit in the FSRC Register that corresponds to the DMA channel number. See Fault Status DMA Channel Register.
3. Sets the ch_periph_err bit in the FTRn Register, see Fault Type DMA Channel Registers.
4. Moves the DMA channel to the Faulting completing state.
PNS = 1
The peripheral is in the Non-secure state. The DMAC clears the state of the peripheral and sends a message to the peripheral to resend its level status.
When a DMA channel thread is in the Non-secure state, and a DMAMOV CCR instruction attempts to program the channel to perform a secure AXI transaction, the DMAC:
1. Executes a DMANOP.
2. Sets the appropriate bit in the FSRC Register that corresponds to the DMA channel number. See Fault Status DMA Channel Register.
3. Sets the ch_rdwr_err bit in the FTRn Register, see Fault Type DMA Channel Registers.
4. Moves the DMA channel thread to the Faulting completing state.

15.7.3 Programming restrictions

Fixed unaligned bursts
The DMAC does not support fixed unaligned bursts. If you program the following conditions, the DMAC treats this as a programming error:
Unaligned read
- src_inc field is 0 in the CCRn Register
- the SARn Register contains an address that is not aligned to the size of data that the src_burst_size field contain

Unaligned write
- dst_inc field is 0 in the CCRn Register
- the DARn Register contains an address that is not aligned to the size of data that the dst_burst_size field contains

Endian swap size restrictions
If you program the endian_swap_size field in the CCRn Register, to enable a DMA channel to perform an endian swap then you must set the corresponding SARn Register and the corresponding DARn Register to contain an address that is aligned to the value that the endian_swap_size field contains.
Updating DMA channel control registers during a DMA cycle restrictions
Prior to the DMAC executing a sequence of DMALD and DMAST instructions, the values you program in to the CCRn Register, SARn Register, and DARn Register control the data byte lane manipulation that the DMAC performs when it transfers the data from the source address to the destination address. You'd better not update these registers during a DMA cycle.
Resource sharing between DMA channels
DMA channel programs share the MFIFO data storage resource. You must not start a set of concurrently running DMA channel programs with a resource requirement that exceeds the configured size of the MFIFO. If you exceed this limit then the DMAC might lock up and generate a Watchdog abort.

15.7.4 Unaligned transfers may be corrupted

For a configuration with more than one channel, if any of channels 1 to 7 is performing transfers between certain types of misaligned source and destination addresses, then the output data may be corrupted by the action of channel 0.
Data corruption might occur if all of the following are true:
1. Two beats of AXI read data are received for one of channels 1 to 7.
2. Source and destination address alignments mean that each read data beat is splited across two lines in the data buffer (see Splitting data, below).
3. There is one idle cycle between the two read data beats.
4. Channel 0 performs an operation that updates channel control information during this idle

cycle (see Updates to channel control information, below)

Splitting data

Depending upon the programmed values for the DMA transfer, one beat of read data from the AXI interface need to be splited across two lines in the internal data buffer. This occurs when the read data beat contains data bytes which will be written to addresses that wrap around at the AXI interface data width, so that these bytes could not be transferred by a single AXI write data beat of the full interface width.

Most applications of DMA-330 do not split data in this way, so are NOT vulnerable to data corruption from this defect.

The following cases are NOT vulnerable to data corruption because they do not split data:

- Byte lane offset between source and destination addresses is 0 when source and destination addresses have the same byte lane alignment, the offset is 0 and a wrap operation that splits data cannot occur.
- Byte lane offset between source and destination addresses is a multiple of source size

Table 15-5 Source size in CCRn

Source size in CCRn	Allowed offset between SARn and DARn
SS8	any offset allowed.
SS16	0,2,4,6,8,10,12,14
SS32	0,4,8,12
SS64	0,8

15.7.5 Interrupt shares between channel

As the DMAC does not record which channel (or list of channels) have asserted an interrupt. So it will depend on your program and whether any of the visible information for that program can be used to determine progress, and help identify the interrupt source.

There are 4 likely information sources that can be used to determine the progress made by a program:

- Program counter (PC)
- Source address
- Destination address
- Loop counters (LC)

For example, a program might emit an interrupt each time that it iterates around a loop. In this case, the interrupt service routine (ISR) would need to store the loop value of each channel when it is called, and then compare against the new value when it is next called. A change in value would indicate that the program has progressed.

The ISR must be carefully written to ensure that no interrupts are lost. The sequence of operations is as follows:

1. Disable interrupts
2. Immediately clear the interrupt in DMA-330
3. Check the relevant registers for both channels to determine which must be serviced
4. Take appropriate action for the channels
5. Re-enable interrupts and exit ISR

15.7.6 Instruction sets

Table 15-6 DMAC Instruction sets

Mnemonic	Instruction	Thread usage
DMAADDH	Add Halfword	C
DMAEND	End	M/C
DMAFLUSHP	Flush and notify Peripheral	C
DMAGO	Go	M
DMAKILL	Kill	C
DMALD	Load	C
DMALDP	Load Peripheral	C
DMALP	Loop	C
DMALPEND	Loop End	C
DMALPFE	Loop Forever	C

Mnemonic	Instruction	Thread usage
DMAMOV	Move	C
DMANOP	No operation	M/C
DMARMB	Read Memory Barrier	C
DMASEV	Send Event	M/C
DMAST	Store	C
DMASTP	Store and notify Peripheral	C
DMASTZ	Store Zero	C
DMAWFE	Wait For Event M	M/C
DMAWFP	Wait For Peripheral	C
DMAWMB	Write Memory Barrier	C
DMAADNH	Add Negative Halfword	C

Notes: Thread usage: C=DMA channel, M=DMA manager

15.7.7 Assembler directives

In this document, only DMMADNH instruction is took as an example to show the way the instruction assembled.

DMAADNH

Add Negative Halfword adds an immediate negative 16-bit value to the SARn Register or DARn Register, for the DMA channel thread. This enables the DMAC to support 2D DMA operations, or reading or writing an area of memory in a different order to naturally incrementing addresses. See Source Address Registers and Destination Address Registers.

The immediate unsigned 16-bit value is one-extended to 32 bits, to create a value that is the two's complement representation of a negative number between -65536 and -1, before the DMAC adds it to the address using 32-bit addition. The DMAC discards the carry bit so that addresses wrap from 0xFFFFFFFF to 0x00000000. The net effect is to subtract between 65536 and 1 from the current value in the Source or Destination Address Register.

Following table shows the instruction encoding.

Table 15-7 DMAC instruction encoding

Imm[15:8]	Imm[7:0]	0	1	0	1	1	1	ra	0

Assembler syntax

DMAADNH <address_register>, <16-bit immediate>

where:

<address_register>

Selects the address register to use. It must be either:

SAR

SARn Register and sets ra to 0.

DAR

DARn Register and sets ra to 1.

<16-bit immediate>

The immediate value to be added to the <address_register>.

You should specify the 16-bit immediate as the number that is to be represented in the instruction encoding. For example, DMAADNH DAR, 0xFFF0 causes the value 0xFFFFFFF0 to be added to the current value of the Destination Address Register, effectively subtracting 16 from the DAR.

You can only use this instruction in a DMA channel thread.

Chapter 16 System Security

16.1 Overview

The RK3399 support the system security application requirement base on the TrustZone access control scheme. The following secure feature are supported

- Secure control of JTAG access
- Secure boot
- eight secure address space in DDR device, the start address and end address for each address scope is configurable, maximum 4GB secure address are supported
- 192K secure internal SRAM
- Many devices are configurable to act as secure or non-secure

16.2 Block Diagram

The following figure show the system security architecture. All the devices which support security access are demonstrated in this figure.

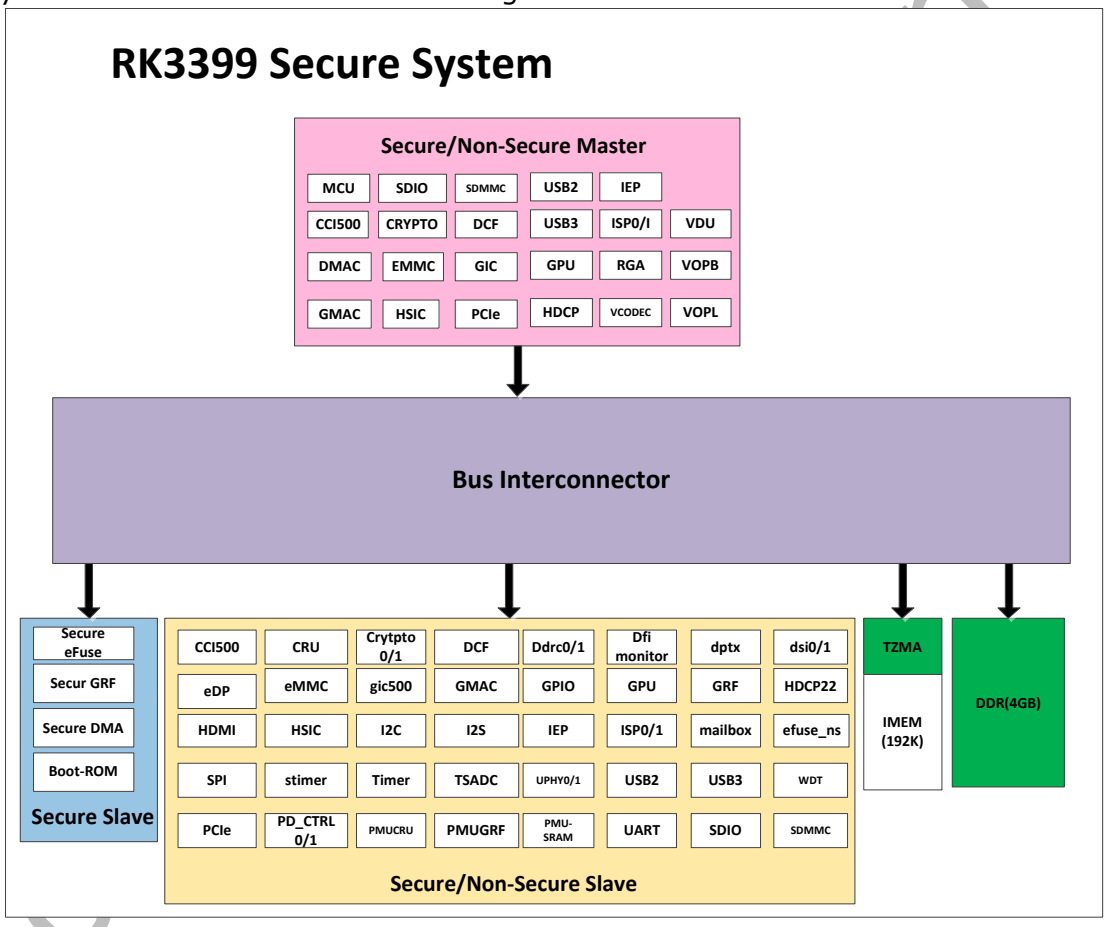


Fig. 16-1 RK3399 security architecture

16.3 Function Description

16.3.1 Cortex-A53/Cortex-A72 Security Extension architecture

The processor implements the TrustZone Security Extensions architecture to facilitate the development of secure applications.
Security Extensions are based on these fundamental principles:

- The extensions define a class of core operation that you can switch between secure and non-secure state. Most code runs in non-secure state. Only trusted code runs in secure state
- The extensions define some memory as secure memory. When the core is in secure state, it can access secure memory

- Entry into secure state is strictly controlled
- Exit from secure state can only occur at programmed points
- Debug is strictly controlled
- The processor enters secure state on reset

16.3.2 TZMA

The TZMA (TrustZone Memory Adapter) is a bridge between AXI bus and Embedded SRAM, which support the flexible secure access by controlling R0SIZE port.

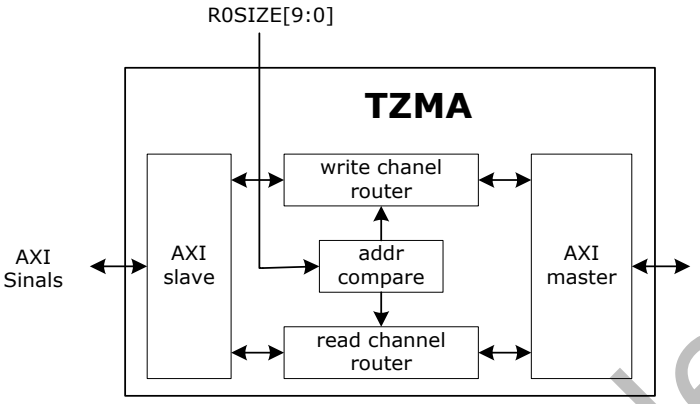


Fig. 16-2 TZMA block diagram

TZMA can support 0KB, 4KB, 8KB, 12KB… up to 192KB by 4KB step(the whole Embedded SRAM space) secure access by setting SGRF_SOC_CON4[9:0].

16.3.3 DMAC_BUS secure access

The DMAC_BUS is an AMBA compliant peripheral, which provides an AXI interface to perform the DMA transfer and two APB interfaces that control its operation. The DMAC_BUS implements TrustZone secure technology with one APB interface operating in the secure state and the other operating in the Non-secure state. For the detailed description for DMAC_BUS, please refer to Chapter 10.

The following diagram shows the interface of DMAC_BUS.

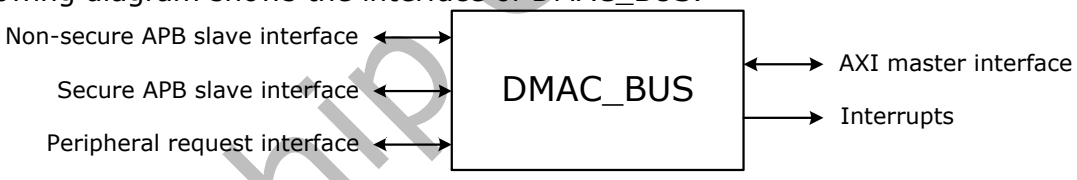


Fig. 16-3 DMAC_BUS interface

The DMAC_BUS support the secure feature in the following section:

- DMA manager thread
- DMA channel thread
- Event and interrupts
- Peripheral request interface

1. The security of DMA manager thread is controlled by input port boot_manager_ns.
0=assign DMA manager to the Secure state
1=assign DMA manager to the Non-secure state
2. The security of DMA channel thread is controlled by instruction DMAGO ns bit. If ns is present, DMA channel operation is in the non-secure state. Otherwise, the execution of the instruction depends on the security of the state of DMA manager:
DMA manager is in the secure state, DMA channel operates in the secure state
DMA manager is in the non-secure state, DMA abort
3. The security state of the event-interrupt source is controlled by the input port boot_irq_ns[x:0], if boot_irq_ns[x] is LOW, the DMAC_BUS assign event<x> or irq[x] to the secure state, otherwise the DMAC_BUS assign event<x> or irq[x] to the non-secure state.
4. The security state of peripheral request interface is controlled by the input port boot_irq_ns[x], if boot_irq_ns[x] is lOW, the DMAC_BUS assign peripheral interface x to secure state, otherwise the DMAC_BUS assign peripheral interface x to non-secure state.

16.3.4 Bus components security setting

The following table describes the security support on bus components which have the master interface or slave interface.

Table 16-1 bus components security setting

AXI master	secure	All transactions originating from this master interface are flagged as secure transaction and can access both secure and non-secure component.
	non-secure	All transactions originating from this master interface are flagged as non-secure transactions and cannot access secure component
	per access	The AxPROTx signal determines the security setting of each transaction, and the slave that it can access
	per configure	Can be configured act as secure or non-secure by Secure GRF register
AHB-Lite master	secure	All transactions originating from this master interface are flagged as secure transaction and can access both secure and non-secure component.
	non-secure	All transactions originating from this master interface are flagged as non-secure transactions and cannot access secure component
	per configure	Can be configured act as secure or non-secure by Secure GRF register
AXI slave	secure	Only secure transactions can access this component
	non-secure	Both secure and non-secure transactions can access this components
	boot-secure	You can use software to configure whether it permits secure and non-secure transactions to access component. When boot up, this component only can be accessed by secure transactions.
	per configure	Can be configured act as secure or non-secure by Secure GRF register
AHB slave	secure	Only secure transactions can access this components
	non-secure	Both secure and non-secure transactions can access this components
	boot-secure	You can use software to configure whether it permit secure and non-secure transactions to access this components. When boot up, this component only can be accessed by secure transactions.
	per configure	Can be configured act as secure or non-secure by Secure GRF register
APB slave	secure	Only secure transactions can access this components
	non-secure	Both secure and non-secure transactions can access this components
	boot-secure	You can use software to configure whether it permit secure and non-secure transactions to access this components. When boot up, this component only can be accessed by secure transactions.

	per configure	Can be configured act as secure or non-secure by Secure GRF register

Notes: When a non-secure master tries to access a secure slave, an error response will be returned. In RK3399, Cortex-A53 non-secure access a secure slave will cause a data-abort, and dmac_bus non-secure access a secure slave will cause an interrupt for access error.

16.3.5 RK3399 secure master setting

Table 16-2 RK3399 secure master setting

IP	Bus type	Secure type	Configuration
cci_m0	AXI	per configure	rgn_ctrl[263:256]
ccidbg	AHB	per configure	rgn_ctrl[271:264]
crypto	AHB	per configure	rgn_ctrl[279:272]
crypto1	AHB	per configure	rgn_ctrl[247:240]
dcf	AXI	per configure	rgn_ctrl[287:280]
dmac0	AXI	per configure	rgn_ctrl[295:288]
dmac1	AXI	per configure	rgn_ctrl[303:296]
emmc	AHB	per configure	rgn_ctrl[311:304]
gic	AXI	per configure	rgn_ctrl[319:312]
gmac	AHB	per configure	rgn_ctrl[327:320]
hsic	AHB	per configure	rgn_ctrl[335:328]
pcie	AXI	per configure	rgn_ctrl[343:336]
perilp_cm0	AHB	per configure	rgn_ctrl[351:344]
pmu_cm0	AHB	per configure	rgn_ctrl[359:352]
sdio	AHB	per configure	rgn_ctrl[367:360]
sdmmc	AHB	per configure	rgn_ctrl[375:368]
usb2host0	AHB	per configure	rgn_ctrl[383:376]
usb2host1	AHB	per configure	rgn_ctrl[391:384]
usb3otg0	AXI	per configure	rgn_ctrl[399:392]
usb3otg1	AXI	per configure	rgn_ctrl[407:400]
cci_m1	AXI	per configure	rgn_ctrl[415:408]
gpu	AXI	per configure	rgn_ctrl[423:416]
hdcp	AXI	per configure	rgn_ctrl[431:424]
iep	AXI	per configure	rgn_ctrl[439:432]
isp0	AXI	per configure	rgn_ctrl[447:440]
isp1	AXI	per configure	rgn_ctrl[455:448]
rga	AXI	per configure	rgn_ctrl[463:456]
vcodec	AXI	per configure	rgn_ctrl[471:464]
vdu	AXI	per configure	rgn_ctrl[479:472]
vopb_rd	AXI	per configure	rgn_ctrl[487:480]
vopb_wr	AXI	per configure	rgn_ctrl[255:248]
vopl	AXI	per configure	rgn_ctrl[497:488]

Table 16-3 RK3399 secure device setting

16.3.6 RK3399 secure slave setting

Table 16-4 RK3399 secure slave setting

IP	Bus type	Secure type	Configuration
secure_grf	APB	Secure	NA
efuse1	APB	Secure	NA
bootrom	AHB	Secure	NA

IP	Bus type	Secure type	Configuration
secure_dma	APB	Secure	NA
cci500	APB	per configure	rk_slv_sctrl[89]
cic	APB	per configure	rk_slv_sctrl[48]
cru	APB	per configure	rk_slv_sctrl[57]
crypto1	AHB	per configure	rk_slv_sctrl[95]
crypto0	AHB	per configure	rk_slv_sctrl[77]
dcf	APB	per configure	rk_slv_sctrl[55]
ddrc0	internal bus	per configure	rk_slv_sctrl[90]
ddrc1	internal bus	per configure	rk_slv_sctrl[91]
debug	APB	per configure	rk_slv_sctrl[26]
dfimonitor	APB	per configure	rk_slv_sctrl[49]
dp	APB	per configure	rk_slv_sctrl[29]
dsihost0	APB	per configure	rk_slv_sctrl[83]
dsihost1	APB	per configure	rk_slv_sctrl[84]
edp	APB	per configure	rk_slv_sctrl[85]
emmc	AHB	per configure	rk_slv_sctrl[21]
gasket	APB	per configure	rk_slv_sctrl[30]
gic500	APB	per configure	rk_slv_sctrl[31]
gmac	APB	per configure	rk_slv_sctrl[18]
gpio0	APB	per configure	rk_slv_sctrl[14]
gpio1	APB	per configure	rk_slv_sctrl[15]
gpio2	APB	per configure	rk_slv_sctrl[59]
gpio3	APB	per configure	rk_slv_sctrl[60]
gpio4	APB	per configure	rk_slv_sctrl[61]
gpu	APB	per configure	rk_slv_sctrl[88]
grf	APB	per configure	rk_slv_sctrl[58]
hdcp22	APB	per configure	rk_slv_sctrl[87]
hdcpmmu	APB	per configure	rk_slv_sctrl[82]
hdmi	APB	per configure	rk_slv_sctrl[86]
hsic_phy	APB	per configure	rk_slv_sctrl[23]
hsic	APB	per configure	rk_slv_sctrl[22]
i2c1	APB	per configure	rk_slv_sctrl[33]
i2c3	APB	per configure	rk_slv_sctrl[35]
i2c7	APB	per configure	rk_slv_sctrl[38]
i2c6	APB	per configure	rk_slv_sctrl[37]
i2c2	APB	per configure	rk_slv_sctrl[34]
i2c5	APB	per configure	rk_slv_sctrl[36]
i2s0	APB	per configure	rk_slv_sctrl[74]
i2s1	APB	per configure	rk_slv_sctrl[75]
i2s2	APB	per configure	rk_slv_sctrl[76]
iep	APB	per configure	rk_slv_sctrl[52]
intrarb	APB	per configure	rk_slv_sctrl[62]
intmem0	APB	per configure	rk_slv_sctrl[93]
isp0	APB	per configure	rk_slv_sctrl[80]

IP	Bus type	Secure type	Configuration
isp1	APB	per configure	rk_slv_sctrl[81]
mailbox0	APB	per configure	rk_slv_sctrl[56]
efuse0	APB	per configure	rk_slv_sctrl[54]
pcie_apb	APB	per configure	rk_slv_sctrl[17]
pcie_axi	AXI	per configure	rk_slv_sctrl[16]
pdcon0	APB	per configure	rk_slv_sctrl[63]
pdcon1	APB	per configure	rk_slv_sctrl[64]
pmu_cru	APB	per configure	rk_slv_sctrl[13]
pmu_grf	APB	per configure	rk_slv_sctrl[1]
i2c8	APB	per configure	rk_slv_sctrl[11]
i2c0	APB	per configure	rk_slv_sctrl[9]
pmui2c4	APB	per configure	rk_slv_sctrl[10]
intarb0	APB	per configure	rk_slv_sctrl[2]
mailbox1	APB	per configure	rk_slv_sctrl[7]
pwm	APB	per configure	rk_slv_sctrl[12]
spi3	APB	per configure	rk_slv_sctrl[3]
intmem1	APB	per configure	rk_slv_sctrl[8]
pmu	APB	per configure	rk_slv_sctrl[0]
pmutimer	APB	per configure	rk_slv_sctrl[4]
uart4	APB	per configure	rk_slv_sctrl[5]
wdt2	APB	per configure	rk_slv_sctrl[6]
rga	AHB	per configure	rk_slv_sctrl[53]
rkvdec	AHB	per configure	rk_slv_sctrl[51]
saradc	APB	per configure	rk_slv_sctrl[32]
sdio	APB	per configure	rk_slv_sctrl[19]
sdmmc	AHB	per configure	rk_slv_sctrl[20]
spdif	AHB	per configure	rk_slv_sctrl[73]
spi1	APB	per configure	rk_slv_sctrl[44]
spi5	APB	per configure	rk_slv_sctrl[94]
spi4	APB	per configure	rk_slv_sctrl[46]
spi0	APB	per configure	rk_slv_sctrl[43]
spi2	APB	per configure	rk_slv_sctrl[45]
stimer0	APB	per configure	rk_slv_sctrl[70]
stimer1	APB	per configure	rk_slv_sctrl[71]
timer0	APB	per configure	rk_slv_sctrl[68]
timer1	APB	per configure	rk_slv_sctrl[69]
tsadc	APB	per configure	rk_slv_sctrl[47]
uart1	APB	per configure	rk_slv_sctrl[40]
uart0	APB	per configure	rk_slv_sctrl[39]
uart2	APB	per configure	rk_slv_sctrl[41]
uart3	APB	per configure	rk_slv_sctrl[42]
uphy0	APB	per configure	rk_slv_sctrl[65]
uphy1	APB	per configure	rk_slv_sctrl[72]
usb2host0	AHB	per configure	rk_slv_sctrl[24]

IP	Bus type	Secure type	Configuration
usb2host1	AHB	per configure	rk_slv_sctrl[25]
usb3otg0	AHB	per configure	rk_slv_sctrl[27]
usb3otg1	AHB	per configure	rk_slv_sctrl[28]
vcodec	AHB	per configure	rk_slv_sctrl[50]
vopb	AHB	per configure	rk_slv_sctrl[79]
vopl	AHB	per configure	rk_slv_sctrl[78]
wdt0	APB	per configure	rk_slv_sctrl[66]
wdt1	APB	per configure	rk_slv_sctrl[67]

16.3.7 RK3399 device secure input port setting

The following table lists all the secure input ports for the secure device. These secure input ports could be set by configuring SGRF registers.

Table 16-5 RK3399 device secure input port setting

Input Port	Module	Function description
boot_manager_ns	DMAC_BUS	When the DMAC exits from reset, this signal controls the security state of the DMAmanager thread: 1'b0: assigns DMA manager to the secure state 1'b1: assigns DMA manager to the non-secure state
boot_perih_ns[2:0]	DMAC_BUS	Controls the security state of a peripheral request interface, when the DMAC exits from reset: boot_periph_ns[x] is LOW The DMAC assigns peripheral request interface x to the secure state boot_periph_ns[x] is HIGH The DMAC assigns peripheral request interface x to the non-secure state.
boot_irq_ns[7:0]	DMAC_BUS	Controls the security state of an event-interrupt resource, when the DMAC exits fromreset: boot_irq_ns[x] is LOW The DMAC assigns event<x> or irq[x] to the secure state. boot_irq_ns[x] is HIGH The DMAC assigns event<x> or irq[x] to the non-secure state.

16.3.8 Secure JTAG

The JTAG access is controlled by system secure control register, the following table show the detailed information about the secure control to JTAG.

JTAG Type	Register
CA53 JTAG	SGRF_SOC_CON0[3] SGRF_SOC_CON0[4] SGRF_SOC_CON0[5] SGRF_SOC_CON0[6]

16.4 Application Notes

Secure software conception

The basis of the security extensions model is that the computing environment splits into two isolated states, the secure state and the non-secure state, with no leakage of secure data to the non-secure state. Software secure monitor code, running in the monitor mode, links the two states and acts as a gatekeeper to manage program flow. The system can have both secure and non-secure peripherals that are suitable to secure and non-secure device driver control. Following figure shows the relationship between the secure and non-secure states.

The operating system (OS) splits into the secure OS, that includes the secure kernel, and the non-secure OS, that includes the non-secure kernel.

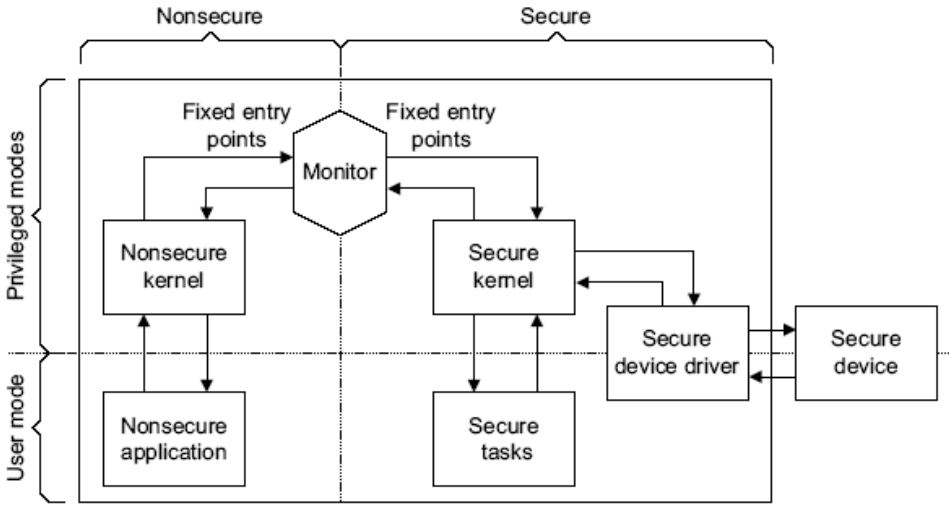


Fig. 16-4 Software Diagram of Secure and Non-secure

In normal non-secure operation, the OS runs tasks in the usual way. When a user process requires secure execution it makes a request to the secure kernel, that operates in privileged mode. This then calls the secure monitor to transfer execution to the secure state.
This approach to secure systems means that the platform OS that works in the non-secure state, has only a few fixed entry points into the secure state through the secure monitor. The trusted code base for the secure state, that includes the secure kernel and secure device drivers, is small and therefore much easier to maintain and verify.

Secure/Non-secure memory space for Embedded SRAM

The following figure gives an example of embedded SRAM secure/non-secure memory space setting. The software configure 4KB secure space. The bottom 4KB space will act as secure space and the other 188K space will be non-secure space.

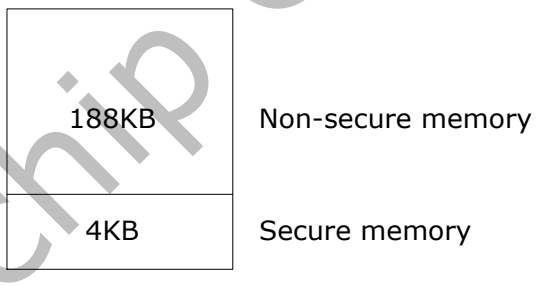


Fig. 16-5 Embedded SRAM secure memory space setting

Chapter 17 Process-Voltage-Temperature Monitor (PVTM)

17.1 Overview

The Process-Voltage-Temperature Monitor (PVTM) is used to monitor the chip performance variance caused by chip process, voltage and temperature.
PVTM supports the following features:

- A clock oscillation ring is integrated and used to generate a clock like signal, the frequency of this clock is determined by the cell delay value of clock oscillation ring circuit.
- A frequency counter is used to measure the frequency of the clock oscillation ring.
- Follow PVTM blocks are supported:
  - core_l_pvtm, used near Cortex-A53
  - core_b_pvtm, used near Cortex-A72
  - ddr_pvtm, used near DDR
  - gpu_pvtm, used near GPU
  - pmu_pvtm, used near PMU

17.2 Block Diagram

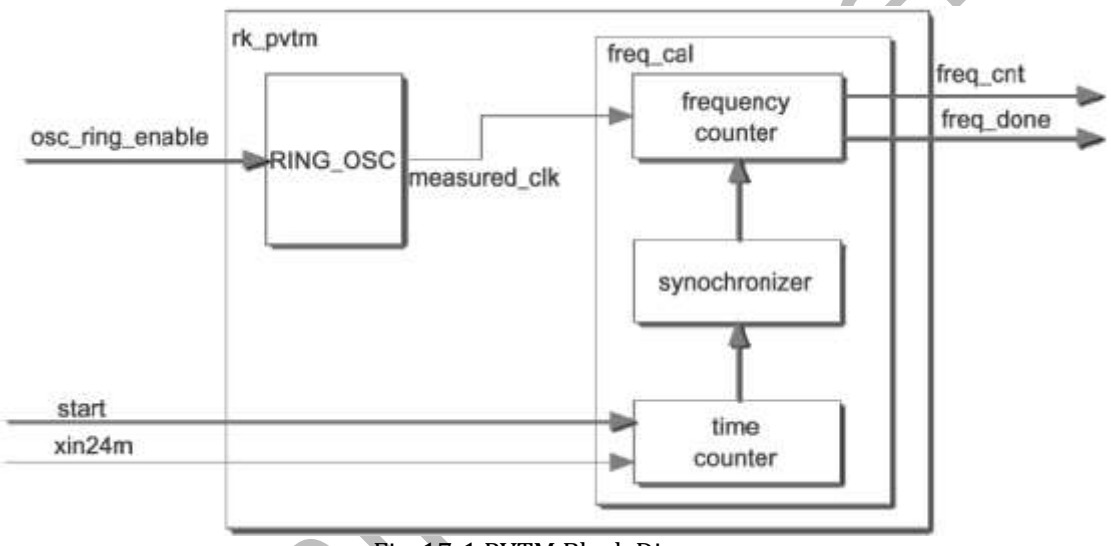


Fig. 17-1 PVTM Block Diagram

The PVTM include two main blocks:

- RING_OSC, it is composed with inverters with odd number, which is used to generate a clock. core_l_pvtm, core_b_pvtm, gpu_pvtm and ddr_pvtm support multiple clock oscillation ring in RING_OSC, and finally select a clock output by signal osc_ring_sel.
- Freq_cal, it is used to measure the frequency of clock which generated from the RING_SOC block.

17.3 Function Description

17.3.1 Frequency Calculation

A clock is generated by the RING_OSC, and a frequency fixed clock (24MHz) is used to calculate the cycles of the clock. Suppose the time period is 1s, then the clock period of RING_OSC clock is T= 1/clock_counter(s), the cell delay value is T/2.

17.3.2 Control Source and Result Destination

The pvtm is controlled by CRU and GRF, and the monitor result is geted by GRF. Following tables shows the PVTM control source and result destination.

Table 17-1 core_l_pvtm control source and result destination

Interface	Reset value	Control Source/Result Destination
xin24m	0x0	CRU_CLKGATE0_CON[7], clock gating control

Interface	Reset value	Control Source/Result Destination
resetn	0x1	CRU_SOFTRST1_CON[15], reverse connect to resetn, active high
start	0x0	GRF_DLL_CON0[0], active high
osc_ring_enable	0x0	GRF_DLL_CON0[1], active high
osc_ring_sel	0x0	GRF_DLL_CON0[3:2]
cal_cnt	0x0	GRF_DLL_CON1[31:0]
freq_done	0x0	GRF_DLL_STATUS0[0]
freq_cnt	0x0	GRF_DLL_STATUS1[31:0]

Table 17-2 core_b_pvtm control source and result destination

Interface	Reset value	Control Source/Result Destination
xin24m	0x0	CRU_CLKGATE1_CON[7], clock gating control
resetn	0x1	CRU_SOFTRST2_CON[15], reverse connect to resetn, active high
start	0x0	GRF_DLL_CON0[4], active high
osc_ring_enable	0x0	GRF_DLL_CON0[5], active high
osc_ring_sel	0x0	{ GRF_DLL_CON5[0], GRF_DLL_CON0[7:6]}, only 0~5 is valid
cal_cnt	0x0	GRF_DLL_CON2[31:0]
freq_done	0x0	GRF_DLL_STATUS0[1]
freq_cnt	0x0	GRF_DLL_STATUS2[31:0]

Table 17-3 ddr_pvtm control source and result destination

Interface	Reset value	Control Source/Result Destination
xin24m	0x0	CRU_CLKGATE4_CON[11], clock gating control
resetn	0x1	CRU_SOFTRST4_CON[15], reverse connect to resetn, active high
start	0x0	GRF_DLL_CON0[8], active high
osc_ring_enable	0x0	GRF_DLL_CON0[9], active high
osc_ring_sel	0x0	GRF_DLL_CON0[11:10]
cal_cnt	0x0	GRF_DLL_CON3[31:0]
freq_done	0x0	GRF_DLL_STATUS0[2]
freq_cnt	0x0	GRF_DLL_STATUS3[31:0]

Table 17-4 gpu_pvtm control source and result destination

Interface	Reset value	Control Source/Result Destination
xin24m	0x0	CRU_CLKGATE13_CON[1], clock gating control
resetn	0x1	CRU_SOFTRST18_CON[3], reverse connect to resetn, active high
start	0x0	GRF_DLL_CON0[12], active high
osc_ring_enable	0x0	GRF_DLL_CON0[13], active high
osc_ring_sel	0x0	GRF_DLL_CON0[15:14]
cal_cnt	0x0	GRF_DLL_CON4[31:0]

Interface	Reset value	Control Source/Result Destination
freq_done	0x0	GRF_DLL_STATUS0[3]
freq_cnt	0x0	GRF_PSDLL_STATUS4[31:0]

Table 17-5 pmu_pvtm control source and result destination

Interface	Reset value	Control Source/Result Destination
xin24m	0x0	PMU_CLKGATE_CON0[7], clock gating control
resetn	0x1	PMU_SOFTRST_CON1[11], reverse connect to resetn, active high
start	0x0	PMUGRF_DLL_CON0[0], active high
osc_ring_enable	0x0	PMUGRF_DLL_CON0[1], active high
cal_cnt	0x0	PMUGRF_DLL_CON1[31:0]
freq_done	0x0	PMUGRF_DLL_STATUS0[0]
freq_cnt	0x0	PMUGRF_DLL_STATUS1[31:0]

17.3.3 pmu_pvtm usage

A clock dividered from pmu_pvtm oscillation ring is used in low power mode, which can replace the function of 32KHz clock source by configure PMUGRF_SOC_CON0[0]. The division factor is configured by PMUGRF_DLL_CON0[15:2].

17.4 Application Notes

17.4.1 PVTM Usage Flow

1. Enable the frequency fixed clock xin24m.
2. Reset the pvtm.
3. Set osc_ring_enable '1' to enable the generated clock.
4. Set osc_ring_sel to select the clock oscillation ring(Only core_b_pvtm, core_l_pvtm, ddr_pvtm and gpu_pvtm need)
5. Configure the cal_cnt to an appropriate value.
6. Set start '1' to calculate the cycles of the generated clock.
7. Wait the freq_done is asserted, then get the value of freq_cnt. The period of RING_OSC clock is T= cal_cnt*(Period of 24MHz clock)/freq_cnt, the cell delay value is T/2.

Chapter 18 Temperature-Sensor ADC(TS-ADC)

18.1 Overview

TS-ADC Controller module supports user-defined mode and automatic mode. User-defined mode refers, TSADC all the control signals entirely by software writing to register for direct control. Automatic mode refers to the module automatically poll TSADC output, and the results were checked. If you find that the temperature High in a period of time, an interrupt is generated to the processor down-measures taken; if the temperature over a period of time High, the resulting TSHUT gave CRU module, let it reset the entire chip, or via GPIO give PMIC.
TS-ADC Controller supports the following features:

- Support User-Defined Mode and Automatic Mode
- In User-Defined Mode, start_of_conversion can be controlled completely by software, and also can be generated by hardware.
- In Automatic Mode, the temperature of alarm(high/low temperature) interrupt can be configurable
- In Automatic Mode, the temperature of system reset can be configurable
- Support to 2 channel TS-ADC, the temperature criteria of each channel can be configurable
- In Automatic Mode, the time interval of temperature detection can be configurable
- In Automatic Mode, when detecting a high temperature, the time interval of temperature detection can be configurable
- High temperature debounce can be configurable
- -40~125°C temperature range and 5°C temperature resolution
- 10-bit SARADC up to 50KS/s sampling rate

18.2 Block Diagram

TS-ADC controller comprises with:

- APB Interface
- TS-ADC control logic

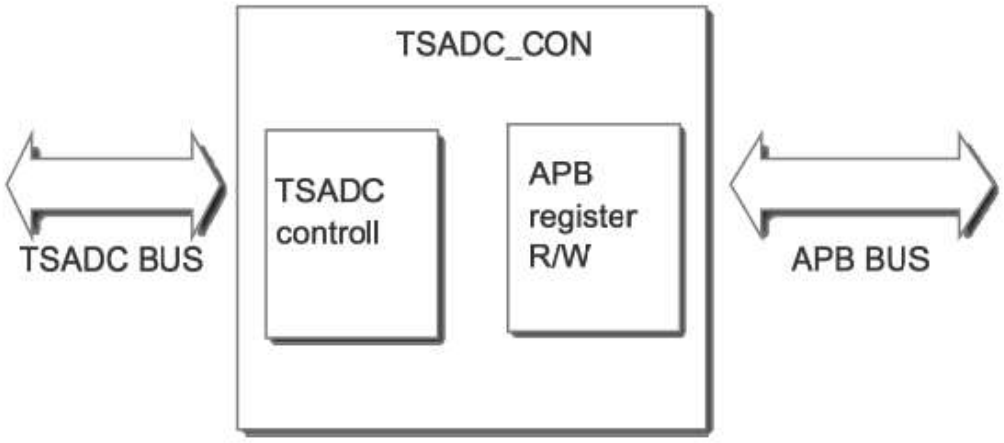


Fig. 18-1 TS-ADC Controller Block Diagram

18.3 Function Description

18.3.1 APB Interface

There is an APB Slave interface in TS-ADC Controller, which is used to configure the TS-ADC Controller registers and look up the temperature from the temperature sensor.

18.3.2 TS-ADC Controller

This block is exploited to realize binary search algorithm, storing the intermediate result and generate control signal for analog block.This block compares the analog input with the voltage

generated from D/A Converter, and output the comparison result to SAR and Control Logic Block for binary search. Three level amplifiers are employed in this comparator to provide enough gain.

18.4 Register description

18.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
TSADC_USER_CON	0x0000	W	0x00000208	The control register of A/D Converter.
TSADC_AUTO_CON	0x0004	W	0x00000000	TSADC auto mode control register
TSADC_INT_EN	0x0008	W	0x00000000	
TSADC_INT_PD	0x000c	W	0x00000000	
TSADC_DATA0	0x0020	W	0x00000000	This register contains the data after A/D Conversion.
TSADC_DATA1	0x0024	W	0x00000000	This register contains the data after A/D Conversion.
TSADC_COMP0_INT	0x0030	W	0x00000000	TSADC high temperature level for source 0
TSADC_COMP1_INT	0x0034	W	0x00000000	TSADC high temperature level for source 1
TSADC_COMP0_SHUT	0x0040	W	0x00000000	TSADC high temperature level for source 0
TSADC_COMP1_SHUT	0x0044	W	0x00000000	TSADC high temperature level for source 1
TSADC_HIGHT_INT_DEBOUNCE	0x0060	W	0x00000003	high temperature debounce
TSADC_HIGHT_TSHUT_DEBOUNCE	0x0064	W	0x00000003	high temperature debounce
TSADC_AUTO_PERIOD	0x0068	W	0x00010000	TSADC auto access period
TSADC_AUTO_PERIOD_HT	0x006c	W	0x00010000	TSADC auto access period when temperature is high
TSADC_COMP0_LOW_INT	0x0080	W	0x00000000	TSADC low temperature level for source 0
TSADC_COMP1_LOW_INT	0x0084	W	0x00000000	TSADC low temperature level for source 1

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

18.4.2 Detail Register Description

TSADC_USER_CON

Address: Operational Base + offset (0x0000)

The control register of A/D Converter.

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12	RO	0x0	adc_status ADC status (EOC) 0: ADC stop 1: Conversion in progress

Bit	Attr	Reset Value	Description
11:6	RW	0x08	inter_pd_soc interleave between power down and start of conversion
5	RW	0x0	start When software write 1 to this bit , start_of_conversion will be assert. This bit will be cleared after TSADC access finishing. When TSADC_USER_CON[4] = 1'b1 take effect.
4	RW	0x0	start_mode start mode. 0: tsadc controller will asert start_of_conversion after "inter_pd_soc" cycles. 1: the start_of_conversion will be controlled by TSADC_USER_CON[5].
3	RW	0x1	adc_power_ctrl ADC power down control bit 0: ADC power down 1: ADC power up and reset
2:0	RW	0x0	adc_input_src_sel ADC input source selection(CH_SEL[2:0]). 000 : Input source 0 (SARADC_AIN[0]) 001 : Input source 1 (SARADC_AIN[1]) Others : Reserved

TSADC_AUTO_CON

Address: Operational Base + offset (0x0004)

TSADC auto mode control register

Bit	Attr	Reset Value	Description
31:26	RO	0x0	reserved
25	RW	0x0	last_tshut_2cru last_tshut_2cru for cru first/second reset TSHUT status. This bit will set to 1 when tshut is valid, and only be cleared when application write 1 to it. This bit will not be cleared by system reset.
24	RW	0x0	last_tshut_2gpio last_tshut_2gpio for hardware reset TSHUT status. This bit will set to 1 when tshut is valid, and only be cleared when application write 1 to it. This bit will not be cleared by system reset.
23:18	RO	0x0	reserved
17	RO	0x0	sample_dly_sel 0: AUTO_PERIOD is used 1: AUTO_PERIOD_HT is used

Bit	Attr	Reset Value	Description
16	RO	0x0	auto_status 0: auto mode stop; 1: auto mode in progress.
15:14	RO	0x0	reserved
13	RW	0x0	src1_lt_en 0: do not care low temperature of source 0 1: enable the low temperature monitor of source 0
12	RW	0x0	src0_lt_en 0: do not care low temperature of source 0 1: enable the low temperature monitor of source 0
11:9	RO	0x0	reserved
8	RW	0x0	tshut_prolarity 0: low active 1: high active
7:6	RO	0x0	reserved
5	RW	0x0	src1_en 0: do not care the temperature of source 1 1: if the temperature of source 0 is too high , TSHUT will be valid
4	RW	0x0	src0_en 0: do not care the temperature of source 0 1: if the temperature of source 0 is too high , TSHUT will be valid
3:2	RO	0x0	reserved
1	RW	0x0	tsadc_q_sel temperature coefficient 1'b0:use tsadc_q as output(positive temperature coefficient) 1'b1:use(1024 - tsadc_q) as output (negative temperature coefficient) RK3399 is negative temprature coefficient, so please set this bit as 1'b1
0	RW	0x0	auto_en 0: TSADC controller works at user-define mode 1: TSADC controller works at auto mode

TSADC_INT_EN
Address: Operational Base + offset (0x0008)

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16	RW	0x0	eoc_int_en eoc_Interrupt enable. eoc_interrupt enable in user defined mode 0: disable 1: enable
15:14	RO	0x0	reserved

Bit	Attr	Reset Value	Description
13	RW	0x0	lt_inten_src1 low temperature interrupt enable for src1 0: disable 1: enable
12	RW	0x0	lt_inten_src0 low temperature interrupt enable for src0 0: disable 1: enable
11:10	RO	0x0	reserved
9	RW	0x0	tshut_2cru_en_src1 0: TSHUT output to cru disabled. TSHUT output will always keep low . 1: TSHUT output works.
8	RW	0x0	tshut_2cru_en_src0 0: TSHUT output to cru disabled. TSHUT output will always keep low . 1: TSHUT output works.
7:6	RO	0x0	reserved
5	RW	0x0	tshut_2gpio_en_src1 0: TSHUT output to gpio disabled. TSHUT output will always keep low . 1: TSHUT output works.
4	RW	0x0	tshut_2gpio_en_src0 0: TSHUT output to gpio disabled. TSHUT output will always keep low . 1: TSHUT output works.
3:2	RO	0x0	reserved
1	RW	0x0	ht_inten_src1 high temperature interrupt enable for src1 0: disable 1: enable
0	RW	0x0	ht_inten_src0 high temperature interrupt enable for src0 0: disable 1: enable

TSADC_INT_PD
Address: Operational Base + offset (0x000c)

Bit	Attr	Reset Value	Description
31:17	RO	0x0	reserved
16	RW	0x0	eoc_int_pd Interrupt status. This bit will be set to 1 when end-of-conversion. Set 0 to clear the interrupt.

Bit	Attr	Reset Value	Description
15:14	RO	0x0	reserved
13	RW	0x0	lt_irq_src1 When TSADC output is lower than COMP_INT_LOW, this bit will be valid, which means temperature is low, and the application should in charge of this. write 1 to it , this bit will be cleared.
12	RW	0x0	lt_irq_src0 When TSADC output is lower than COMP_INT_LOW, this bit will be valid, which means temperature is low, and the application should in charge of this. write 1 to it , this bit will be cleared.
11:6	RO	0x0	reserved
5	RW	0x0	tshut_o_src1 TSHUT output status When TSADC output is bigger than COMP_SHUT, this bit will be valid, which means temperature is VERY high, and the application should in charge of this. write 1 to it , this bit will be cleared.
4	RW	0x0	tshut_o_src0 TSHUT output status When TSADC output is bigger than COMP_SHUT, this bit will be valid, which means temperature is VERY high, and the application should in charge of this. write 1 to it , this bit will be cleared.
3:2	RO	0x0	reserved
1	RW	0x0	ht_irq_src1 When TSADC output is bigger than COMP_INT, this bit will be valid, which means temperature is high, and the application should in charge of this. write 1 to it , this bit will be cleared.
0	RW	0x0	ht_irq_src0 When TSADC output is bigger than COMP_INT, this bit will be valid, which means temperature is high, and the application should in charge of this. write 1 to it , this bit will be cleared.

TSADC_DATA0

Address: Operational Base + offset (0x0020)

This register contains the data after A/D Conversion.

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RO	0x000	adc_data A/D value of the channel 0 last conversion (DOUT[9:0]).

TSADC_DATA1
Address: Operational Base + offset (0x0024)
This register contains the data after A/D Conversion.

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RO	0x000	adc_data A/D value of the channel 0 last conversion (DOUT[9:0]).

TSADC_COMP0_INT
Address: Operational Base + offset (0x0030)
TSADC high temperature level for source 0

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x000	tsadc_comp_src0 TSADC high temperature level. TSADC output is bigger than tsadc_comp, means the temperature is high. TSADC_INT will be valid.

TSADC_COMP1_INT
Address: Operational Base + offset (0x0034)
TSADC high temperature level for source 1

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x000	tsadc_comp_src1 TSADC high temperature level. TSADC output is bigger than tsadc_comp, means the temperature is high. TSADC_INT will be valid.

TSADC_COMP0_SHUT
Address: Operational Base + offset (0x0040)
TSADC high temperature level for source 0

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x000	tsadc_comp_src0 TSADC high temperature level. TSADC output is bigger than tsadc_comp, means the temperature is too high. TSHUT will be valid.

TSADC_COMP1_SHUT
Address: Operational Base + offset (0x0044)
TSADC high temperature level for source 1

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x000	tsadc_comp_src1 TSADC high temperature level. TSADC output is bigger than tsadc_comp, means the temperature is too high. TSHUT will be valid.

TSADC_HIGHT_INT_DEBOUNCE
Address: Operational Base + offset (0x0060)
high temperature debounce

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x03	debounce TSADC controller will only generate interrupt or TSHUT when temperature is higher than COMP_INT for "debounce" times.

TSADC_HIGHT_TSHUT_DEBOUNCE
Address: Operational Base + offset (0x0064)
high temperature debounce

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x03	debounce TSADC controller will only generate interrupt or TSHUT when temperature is higher than COMP_SHUT for "debounce" times.

TSADC_AUTO_PERIOD
Address: Operational Base + offset (0x0068)
TSADC auto access period

Bit	Attr	Reset Value	Description
31:0	RW	0x00010000	auto_period when auto mode is enabled, this register controls the interleave between every two accessing of TSADC.

TSADC_AUTO_PERIOD_HT
Address: Operational Base + offset (0x006c)
TSADC auto access period when temperature is high

Bit	Attr	Reset Value	Description
31:0	RW	0x00010000	auto_period This register controls the interleave between every two accessing of TSADC after the temperature is higher than COMP_SHUT or COMP_INT

TSADC_COMP0_LOW_INT
Address: Operational Base + offset (0x0080)
TSADC low temperature level for source 0

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x000	tsadc_comp_src0 TSADC low temperature level. TSADC output is lower than tsadc_comp, means the temperature is low. TSADC_LOW_INT will be valid.

TSADC_COMP1_LOW_INT
Address: Operational Base + offset (0x0084)
TSADC low temperature level for source 1

Bit	Attr	Reset Value	Description
31:12	RO	0x0	reserved
11:0	RW	0x000	tsadc_comp_src1 TSADC low temperature level. TSADC output is lower than tsadc_comp, means the temperature is low. TSADC_LOW_INT will be valid.

18.5 Application Notes

18.5.1 Channel Select

The system has oneTemperature Sensors, channel 0is for CPU.

18.5.2 Single-sample conversion

To saving power, the TS-ADC used single-sample conversion. The timing as flowing picture:

- Bypass mode(grf_sco_con1[1] = 1'b1)
  When the ADC bypass mode is enable(tsadc_dig_bypass = 1'b1), the ADC will cost 14 clock cycles to complete the conversion. The tsadc_dout will keep the valid data output unchanged untile the next clock cycles when the tsadc_sample is valid.

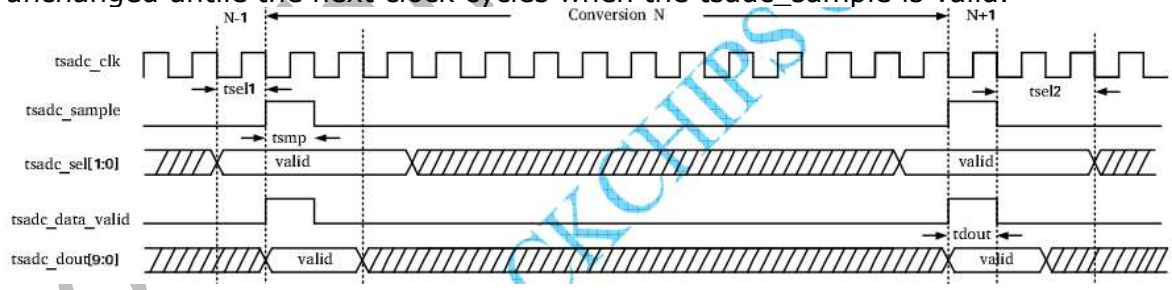


Fig. 18-2 tsadc timing diagram in bypass mode

- The Normal mode
  - Tsadc_clk_sel = 1'b0(grf_sco_con1[0] = 1'b0)
    The ADC will cost 15 clock cycles to complete the conversion.The tsadc_dout will keep the valid data output unchanged untile the next two clock cycles when the tsadc_sample is valid.

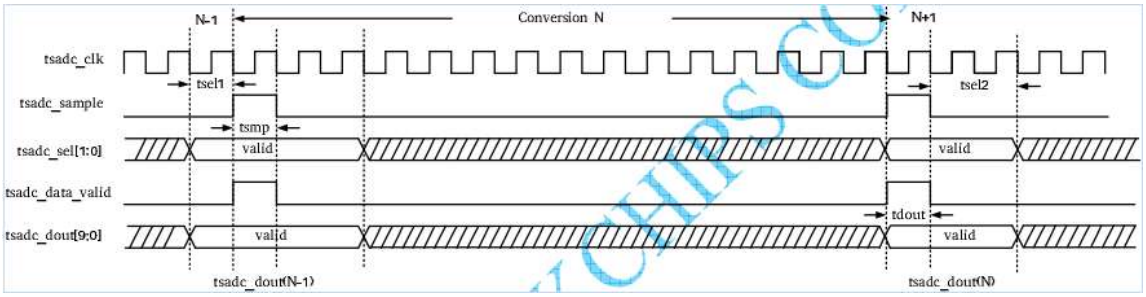


Fig. 18-3 tsadc timing diagram in normal mode with tsadc_clk_sel = 1'b0

- Tsadc_clk_sel = 1'b1(grf_sco_con1[0] = 1'b1)
  The ADC will cost 16 clock cycles to complete the conversion.The tsadc_dout will keep the valid data output unchanged untile the next three clock cycles when the tsadc_sample is valid.

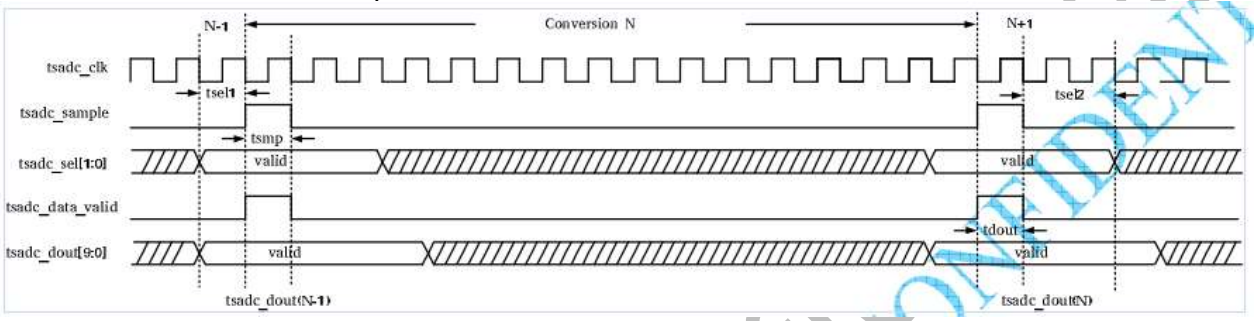


Fig. 18-4 tsadc timing diagram in normal mode with tsadc_clk_sel = 1'b1

18.5.3 Temperature-to-code mapping

Table 18-1 Temperature Code Mapping

Temperature/℃	ADC Output Data AUTO_CON[1] = 1'b0			ADC Output Data AUTO_CON[1] = 1'b1		
	Min	Typ	Max	Min	Typ	Max
-40	-	436	-	-	588	-
-35	-	431	-	-	593	-
-30	-	426	-	-	598	-
-25	-	421	-	-	603	-
-20	-	416	-	-	608	-
-15	-	411	-	-	613	-
-10	-	406	-	-	618	-
-5	-	401	-	-	623	-
0	-	395	-	-	629	-
5	-	390	-	-	634	-
10	-	385	-	-	639	-
15	-	380	-	-	644	-
20	-	375	-	-	649	-
25	-	370	-	-	654	-
30	-	364	-	-	660	-
35	-	359	-	-	665	-
40	-	354	-	-	670	-
45	-	349	-	-	675	-
50	-	343	-	-	681	-
55	-	338	-	-	686	-
60	-	333	-	-	691	-
65	-	328	-	-	696	-

Temperature/℃	ADC Output Data AUTO_CON[1] = 1'b0			ADC Output Data AUTO_CON[1] = 1'b1		
	Min	Typ	Max	Min	Typ	Max
70	-	322	-	-	702	-
75	-	317	-	-	707	-
80	-	312	-	-	712	-
85	-	307	-	-	717	-
90	-	301	-	-	723	-
95	-	296	-	-	728	-
100	-	291	-	-	733	-
105	-	286	-	-	738	-
110	-	280	-	-	744	-
115	-	275	-	-	749	-
120	-	270	-	-	754	-
125	-	264	-	-	760	-

Note:
Code to Temperature mapping of the Temperature sensor is a piece wise linear curve. Any temperature, code faling between to 2 give temperatures can be linearly interpolated.
Code to Temperature mapping should be updated based on sillcon results.

18.5.4 User-Define Mode

- In user-define mode, the PD_DVDD and CHSEL_DVDD are generate by setting register TSADC_USER_CON, bit[3] and bit[2:0]. In order to ensure timing between PD_DVDD and CHSEL_DVDD, the CHSEL_DVDD must be set before the PD_DVDD.
- In user-define mode, you can choose the method to control the START_OF_CONVERSION by setting bit[4] of TSADC_USER_CON. If set to 0, the start_of_conversion will be assert after "inter_pd_soc" cycles, which could be set by bit[11:6] of TSADC_USER_CON. And if start_mode was set 1, the start_of_conversion will be controlled by bit[5] of TSADC_USER_CON.
- Software can get the four channel temperature from TSADC_DATAn (n=0,1,2,3).

18.5.5 Automatic Mode

You can use the automatic mode with the following step:

- Set TSADC_AUTO_PERIOD，configure the interleave between every two accessing of TSADC in normal operation.
- Set TSADC_AUTO_PERIOD_HT. configure the interleave between every two accessing of TSADC after the temperature is higher than COMP_SHUT or COMP_INT.
- Set TSADC_COMPn_INT(n=0,1), configure the high temperature level, if tsadc output is smaller than the value, means the temperature is high, tsadc_int will be asserted.
- Set TSADC_COMPn_SHUT(n=0,1), configure the super high temperature level, if tsadc output is smaller than the value, means the temperature is too high, TSHUT will be asserted.
- Set TSADC_INT_EN, you can enable the high temperature interrupt for all channel; and you can also set TSHUT output to gpio to reset the whole chip; and you can set TSHUT output to cru to reset the whole chip.
- Set TSADC_HIGHT_INT_DEBOUNCE and TSADC_HIGHT_TSHUT_DEBOUNCE, if the temperature is higher than COMP_INT or COMP_SHUT for "debounce" times, TSADC controller will generate interrupt or TSHUT.
- Set TSADC_AUTO_CON, enable the TSADC controller.

Chapter 19 Debug

19

19.1 Overview

The RK3399 uses the Coresight-SOC Technology to support real-time debug access and trace for the multi-core. Software can access debug components and control of debug behavior through a DAP (Debug Access Port). A standard infrastructure is implemented for the capture and transmission of trace data, combination of multiple data streams by funneling together, and then output of data to a trace port. The cross-triggering components are also implemented in RK3399 for debug component broadcast events to each other.

19.1.1 Feature

- Access to debug features and on-chip AHB, APB, and JTAG buses through a JTAG or Single Wire Debug (SWD) interface.
- Merging of multiple trace sources into a single trace stream.
- Capture of trace streams on-chip or off-chip.
- Cross-triggering between different debug and trace components.
- Support Timestamp generation.

19.1.2 Debug components address map

The following table shows the debug components address in memory map, the DEBUG system base address is 0xfe400000:

Module	Offset	Size
DAP_ROM	0x000000	4KB
Trace Funnel	0x001000	4KB
CTI_TPIU	0x003000	4KB
Timestamp	0x004000	4KB
TPIU	0x005000	4KB
CLUSTERL_ROM	0x020000	4KB
CLUSTERL_DBG0	0x030000	4KB
CLUSTERL_PMU0	0x031000	4KB
CLUSTERL_DBG1	0x032000	4KB
CLUSTERL_PMU1	0x033000	4KB
CLUSTERL_DBG2	0x034000	4KB
CLUSTERL_PMU2	0x035000	4KB
CLUSTERL_DBG3	0x036000	4KB
CLUSTERL_PMU3	0x037000	4KB
CLUSTERL_CTI0	0x038000	4KB
CLUSTERL_CTI1	0x039000	4KB
CLUSTERL_CTI2	0x03A000	4KB
CLUSTERL_CTI3	0x03B000	4KB
CLUSTERL_ETM0	0x03C000	4KB
CLUSTERL_ETM1	0x03D000	4KB
CLUSTERL_ETM2	0x03E000	4KB
CLUSTERL_ETM3	0x03F000	4KB
CLUSTERB_ROM	0x200000	64KB
CLUSTERB_DBG0	0x210000	64KB
CLUSTERB_CTI0	0x220000	64KB
CLUSTERB_PMU0	0x230000	64KB
CLUSTERB_ETM0	0x240000	64KB
CLUSTERB_DEBUG1	0x310000	64KB
CLUSTERB_CTI1	0x320000	64KB
CLUSTERB_PMU1	0x330000	64KB

Module	Offset	Size
CLUSTERB_ETM1	0x340000	64KB

19.2 Block Diagram

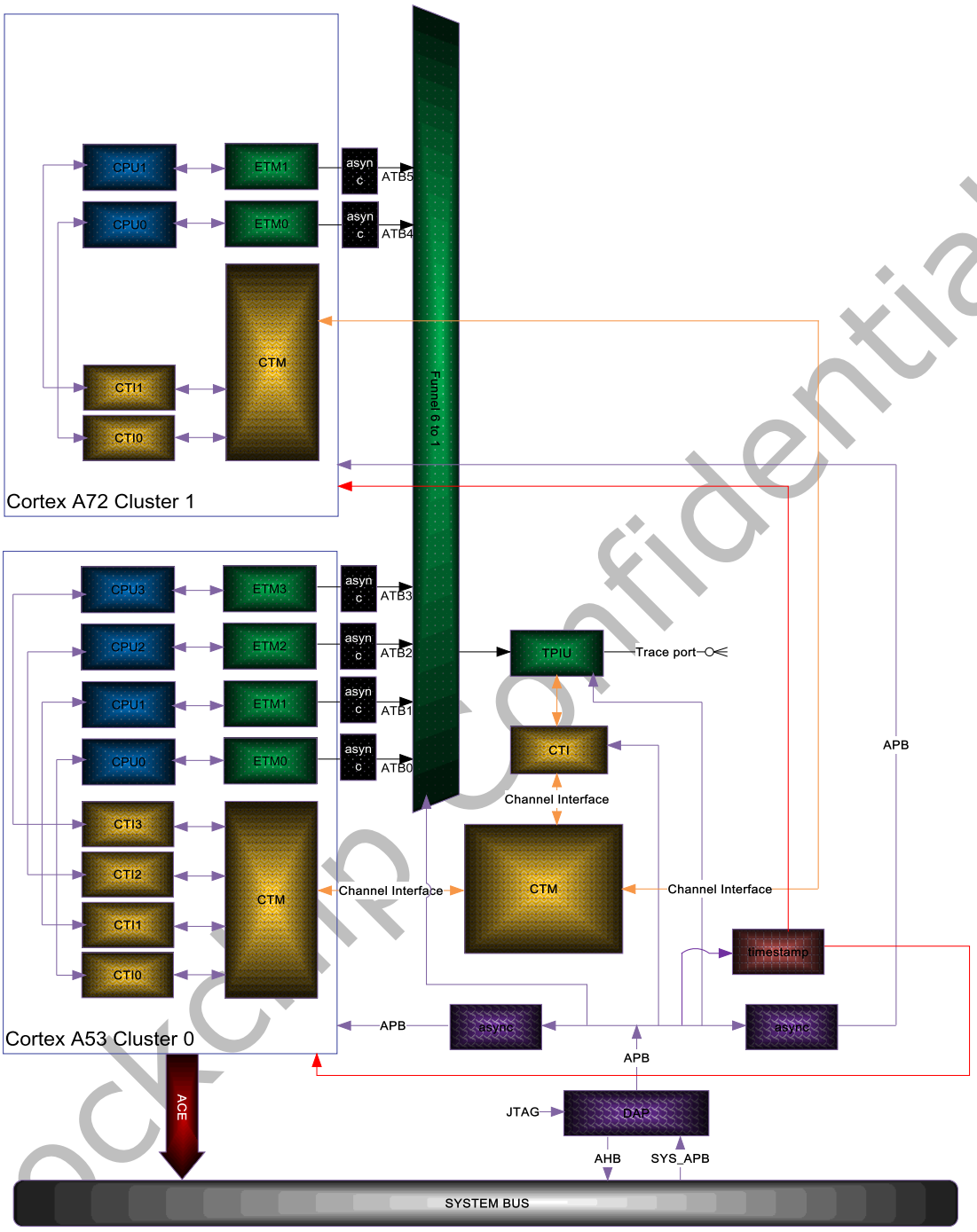


Fig. 19-1 RK3399 Debug system structure

The RK3399 DEBUG system is designed for a dual-cluster processor system, as shown in figure above. Cluster 0 is a four-core Cortex-A53, and cluster 1 is a dual-core Cortex-A72. The JTAG/SW controller can access all debug system components and system memory through DAP which is a package of APs(access port).

The data flow of trace can be linked together through a “trace funnel component” and be sent to IO by a TPIU component.

ECT (embedded cross trigger) is supported by CTM/CTIs in DEBUG system, CTM/CTIs in the Cortex-A53 cluster and CTM/CTIs in the Cortex-A72 cluster. And a timestamp generator in the DEBUG system can generate a 64bit binary count and be shared and synchronized to the two clusters by asynchronous bridges.

19.3 Function Description

19.3.1 DAP (Debug Access Port)

DAP in RK3399 is designed base on ARM coresight400 technology, which do not provide a "universal" DAP component as the previous version. So the real DAP in RK3399 is consist of a group of coresight400 components which are integrated by ourselves.
The RK3399 DAP architecture is illustrated in figure 6-2, and be described in the following sections.

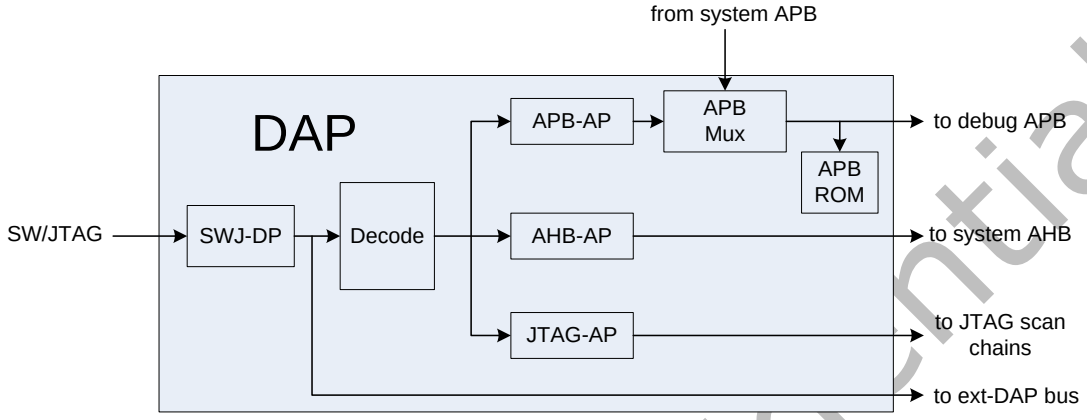


Fig. 19-2 RK3399 Debug system DAP structure

- **SWJ-DP:**

The SWJ-DP is a combined JTAG-DP and SW-DP that enables you to connect either an SWD or JTAG probe to a target. It is the standard CoreSight debug port, and enables access either to the JTAG-DP or SW-DP blocks. To make efficient use of package pins, serial wire shares, or overlays, the JTAG pins use an auto-detect mechanism that switches between JTAG-DP and SW-DP depending on which probe is connected. A special sequence on the swdiotms pin switches between JTAG-DP and SW-DP.
The SWJ-DP consists of a wrapper around the JTAG-DP and SW-DP. It selects JTAG or SWD as the connection mechanism and enables either JTAG-DP or SW-DP as the interface to the DAP. Figure 6-3 shows the structure of the SWJ-DP.

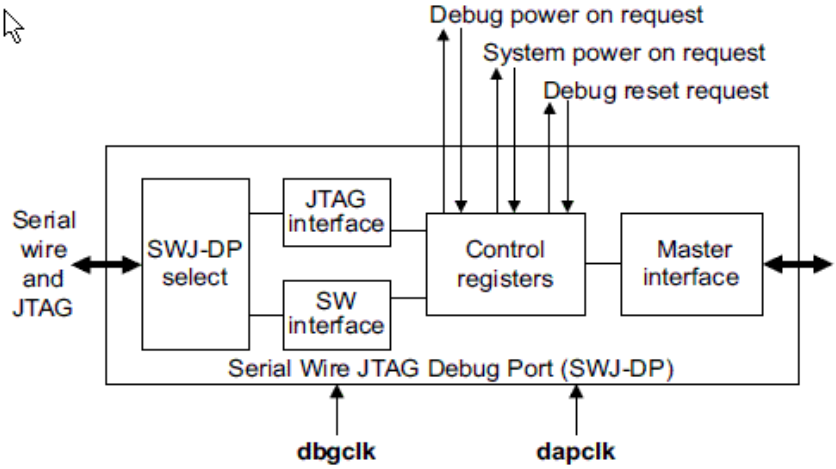


Fig. 19-3 RK3399 SWJ-DP structure

When operating as a JTAG-DP this follows the JTAG-DP as defined in the ARM Debug interface Architecture Specification, ADIv5.0 to ADIv5.2. It also contains an explanation of its programmer model, capabilities, and features.
The JTAG-DP contains a debug port state machine that controls the JTAG-DP mode operation, including controlling the scan chain interface that provides the external physical interface to the JTAG-DP. It is based closely on the JTAG TAP State Machine. See IEEE std 1149.1-2001.
When operating as an SW-DP Interface, this implementation is taken from the ARM debug Interface Architecture Specification, ADIv5.0 to ADIv5.2, and operates with a synchronous serial interface. This uses a single bidirectional data signal and a clock signal.
The SW-DP provides a low pin count, bidirectional serial connection to the DAP with a

reference clock signal from synchronous operation.
Communications with the SW-DP use a 3-phase protocol:

- A host-to-target packet request
- A target-to-host acknowledge response
- A data transfer phase, if required. This can be target-to-host or host-to-target, depending on the request made in the first phase.

- **DAPBUSIC:**

The DAPBUS interconnect is a combinational component for connecting the DP to the APs which are AHB-AP and APB-AP in RK3399.
To address a particular AP, the DP uses the eight MSBs of its address bus, dapcaddrs[15:0]. The value driven on these address lines is determined by the APSEL[7:0] field in the AP Select register.

- **AHB-AP:**

The AHB-AP implements the MEM-AP architecture to directly connect to an AHB-based memory system. Connection to other memory systems is possible through suitable bridging.

- **APB-AP:**

The APB-AP implements the MEM-AP architecture to connect directly to an APB based system. This bus is normally dedicated to CoreSight and other debug components.

- **APBIC:**

The APB interconnect connects one or more APB bus masters, for example an APB-AP and an APB interface driven by an on-chip processor. APB interconnects can be cascaded. The RK3399 APBIC implements a ROM table at address 0x00000000, which identifies the locations of the CoreSight compoents accessed through it.

19.3.2 ETM (Embedded Trace Macro)

There are eight ETMs in the RK3399 along with Cortex-A53 processor and Cortex-A72 processor separately in little and big clusters. The ETM trace unit is a module that performs real-time instruction flow tracing based on the Embedded Trace Macrocell(ETM), architecture ETMv4. ETM is a CoreSight component, and is an integral part of the ARM Real-time Debug solution, DS-5 Development Studio.
The figure 6-4 shows the main function blocks of the ETM trace unit.

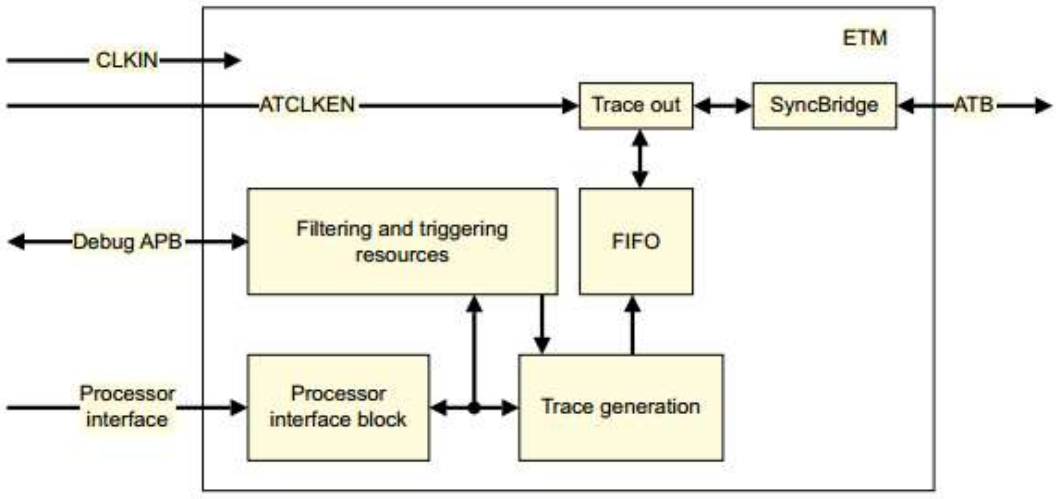


Fig. 19-4 RK3399 ETM structure

19.3.3 Trace funnel

The ATB funnel component merges multiple ATB buses into a single ATB buses into a single ATB bus. If the optional APB interface is implemented, a debugger can also control the arbitration scheme and selectively enable the ATB slave interfaces for tracing.
The following figure shows ATB funnel block architecture.

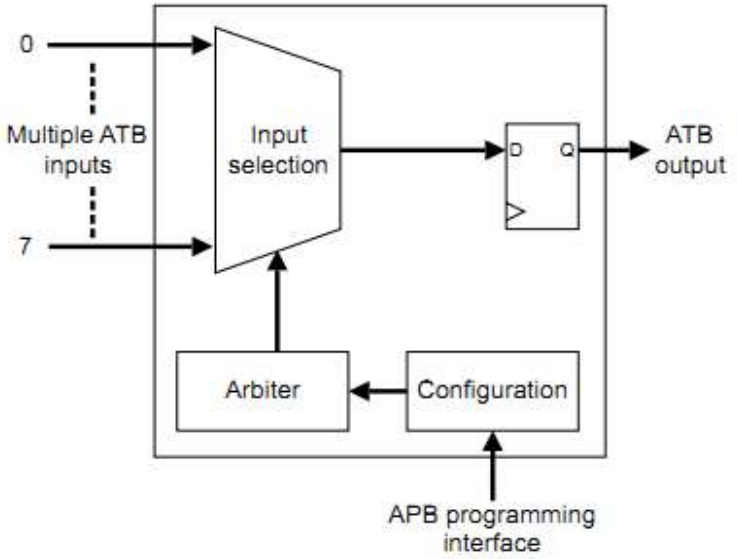


Fig. 19-5 Trace funnel architecture

19.3.4 TPIU

The TPIU acts as a bridge between the on-chip trace data, with separate IDs, to a data stream, encapsulating IDs where required, that is then captured by a Trace Port Analyzer (TPA). Fig. 6-6 shows the main blocks of the TPIU and the clock domains.

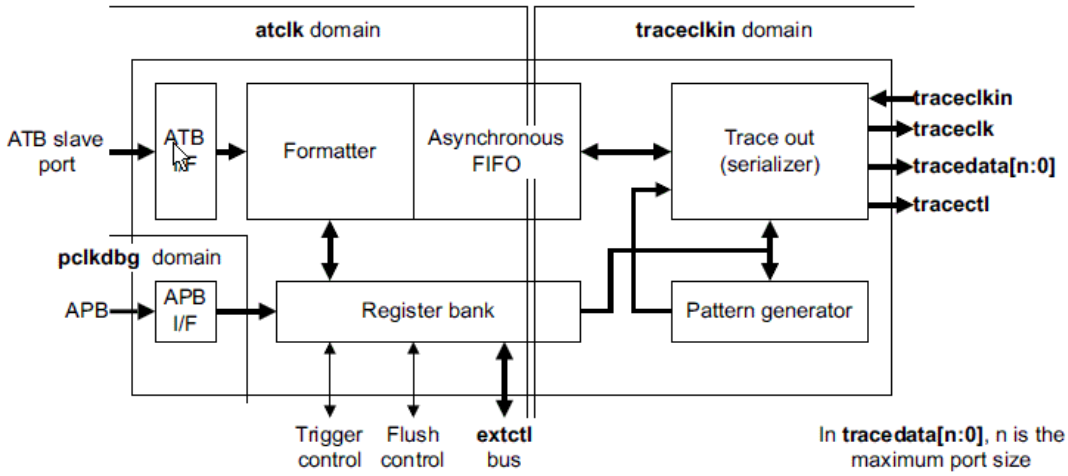


Fig. 19-6 RK3399 TPIU structure

The TPIU contains the following components:

- Formatter
  Inserts source ID signals into the data packet stream so that trace data can be re-associated with its trace source. See TPIU formatter and FIFO.
- Asynchronous FIFO
  Enables trace data to be driven out at a speed that is not dependent on the on-chip bus clock.
- Register bank
  Contains the management, control and status registers for triggers, flushing behavior and external control.
- Trace out
  The trace out block serializes formatted data before it goes off-chip.
- Pattern Generator
  The pattern generator unit provides a simple set of defined bit sequences or patterns that can be output over the Trace Port and be detected by the TPA or other associated Trace Capture Device (TCD). The TCD can use these patterns to indicate if it is possible to increase or to decrease the trace port clock speed.
- ATB interface

The TPIU accepts trace data from a trace source, either direct from a trace source or using a Trace Funnel.

- APB interface
  The APB interface is the programming interface for the TPIU.

Software must consider the following when programming the TPIU registers for trace capture:

- TPAs that are only capable of operation with tracectl must only use the formatter in either bypass or normal mode, not in continuous mode.
- ARM recommends that following a trigger event within a multi-trace source configuration, a flush is performed to ensure that all historical information related to the trigger is output.
- If flush on trigger event and stop on trigger event options are chosen then any data after the trigger is not captured by the TPA. When the TPIU is instructed to stop, it discards any subsequent trace data, including data returned by the flush. Select Stop on Flush completion instead.
- Although multiple flushes can be scheduled using flush on trigger event, flush on flushin, and manual flush, when one of these requests are made, it masks additional requests of the same type. This means repeated writing to the manual flush bit does not schedule multiple manual requests unless each is permitted to complete first.
- Unless multiple triggers are required, it is not advisable to set both trigger event and trigger on flush completion, if flush on trigger event is also enabled. In addition, if trigger on trigin is enabled with this configuration, it can also cause multiple trigger markers groom on trigger request.

19.3.5 ECT (CTI & CTM)

The ECT for CoreSight consists of a number of CTIs and CTMs connected together. This enables ARM/ETM subsystems to interact. That is cross trigger, with each other. The debug system enables debug support for multiple cores, together with cross triggering between the cores and their respective ETMs.

The main function of the ECT (CTI and CTM) is to pass debug events from one core to another. For example, the ECT can communicate debug state information from one core to another, so that program execution on both processors can be stopped at the same time if required.

- CTI (Cross Trigger Interface)
  The CTI combines and maps the trigger requests, and broadcasts them to all other interfaces on the ECT as channel events. When the CTI receives a channel event it maps this onto a trigger output. This enables subsystems to cross trigger with each other. The receiving and transmitting of triggers is performed through the trigger interface.
- CTM (Cross Trigger Matrix)
  This block controls the distribution of channel events. It provides Channel Interfaces (CIs) for connection to either CTIs or CTMs. This enables multiple CTIs to be linked together.

19.3.6 Timestamp

The timestamp components generate and distribute a consistent time value to multiple processors in RK3399.

The timestamp system is shown in the following figure:

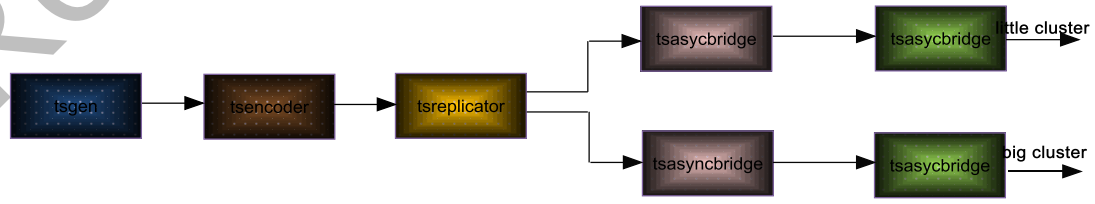


Fig. 19-7 RK3399 Timestamp structure

The timestamp interconnect provides a mechanism for efficiently distributing a timestamp value across a potentially large system in a way that is cost-effective to implement. It has the following features:

- Uses a master timing reference with a fixed frequency of typically 10-50 MHz
- Time always counts forward
- Time available as a natural binary number to software

- Writeable and readable count value
- Distributed synchronization of timestamp
- Time value presented as a 64-bit binary count.

The interconnect ensures that any components that uses the distributed timestamp are synchronized to the distributed count value with minimal skew while the timestamp interconnect is clocked.

The CoreSight timestamp generator can be used in one of the following ways:

- To generate the time reported by ARM processors that implements the Generic Timer specification. Software expects that this time does not count backwards, and so it is important that only secure software can change the timestamp value. The programmer's model of the timestamp generator has been designed to enable non-secure software to read the timestamp value while only permitting secure software to change the timestamp value.
- To generate the time used to align traces and other debug information in the CoreSight system. The timestamp generator is controlled by debug software and connected to the debug APB interconnects. The read-only interface is not used.

19.4 Register Description

For details of DEBUG system components (such as DAP, FUNNEL, TPIU, TIMESTAMP and CTI) registers, please reference ARM document "DDI0480F_soc_r3p1_trm" chapter 3.
For details of debug components inside Cortex-A53 cluster (such as ETM and CA53 CTI), please reference ARM document "DDI0500C_cortex_a53_r0p4_trm" chapter 11. And for Cortex-A72 cluster, please reference ARM document "ARM_Cortex-A72_MPCore_Technical_Reference_Manual_r0p1-00eac0" chapter 12, 13.

19.5 Interface description

19.5.1 DAP SWJ-DP interface

The following figure is the DAP SWJ-DP interface, the SWJ-DP is a combined JTAG-DP and SW-DP that enable you connect either a Serial Write Debug(SWJ) to JTAG probe to a target.

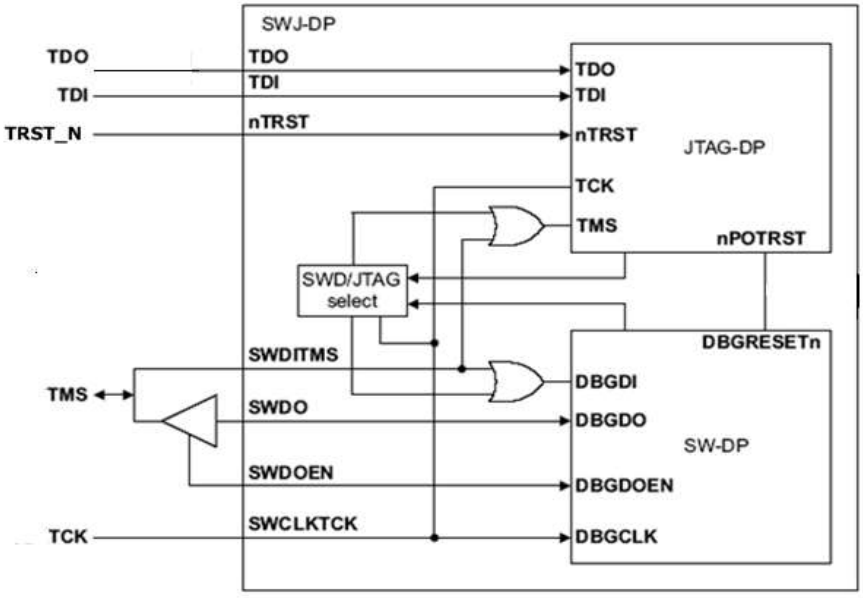


Fig. 19-8 DAP SWJ interface

Table 19-1 SWJ interface

Module Pin	Direction	PAD Name	IOMUX Setting
TCK	I	IO_SDMMCdata2_CXCSJTAGtck_ HDCPJTAGtdi_SDMMCgpio4b2	grf_gpio4b_sel[5:4]= 0x2
TMS	IO	IO_SDMMCdata3_CXCSJTAGtms_ HDCPJTAGtdo_SDMMCgpio4b3	grf_gpio4b_sel[7:6]= 0x2

19.5.2 TPIU trace port interface

Table 19-2 TPIU interface

Module Pin	Direction	PAD Name	IOMUX Setting
trace_data[0]	O	IO_I2S0sclk_TRACEdata0_A72CORE0wfi_AUDIOgpio3d0	grf_gpio3d_sel[1:0] = 0x2
trace_data[1]	O	IO_I2S0lrckrx_TRACEdata1_A72CORE1wfi_AUDIOgpio3d1	grf_gpio3d_sel[3:2] = 0x2
trace_data[2]	O	IO_I2S0lrcktx_TRACEdata2_A53CORE0wfi_AUDIOgpio3d2	grf_gpio3d_sel[5:4] = 0x2
trace_data[3]	O	IO_I2S0sdi0_TRACEdata3_A53CORE1wfi_AUDIOgpio3d3	grf_gpio3d_sel[7:6] = 0x2
trace_data[4]	O	IO_I2S0sdi1sdo3_TRACEdata4_A53CORE2wfi_AUDIOgpio3d4	grf_gpio3d_sel[9:8] = 0x2
trace_data[5]	O	IO_I2S0sdi2sdo2_TRACEdata5_A53CORE3wfi_AUDIOgpio3d5	grf_gpio3d_sel[11:10] = 0x2
trace_data[6]	O	IO_I2S0sdi3sdo1_TRACEdata6_A72L2wfi_AUDIOgpio3d6	grf_gpio3d_sel[13:12] = 0x2
trace_data[7]	O	IO_I2S0sdo0_TRACEdata7_A53L2wfi_AUDIOgpio3d7	grf_gpio3d_sel[15:14] = 0x2
trace_data[8]	O	IO_I2C1AUDIOCAMscl_TRACEdata8_AUDIOgpio4a2	grf_gpio4a_sel[5:4] = 0x2
trace_data[9]	O	IO_I2S1sclk_TRACEdata9_AUDIOgpio4a3	grf_gpio4a_sel[7:6] = 0x2
trace_data[10]	O	IO_I2S1lrckrx_TRACEdata10_AUDIOgpio4a4	grf_gpio4a_sel[9:8] = 0x2
trace_data[11]	O	IO_I2S1lrcktx_TRACEdata11_AUDIOgpio4a5	grf_gpio4a_sel[11:10] = 0x2
trace_data[12]	O	IO_MACtxd2_SPI4EXPrxd_TRACEdata12_GMACgpio3a0	grf_gpio3a_sel[1:0] = 0x3
trace_data[13]	O	IO_MACtxd3_SPI4EXPtxd_TRACEdata13_GMACgpio3a1	grf_gpio3a_sel[3:2] = 0x3
trace_data[14]	O	IO_MACrxd2_SPI4EXPclk_TRACEdata14_GMACgpio3a2	grf_gpio3a_sel[5:4] = 0x3
trace_data[15]	O	IO_MACrxd3_SPI4EXPcsn0_TRACEdata15_GMACgpio3a3	grf_gpio3a_sel[7:6] = 0x3
trace_clk	O	IO_I2C1AUDIOCAMsda_TRACEclk_AUDIOgpio4a1	grf_gpio4a_sel[3:2] = 0x2
trace_ctl	O	IO_I2Sclk_TRACEctl_LPM0wfi_AUDIOgpio4a0	grf_gpio4a_sel[1:0] = 0x2

Chapter 20 Mailbox

20.1 Overview

The Mailbox module is a simple APB peripheral that allows both the Cortex-A53/Cortex-A72 and Cortex-M0 system to communicate by writing operation to generate interrupt. The registers are accessible by both CPU via APB interface.

The Mailbox has the following main features:

- Support dual-core system: Cortex-A53/Cortex-A72 and Cortex-M0
- Support APB interface
- Support four mailbox elements, each element includes one data word, one command word register and one flag bit that can represent one interrupt
- Four interrupts to Cortex-A53/Cortex-A72
- Four interrupts to Cortex-M0
- Provide 32 lock registers for software to use to indicate whether mailbox is occupied

20.2 Block Diagram

The figure below shows Mailbox block diagram:

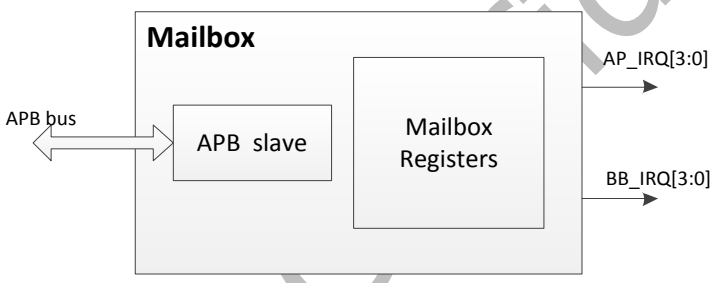


Fig. 20-1 Mailbox Block Diagram

20.3 Function Description

20.3.1 Interrupt to Cortex-A53/ Cortex-A72

The interrupt to Cortex-A53/ Cortex-A72 (CA53/72_IRQ[i] , i=0~3) is generated when B2A_INTEN[i] equals to 1 and there are writing operation to B2A_CMD_i and B2A_DATA_i orderly.(i=0~3)
The interrupt to Cortex-A53/ Cortex-A72 (CA53/72_IRQ[i], i=0~3) is cleared when writing 1 to B2A_STATUS[i]. (i=0~3)

20.3.2 1.3.2 Interrupt to Cortex-M0

The interrupt to Cortex-M0 (MCU_IRQ[i]) is generated when A2B_INTEN[i] equals to 1 and there are writing operation to A2B_CMD_i and A2B_DATA_i orderly.(i=0~3)
The interrupt to Cortex-M0 (MCU_IRQ[i],i=0~3) is cleared when writing 1 to A2B_STATUS[i]. (i=0~3).
There are two Cortex-M0s (perilp Cortex-M0 and PMU Cortex-M0), so there are two independent mail box(mailbox0 for PERILP and mailbox1 for PMU) for each.

20.4 Register Description

20.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
MAILBOX_A2B_INTEN	0x00000	W	0x00000000	Cortex-A53/Cortex-A72 to Cortex-M0 interrupt enable register

Name	Offset	Size	Reset Value	Description
MAILBOX_A2B_STATUS	0x00004	W	0x00000000	Cortex-A53/Cortex-A72 to Cortex-M0 interrupt status register
MAILBOX_A2B_CMD_0	0x00008	W	0x00000000	Cortex-A53/Cortex-A72 to Cortex-M0 command 0
MAILBOX_A2B_DAT_0	0x0000c	W	0x00000000	Cortex-A53/Cortex-A72 to Cortex-M0 data 0
MAILBOX_A2B_CMD_1	0x00010	W	0x00000000	Cortex-A53/Cortex-A72 to Cortex-M0 command 1
MAILBOX_A2B_DAT_1	0x00014	W	0x00000000	Cortex-A53/Cortex-A72 to Cortex-M0 data 1
MAILBOX_A2B_CMD_2	0x00018	W	0x00000000	Cortex-A53/Cortex-A72 to Cortex-M0 command 2
MAILBOX_A2B_DAT_2	0x0001c	W	0x00000000	Cortex-A53/Cortex-A72 to Cortex-M0 data 2
MAILBOX_A2B_CMD_3	0x00020	W	0x00000000	Cortex-A53/Cortex-A72 to Cortex-M0 command 3
MAILBOX_A2B_DAT_3	0x00024	W	0x00000000	Cortex-A53/Cortex-A72 to Cortex-M0 data 3
MAILBOX_B2A_INTEN	0x00028	W	0x00000000	Cortex-A53/Cortex-A72 to Cortex-M0 interrupt enable register
MAILBOX_B2A_STATUS	0x0002c	W	0x00000000	Cortex-M0 to Cortex-A53/Cortex-A72 interrupt status register
MAILBOX_B2A_CMD_0	0x00030	W	0x00000000	Cortex-M0 to Cortex-A53/Cortex-A72 command 0
MAILBOX_B2A_DAT_0	0x00034	W	0x00000000	Cortex-M0 to Cortex-A53/Cortex-A72 data 0
MAILBOX_B2A_CMD_1	0x00038	W	0x00000000	Cortex-M0 to Cortex-A53/Cortex-A72 command 1
MAILBOX_B2A_DAT_1	0x0003c	W	0x00000000	Cortex-M0 to Cortex-A53/Cortex-A72 data 1
MAILBOX_B2A_CMD_2	0x00040	W	0x00000000	Cortex-M0 to Cortex-A53/Cortex-A72 command 2
MAILBOX_B2A_DAT_2	0x00044	W	0x00000000	Cortex-M0 to Cortex-A53/Cortex-A72 data 2
MAILBOX_B2A_CMD_3	0x00048	W	0x00000000	Cortex-M0 to Cortex-A53/Cortex-A72 command 3
MAILBOX_B2A_DAT_3	0x0004c	W	0x00000000	Cortex-M0 to Cortex-A53/Cortex-A72 data 3
MAILBOX_ATOMIC_LOCK_00	0x00100	W	0x00000000	Lock flag register 00
MAILBOX_ATOMIC_LOCK_01	0x00104	W	0x00000000	Lock flag register 01
MAILBOX_ATOMIC_LOCK_02	0x00108	W	0x00000000	Lock flag register 02

Name	Offset	Size	Reset Value	Description
MAILBOX_ATOMIC_LOCK_03	0x0010c	W	0x00000000	Lock flag register 03
MAILBOX_ATOMIC_LOCK_04	0x00110	W	0x00000000	Lock flag register 04
MAILBOX_ATOMIC_LOCK_05	0x00114	W	0x00000000	Lock flag register 05
MAILBOX_ATOMIC_LOCK_06	0x00118	W	0x00000000	Lock flag register 06
MAILBOX_ATOMIC_LOCK_07	0x0011c	W	0x00000000	Lock flag register 07
MAILBOX_ATOMIC_LOCK_08	0x00120	W	0x00000000	Lock flag register 08
MAILBOX_ATOMIC_LOCK_09	0x00124	W	0x00000000	Lock flag register 09
MAILBOX_ATOMIC_LOCK_10	0x00128	W	0x00000000	Lock flag register 10
MAILBOX_ATOMIC_LOCK_11	0x0012c	W	0x00000000	Lock flag register 11
MAILBOX_ATOMIC_LOCK_12	0x00130	W	0x00000000	Lock flag register 12
MAILBOX_ATOMIC_LOCK_13	0x00134	W	0x00000000	Lock flag register 13
MAILBOX_ATOMIC_LOCK_14	0x00138	W	0x00000000	Lock flag register 14
MAILBOX_ATOMIC_LOCK_15	0x0013c	W	0x00000000	Lock flag register 15
MAILBOX_ATOMIC_LOCK_16	0x00140	W	0x00000000	Lock flag register 16
MAILBOX_ATOMIC_LOCK_17	0x00144	W	0x00000000	Lock flag register 17
MAILBOX_ATOMIC_LOCK_18	0x00148	W	0x00000000	Lock flag register 18
MAILBOX_ATOMIC_LOCK_19	0x0014c	W	0x00000000	Lock flag register 19
MAILBOX_ATOMIC_LOCK_20	0x00150	W	0x00000000	Lock flag register 20
MAILBOX_ATOMIC_LOCK_21	0x00154	W	0x00000000	Lock flag register 21
MAILBOX_ATOMIC_LOCK_22	0x00158	W	0x00000000	Lock flag register 22
MAILBOX_ATOMIC_LOCK_23	0x0015c	W	0x00000000	Lock flag register 23
MAILBOX_ATOMIC_LOCK_24	0x00160	W	0x00000000	Lock flag register 24

Name	Offset	Size	Reset Value	Description
MAILBOX_ATOMIC_LOCK_25	0x00164	W	0x00000000	Lock flag register 25
MAILBOX_ATOMIC_LOCK_26	0x00168	W	0x00000000	Lock flag register 26
MAILBOX_ATOMIC_LOCK_27	0x0016c	W	0x00000000	Lock flag register 27
MAILBOX_ATOMIC_LOCK_28	0x00170	W	0x00000000	Lock flag register 28
MAILBOX_ATOMIC_LOCK_29	0x00174	W	0x00000000	Lock flag register 29
MAILBOX_ATOMIC_LOCK_30	0x00178	W	0x00000000	Lock flag register 30
MAILBOX_ATOMIC_LOCK_31	0x0017c	W	0x00000000	Lock flag register 31

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

20.4.2 Detail Register Description

MAILBOX_A2B_INTEN
Address: Operational Base + offset (0x00000)
Cortex-A53/Cortex-A72 to MCU interrupt enable register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	RW	0x0	int3 interrupt enable for int3
2	RW	0x0	int2 interrupt enable for int2
1	RW	0x0	int1 interrupt enable for int1
0	RW	0x0	int0 interrupt enable for int0

MAILBOX_A2B_STATUS
Address: Operational Base + offset (0x00004)
Cortex-A53/Cortex-A72 to MCU interrupt status register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	RW	0x0	int3 interrupt status for int3. when writte 1, int is cleared.
2	RW	0x0	int2 interrupt status for int2. when writte 1, int is cleared.

Bit	Attr	Reset Value	Description
1	RW	0x0	int1 interrupt status for int1. when writte 1, int is cleared.
0	RW	0x0	int0 interrupt status for int0. when writte 1, int is cleared.

MAILBOX_A2B_CMD_0
Address: Operational Base + offset (0x00008)
Cortex-A53/Cortex-A72 to MCU command 0

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	command command of Cortex-A53/Cortex-A72 to Cortex-M0

MAILBOX_A2B_DAT_0
Address: Operational Base + offset (0x0000c)
Cortex-A53/Cortex-A72 to MCU data 0

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	data data of Cortex-A53/Cortex-A72 to Cortex-M0

MAILBOX_A2B_CMD_1
Address: Operational Base + offset (0x00010)
Cortex-A53/Cortex-A72 to MCU command 1

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	command command of Cortex-A53/Cortex-A72 to Cortex-M0

MAILBOX_A2B_DAT_1
Address: Operational Base + offset (0x00014)
Cortex-A53/Cortex-A72 to MCU data 1

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	data data of Cortex-A53/Cortex-A72 to Cortex-M0

MAILBOX_A2B_CMD_2
Address: Operational Base + offset (0x00018)
Cortex-A53/Cortex-A72 to MCU command 2

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	command command of Cortex-A53/Cortex-A72 to Cortex-M0

MAILBOX_A2B_DAT_2
Address: Operational Base + offset (0x0001c)
Cortex-A53/Cortex-A72 to MCU data 2

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	data data of Cortex-A53/Cortex-A72 to Cortex-M0

MAILBOX_A2B_CMD_3
Address: Operational Base + offset (0x00020)
Cortex-A53/Cortex-A72 to MCU command 3

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	command command of Cortex-A53/Cortex-A72 to Cortex-M0

MAILBOX_A2B_DAT_3
Address: Operational Base + offset (0x00024)
Cortex-A53/Cortex-A72 to MCU data 3

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	data data of Cortex-A53/Cortex-A72 to Cortex-M0

MAILBOX_B2A_INTEN
Address: Operational Base + offset (0x00028)
Cortex-A53/Cortex-A72 to MCU interrupt enable register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	RW	0x0	int3 interrupt enable for int3
2	RW	0x0	int2 interrupt enable for int2
1	RW	0x0	int1 interrupt enable for int1
0	RW	0x0	int0 interrupt enable for int0

MAILBOX_B2A_STATUS
Address: Operational Base + offset (0x0002c)
MCU to Cortex-A53/Cortex-A72 interrupt status register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	RW	0x0	int3 interrupt status for int3. when writte 1, int is cleared.

Bit	Attr	Reset Value	Description
2	RW	0x0	int2 interrupt status for int2. when writte 1, int is cleared.
1	RW	0x0	int1 interrupt status for int1. when writte 1, int is cleared.
0	RW	0x0	int0 interrupt status for int0. when writte 1, int is cleared.

MAILBOX_B2A_CMD_0
Address: Operational Base + offset (0x00030)
MCU to Cortex-A53/Cortex-A72 command 0

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	command command of MCU to Cortex-A53/Cortex-A72

MAILBOX_B2A_DAT_0
Address: Operational Base + offset (0x00034)
MCU to Cortex-A53/Cortex-A72 data 0

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	data data of MCU to Cortex-A53/Cortex-A72

MAILBOX_B2A_CMD_1
Address: Operational Base + offset (0x00038)
MCU to Cortex-A53/Cortex-A72 command 1

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	command command of MCU to Cortex-A53/Cortex-A72

MAILBOX_B2A_DAT_1
Address: Operational Base + offset (0x0003c)
MCU to Cortex-A53/Cortex-A72 data 1

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	data data of MCU to Cortex-A53/Cortex-A72

MAILBOX_B2A_CMD_2
Address: Operational Base + offset (0x00040)
MCU to Cortex-A53/Cortex-A72 command 2

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	command command of Cortex-M0 to Cortex-A53/Cortex-A72

MAILBOX_B2A_DAT_2
Address: Operational Base + offset (0x00044)
MCU to Cortex-A53/Cortex-A72 data 2

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	data data of Cortex-M0 to Cortex-A53/Cortex-A72

MAILBOX_B2A_CMD_3
Address: Operational Base + offset (0x00048)
MCU to Cortex-A53/Cortex-A72 command 3

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	command command of Cortex-M0 to Cortex-A53/Cortex-A72

MAILBOX_B2A_DAT_3
Address: Operational Base + offset (0x0004c)
MCU to Cortex-A53/Cortex-A72 data 3

Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	data data of Cortex-M0 to Cortex-A53/Cortex-A72

MAILBOX_ATOMIC_LOCK_00
Address: Operational Base + offset (0x00100)
Lock flag register 00

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	atomic_lock_00 lock flag bit 00

MAILBOX_ATOMIC_LOCK_01
Address: Operational Base + offset (0x00104)
Lock flag register 01

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	atomic_lock_01 lock flag bit 01

MAILBOX_ATOMIC_LOCK_02
Address: Operational Base + offset (0x00108)
Lock flag register 02

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	atomic_lock_02 lock flag bit 02

MAILBOX_ATOMIC_LOCK_03
Address: Operational Base + offset (0x0010c)
Lock flag register 03

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	atomic_lock_03 lock flag bit 03

MAILBOX_ATOMIC_LOCK_04
Address: Operational Base + offset (0x00110)
Lock flag register 04

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	atomic_lock_04 lock flag bit 04

MAILBOX_ATOMIC_LOCK_05
Address: Operational Base + offset (0x00114)
Lock flag register 05

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	atomic_lock_05 lock flag bit 05

MAILBOX_ATOMIC_LOCK_06
Address: Operational Base + offset (0x00118)
Lock flag register 06

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	atomic_lock_06 lock flag bit 06

MAILBOX_ATOMIC_LOCK_07
Address: Operational Base + offset (0x0011c)
Lock flag register 07

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	atomic_lock_07 lock flag bit 07

MAILBOX_ATOMIC_LOCK_08

Address: Operational Base + offset (0x00120)
Lock flag register 08

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	atomic_lock_08 lock flag bit 08

MAILBOX_ATOMIC_LOCK_09
Address: Operational Base + offset (0x00124)
Lock flag register 09

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	atomic_lock_09 lock flag bit 09

MAILBOX_ATOMIC_LOCK_10
Address: Operational Base + offset (0x00128)
Lock flag register 10

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	atomic_lock_10 lock flag bit 10

MAILBOX_ATOMIC_LOCK_11
Address: Operational Base + offset (0x0012c)
Lock flag register 11

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	atomic_lock_11 lock flag bit 11

MAILBOX_ATOMIC_LOCK_12
Address: Operational Base + offset (0x00130)
Lock flag register 12

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	atomic_lock_12 lock flag bit 12

MAILBOX_ATOMIC_LOCK_13
Address: Operational Base + offset (0x00134)
Lock flag register 13

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	atomic_lock_13 lock flag bit 13

MAILBOX_ATOMIC_LOCK_14
Address: Operational Base + offset (0x00138)
Lock flag register 14

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	atomic_lock_14 lock flag bit 14

MAILBOX_ATOMIC_LOCK_15
Address: Operational Base + offset (0x0013c)
Lock flag register 15

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	atomic_lock_15 lock flag bit 15

MAILBOX_ATOMIC_LOCK_16
Address: Operational Base + offset (0x00140)
Lock flag register 16

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	atomic_lock_16 lock flag bit 16

MAILBOX_ATOMIC_LOCK_17
Address: Operational Base + offset (0x00144)
Lock flag register 17

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	atomic_lock_17 lock flag bit 17

MAILBOX_ATOMIC_LOCK_18
Address: Operational Base + offset (0x00148)
Lock flag register 18

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	atomic_lock_18 lock flag bit 18

MAILBOX_ATOMIC_LOCK_19
Address: Operational Base + offset (0x0014c)
Lock flag register 19

Bit	Attr	Reset Value	Description

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	atomic_lock_19 lock flag bit 19

MAILBOX_ATOMIC_LOCK_20
Address: Operational Base + offset (0x00150)
Lock flag register 20

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	atomic_lock_20 lock flag bit 20

MAILBOX_ATOMIC_LOCK_21
Address: Operational Base + offset (0x00154)
Lock flag register 21

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	atomic_lock_21 lock flag bit 21

MAILBOX_ATOMIC_LOCK_22
Address: Operational Base + offset (0x00158)
Lock flag register 22

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	atomic_lock_22 lock flag bit 22

MAILBOX_ATOMIC_LOCK_23
Address: Operational Base + offset (0x0015c)
Lock flag register 23

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	atomic_lock_23 lock flag bit 23

MAILBOX_ATOMIC_LOCK_24
Address: Operational Base + offset (0x00160)
Lock flag register 24

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	atomic_lock_24 lock flag bit 24

MAILBOX_ATOMIC_LOCK_25
Address: Operational Base + offset (0x00164)
Lock flag register 25

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	atomic_lock_25 lock flag bit 25

MAILBOX_ATOMIC_LOCK_26
Address: Operational Base + offset (0x00168)
Lock flag register 26

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	atomic_lock_26 lock flag bit 26

MAILBOX_ATOMIC_LOCK_27
Address: Operational Base + offset (0x0016c)
Lock flag register 27

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	atomic_lock_27 lock flag bit 27

MAILBOX_ATOMIC_LOCK_28
Address: Operational Base + offset (0x00170)
Lock flag register 28

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	atomic_lock_28 lock flag bit 28

MAILBOX_ATOMIC_LOCK_29
Address: Operational Base + offset (0x00174)
Lock flag register 29

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	atomic_lock_29 lock flag bit 29

MAILBOX_ATOMIC_LOCK_30
Address: Operational Base + offset (0x00178)
Lock flag register 30

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved

Bit	Attr	Reset Value	Description
0	RW	0x0	atomic_lock_30 lock flag bit 30

MAILBOX_ATOMIC_LOCK_31
Address: Operational Base + offset (0x0017c)
Lock flag register 31

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	atomic_lock_31 lock flag bit 31

20.5 Application Notes

- The order for writing MAILBOX_B2A_CMD_i/ MAILBOX_A2B_CMD_i and MAILBOX_B2A_DATA_i/ MAILBOX_A2B_DATA_i registers is limited: MAILBOX_B2A_CMD_i/ MAILBOX_A2B_CMD_i firstly, then MAILBOX_B2A_DATA_i/ MAILBOX_A2B_DATA_i. If wrong order is used, then the interrupt cannot be generated successfully.
- If you want to clear the interrupt, you can read out the STATUS register and writing 1 to corresponding bit.
- When using mailbox, software should read MAILBOX_ATOMIC_LOCK_i first. That the reading value is 0 means that it is available, and 1 means it has been automatically locked. Writing MAILBOX_ATOMIC_LOCK_i will clear this bit.

Chapter 21 eFuse

21.1 Overview

This device supports two eFuse. Both are organized as 32bits by 32 one-time programmable electrical fuses. eFuse0 is non-secure efuse(NSeFuse), and eFuse1 is secure efuse(SeFuse). eFuse0 can be accessed by APB bus at secure mode and non-secure mode. eFuse1 can only be accessed by APB bus at secure mode. It is a type of non-volatile memory fabricated in standard CMOS logic process. The main features are as follows:

- Working condition : VDD = 0.9±10%
- Programming condition : VQPS = 1.8V~1.98V
- Program time : 12us±1us
- Read condition : VQPS = 0V
- Embedded four redundancy bits
- Provide power-down and standby mode

21.2 Block Diagram

In the following diagram, all the signals except power supply VDD and VQPS are controlled by registers. For detailed description, please refer to detailed register descriptions.

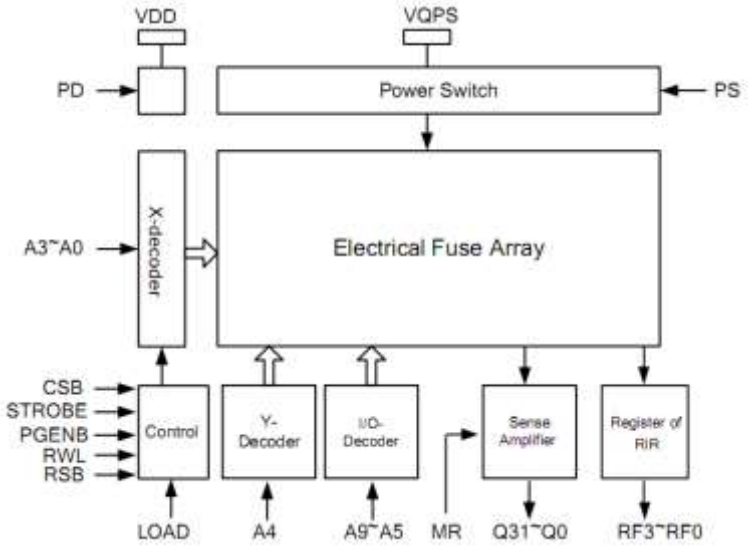


Fig. 21-1 eFuse block diagram

21.3 Function Description

This electrical fuse macro has 8 operation modes: array program(A_PGM), redundancy program (R_PGM), array read (A_READ), redundancy read (R_READ), power-down, standby mode and 2 test modes: margin A_READ1 mode and margin R_READ1 mode.

Array Program Mode (A_PGM)

In this mode, this macro is ready for electrical fuse programming. Any bit in this macro can be programmed in any order by raising STROBE high with a proper address selected. The selected address needs to satisfy setup and hold time with respect to STROBE to be valid. Only one bit is programmed at a time.

Array Read Mode (A_READ); Margin A_READ1 Mode

In these 2 modes, this macro is ready to read data from fuse cells. 32 bits Q31~Q0 can be read out by raising STROBE high with a proper address selected. During this read operation, address signals A9~A5 are "don"t care". The read trip point of Array Read Mode is lower than that of Margin A_READ1 Mode. If RSB is at "L" and enable redundancy function, please MUST enter the redundancy read mode (R_READ or Margin R_READ1) and read the RIR data once prior to the array read mode (A_READ or Margin A_READ1) after power-up even if repairing is not needed. Redundancy read requires two strobe cycles to read out completed repairing information.The data will be stored in registers and remain there until power-down or

power-off. In subsequent array read, when read access the failure bit in the main array, the corresponding output data will be corrected automatically.

Redundancy Program Mode (R_PGM)

In this mode, this macro is ready for electrical fuse programming on redundancy bits. Any bit within the redundancy array can be programmed in any order by raising STROBE high with a proper address selected. The selected address needs to satisfy setup and hold time with respect to STROBE to be valid. Only one bit is programmed at a time.

Redundancy Read Mode (R_READ); Margin R_READ1 Mode

In these 2 modes, this macro is ready to read data from redundancy information row to register, Q31~Q0 and RF3~RF0 by two cycle STROBE high. During redundancy read operation, address signals A9~A0 are "don"t care" except A4. The read trip point of Redundancy READ Mode is lower than that of Margin R_READ1 Mode.

Power-down Mode

In this mode, the macro is at power-down mode. In the power-down mode, the power-leakage has best performance and consumes the least current of VDD.

Standby Mode

When PD=L, PS=L, CSB=H, STROBE, PGENB and LOAD, MR, RWL, RSB are "don"t care", the macro is at standby mode.

21.4 Register Description

This section describes the control/status registers of the design.

21.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
EFUSE_CTRL	0x0000	W	0x00000000	efuse control register
EFUSE_DOUT	0x0004	W	0x00000000	efuse data out register
EFUSE_RF	0x0008	W	0x00000000	efuse redundancy bit used indicator register
EFUSE_JTAG_PASS	0x0010	W	0x0cf7680a	Jtag password
EFUSE_STROBE_FINISH_CTRL	0x0014	W	0x00009003	efuse strobe finish control register

*Notes: Size: **B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**- WORD (32 bits) access*

21.4.2 Detail Register Description

EFUSE_CTRL

Address: Operational Base + offset (0x0000)

eFuse control register

Bit	Attr	Reset Value	Description
31:26	RO	0x00	reserved
25:16	RW	0x00	efuse_addr efuse address pins :A[9:0]
15:10	RO	0x00	reserved
9	RW	0x0	efuse_strobe_sft_sel efuse strobe control software mode select, active high
8	RW	0x0	efuse_rwl efuse redundancy information row select (active high) : RWL
7	RW	0x1	efuse_rsb efuse redundancy enable(active low) : RSB
6	RW	0x0	efuse_mr efuse read trip point setting, MR = L for normal read mode; MR = H for margin read1 mode : MR

Bit	Attr	Reset Value	Description
5	RW	0x1	efuse_pd efuse power down enable (active high) : PD
4	RW	0x0	efuse_ps efuse pass 1.8V program voltage to internal for program(active high) : PS
3	RW	0x1	efuse_pgenb efuse program enable (active low) : PGENB
2	RW	0x0	efuse_load efuse turn on sense amplifier and load data into latch (active high) : LOAD
1	RW	0x0	efuse_strobe efuse turn on the array for read or program access (active high) : STROBE
0	RW	0x1	efuse_csb efuse chip select enable signal, active low : CSB

EFUSE_DOUT
Address: Operational Base + offset (0x0004)
eFuse data out register

Bit	Attr	Reset Value	Description
31:0	RO	0x00	efuse_dout eFuse data output

EFUSE_RF
Address: Operational Base + offset (0x0008)
efuse redundancy bit used indicator register

Bit	Attr	Reset Value	Description
31:4	RO	0x00	reserved
3:0	RO	0x0	efuse_rf_r efuse redundancy bit used indicator register for RF3~RF0, Output high once the redundancy bit has been used.

EFUSE_JTAG_PASSWD
Address: Operational Base + offset (0x0010)
eFuse jtag passwd register

Bit	Attr	Reset Value	Description
31:0	RW	0xcf7680a	Jtag_passwd Jtag password for jtag monitor

EFUSE_STROBE_FINISH_CON
Address: Operational Base + offset (0x0014)
eFuse jtag passwd register

Bit	Attr	Reset Value	Description
31:16	RO	0x00	reserved

Bit	Attr	Reset Value	Description
15:8	RW	0x90	efuse_strobe_finish_prg efuse read strobe finish control in hardware mode.
7:0	RW	0x03	efuse_strobe_finish_read efuse program strobe finish control in hardware mode.

21.5 Timing Diagram

- **When eFuse is in A_PGM mode**

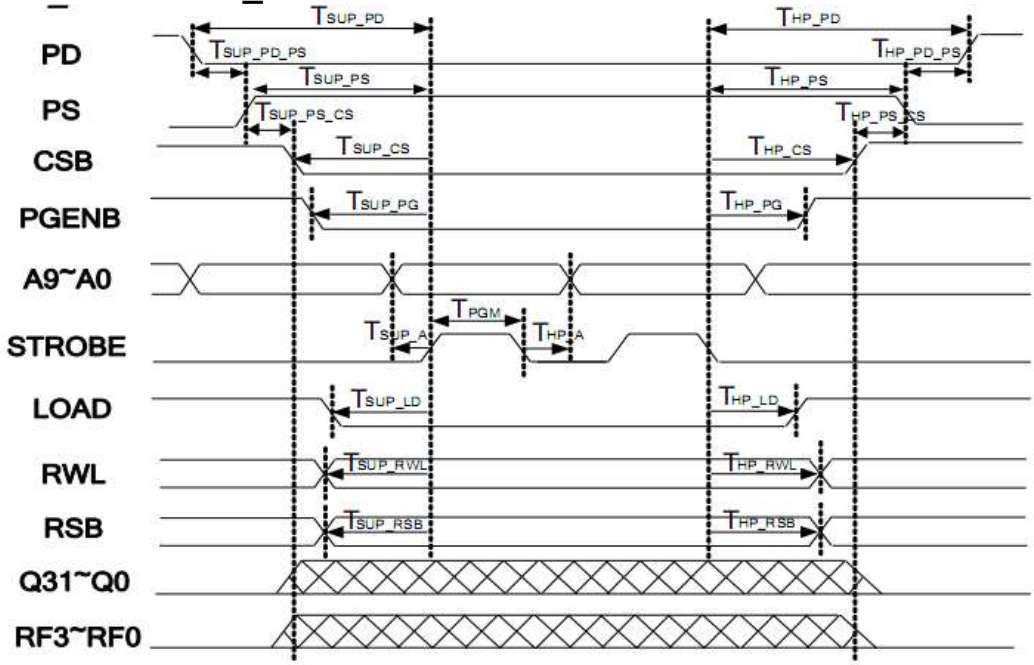


Fig. 21-2 eFuse timing diagram A_PGM mode

- **When eFuse is in R_PGM mode**

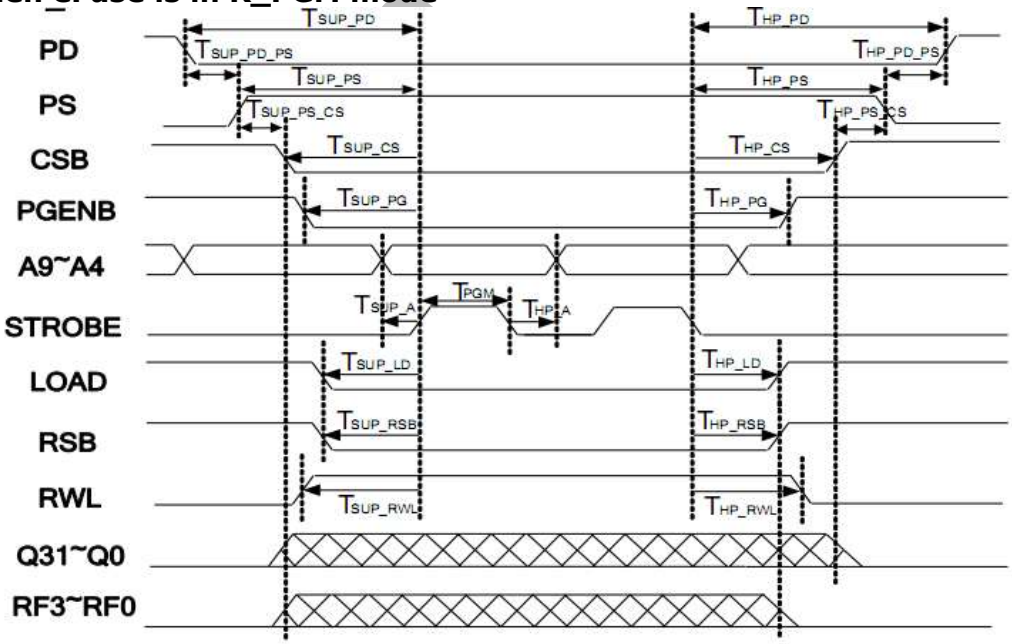


Fig. 21-3 eFuse timing diagram R_PGM mode

Table 21-1 Timing Requirements for Program Mode

Parameter	Symbol	Min.	Typ.	Max.	Unit
PD to PS setup time	$T_{SUP\_PD\_PS}$		796.549		ns
PD to PS hold time	$T_{HP\_PD\_PS}$		8.17		ns

Parameter	Symbol	Min.	Typ.	Max.	Unit
PS to CSB setup time	$T_{SUP\_PS\_CS}$		45.549		ns
PS to CSB hold time	$T_{HP\_PS\_CS}$		45.17		ns
PD to STROBE setup time	T_{SUP_PD}		846.368		ns
PD to STROBE hold time	T_{HP_PD}		57.394		ns
PS to STROBE setup	T_{SUP_PS}		49.819		ns
PS to STROBE hold time	T_{HP_PS}		49.224		ns
RWL to STROBE setup time	T_{SUP_RWL}		12.397		ns
RWL to STROBE hold time	T_{HP_RWL}		11.91		ns
RSB to STROBE setup time	T_{SUP_RSB}		12.897		ns
RSB to STROBE hold time	T_{HP_RSB}		12.41		ns
CSB to STROBE setup time	T_{SUP_CS}		4.29		ns
CSB to STROBE hold time	T_{HP_CS}		4.056		ns
PGENB to STROBE setup time	T_{SUP_PG}		3.846		ns
PGENB to STROBE hold time	T_{HP_PG}		3.872		ns
Typical program strobe pulse width	T_{PGM}		12		us
A7~A0 to STROBE setup time	T_{SUP_A}		11.797		ns
A7~A0 to STROBE hold time	T_{HP_A}		11.31		ns
LOAD to STROBE setup time	T_{SUP_LD}		3.929		ns
LOAD to STROBE hold time	T_{HP_LD}		3.787		ns

- **When efuse is in A_READ mode; Margin A_READ1 Mode.**

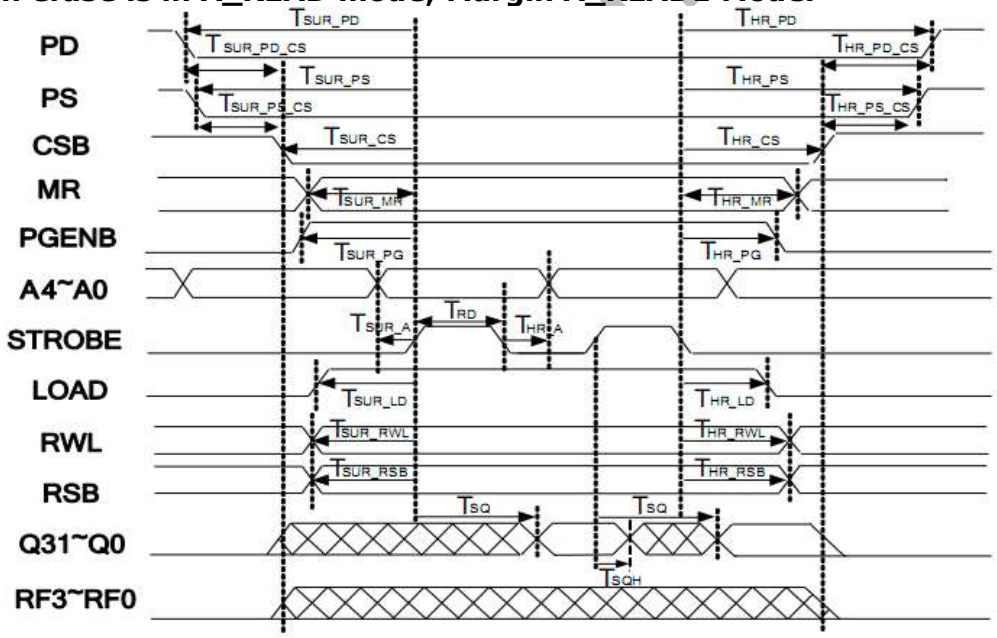


Fig. 21-4 eFuse timing diagram in A_READ mode and Margin A_READ1 Mode

- **When efuse is in R_READ mode; Margin R_READ1 Mode.**

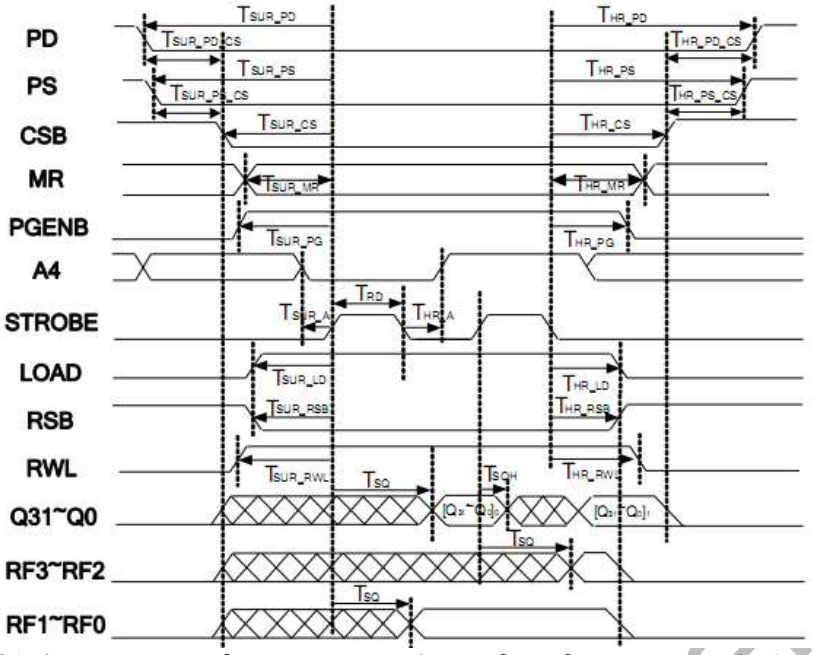


Fig. 21-5 eFuse timing diagram in R_READ mode and Margin R_READ1 Mode

Table 21-2 Timing Requirements for Read Mode

Parameter	Symbol	Min.	Typ.	Max.	Unit
PD to CSB setup time	$T_{SUR\_PD\_CS}$		796.531		ns
PD to CSB hold time	$T_{HR\_PD\_CS}$		8.168		ns
PS to CSB setup time	$T_{SUR\_PS\_CS}$		45.531		ns
PS to CSB hold time in	$T_{HR\_PS\_CS}$		47.168		ns
PD to STROBE setup time	T_{SUR_PD}		800.781		ns
PD to STROBE hold time	T_{HR_PD}		12.22		ns
PS to STROBE setup time	T_{SUR_PS}		49.781		ns
PS to STROBE hold time	T_{HR_PS}		51.22		ns
RWL to STROBE setup time	T_{SUR_RWL}		12.397		ns
RWL to STROBE hold time	T_{HR_RWL}		11.91		ns
RSB to STROBE setup time	T_{SUR_RSB}		12.897		ns
RSB to STROBE hold time	T_{HR_RSB}		12.41		ns
CSB to STROBE setup time	T_{SUR_CS}		4.25		ns
CSB to STROBE hold time	T_{HR_CS}		4.052		ns
PGENB to STROBE setup time	T_{SUR_PG}		3.844		ns
PGENB to STROBE hold time	T_{HR_PG}		3.872		ns
Read strobe pulse width	T_{RD}		110		ns
A2~A0 to STROBE setup time	T_{SUR_A}		11.797		ns
A2~A0 to STROBE hold time	T_{HR_A}		11.31		ns
LOAD to STROBE setup time	T_{SUR_LD}		3.918		ns
LOAD to STROBE hold time	T_{HR_LD}		3.782		ns
MR to STROBE setup time	T_{SUR_MR}		10.097		ns
MR to STROBE hold time	T_{HR_MR}		9.61		ns
Q31~Q0 access time from STROBE high	T_{SQ}		109.2		ns
Q31~Q0 hold time to the next STROBE	T_{SQH}		0		ns

21.6 Application Notes

During usage of efuse, customers must pay more attention to the following items:
1. In condition of program(PGM) mode, VQPS= 1.8V~1.98V.
2. Q0~Q7/Q31 will be reset to "0" once CSB at high.
3. No data access allowed at the rising edge of CSB.
4. All the program timing for each signal must be more than the value defined in the timing table.
5. It must use Margin A_READ1 Mode when read out the eFuse data to determine whether program successfully.
6.If enable redundancy function, please MUST enter the redundancy read mode (R_READ or Margin R_READ1) and read the RIR data once prior to the array read mode (A_READ or Margin A_READ1) after power-up even if repairing is not needed. Redundancy read requires two strobe cycles to read out the complete repairing information. The data will be stored in registers and will remain there until power-down or power-off. In subsequent array read, when read access the failure bit in the main array, the corresponding output data will be corrected automatically.

21.6.1 eFuse Macro Operating Modes

Follow tapble is eFuse macro operation mode truth table

Table 21-3 eFuse macro operation mode truth table

Mode	CSB	STROBE	LOAD	PGENB	PS	PD	MR	RSB	RWL	VQPS
A_READ mode	L	H	H	H	L	L	L	L	L	0V
	L	H	H	H	L	L	L	H	X	0V
A_PGM mode	L	H	L	L	H	L	X	L	L	1.8V~1.98V
	L	H	L	L	H	L	X	H	X	1.8V~1.98V
R_READ mode	L	H	H	H	L	L	L	L	H	0V
R_PGM mode	L	H	L	L	H	L	X	L	H	1.8V~1.98V
Standby mode	H	X	X	X	L	L	X	X	X	0V
Power-down mode	H	X	X	X	L	H	X	X	X	0V
Margin A_READ1	L	H	H	H	L	L	H	L	L	0V
	L	H	H	H	L	L	H	H	X	0V
Margin R_READ1 mode	L	H	H	H	L	L	H	L	H	0V

- Maximum accumulative time when VQPS=1.8V~1.98V, PS=H should be less than 0.2 sec.
- VQPS MUST NOT exceed 1.98V (1.8V+10%) when PS=H for device reliability concern.
- Please always keep PS at "L" except program mode.
- Max accumulative read access time should be less than 2 seconds per each bit when CSB=L, LOAD=H, PGENB=H, STROBE=H.
- Max accumulative numbers of read MUST be less than 2 million reads per each bit when CSB=L, LOAD=H, PGENB=H, STROBE=H.
- PS=H, PD=H state is not allowed to avoid unintended program.
- RSB signal (active low) is used to disable/enable redundancy feature (repair function).

21.6.2 eFuse STOBOE control

eFuse STROBE has hardware and software control mode, the default mode is hardware control.

- In hardware control mode, the STROBE is asserted at the rising edge of efuse_strobe and

de-asserted by the internal circuit accordding to the timing requirements. You can configure the efuse_strobe_finish_read and efuse_strobe_finish_prg to adjust the active time of STROBE. The default active time of STROBE is 250ns in read mode and 12us in program mode. At default setting, internal circuit require efuse_strobe to remain valid longer than 500 ns in read mode and longer than 12.5 us in program mode. In addition, due the exist of internal circuit control, the Tsq (efuse_strobe -> Q) increase 250 ns.

- You can configure the efuse_strobe_sft_sel to select software control mode, the STROBE is directly controlled by efuse_strobe. You must configure the STROBE according to the timing requirements.

21.6.3 Read Mode

For read mode address signals A[9]~A[5] are "invalid"

Table 21-4 eFuse Dout Format

A[4]-~A[0]	D[0]	D[1]	…	…	D[30]	D[31]
00000	Fuse[0]	Fuse[32]	…	…	Fuse[960]	Fuse[992]
00001	Fuse[1]	Fuse[33]	…	…	Fuse[961]	Fuse[993]
…	…	…	…	…	…	…
…	…	…	…	…	…	…
11110	Fuse[30]	Fuse[62]	…	…	Fuse[990]	Fuse[1022]
11111	Fuse[31]	Fuse[63]	…	…	Fuse[991]	Fuse[1023]

21.6.4 Read & Program Masked For eFuse1

The eFuse1 was masked by the program masked bits in program mode and read masked bits in read mode.The masked bits comes from Secure GRF registers SGRF_EFUSE_PRG_MASK and SGRF_EFUSE_READ_MASK. The registers only can write one time. Only when the masked bit is set to "1", the program and read is valid.

The Masked bit only 32bits, so one bit controlled 32 eFuse bit, showed as the following:

READ_MASK /PGR_MASK	A[4]-~A[0]	D[0]	D[1]	…	…	D[30]	D[31]
[0]	00000	Fuse[0]	Fuse[32]	…	…	Fuse[960]	Fuse[992]
[1]	00001	Fuse[1]	Fuse[33]	…	…	Fuse[961]	Fuse[993]
…	…	…	…	…	…	…	…
…	…	…	…	…	…	…	…
[30]	11110	Fuse[30]	Fuse[62]	…	…	Fuse[990]	Fuse[1022]
[31]	11111	Fuse[31]	Fuse[63]	…	…	Fuse[991]	Fuse[1023]

Chapter 22 WDT

22.1 Overview

Watchdog Timer (WDT) is an APB slave peripheral that can be used to prevent system lockup that caused by conflicting parts or programs in a SOC. The WDT would generate interrupt or reset signal when its counter reaches zero, then a reset controller would reset the system. WDT supports the following features:

- 32 bits APB bus width
- WDT counter's clock is pclk
- 32 bits WDT counter width
- Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
- WDT can perform two types of operations when timeout occurs:
  - Generate a system reset
  - First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
- Programmable reset pulse length
- Total 16 defined-ranges of main timeout period
- There are two watchdogs in ALIVE named WDT0 and WDT1, and one watchdog in PMU named WDT2. WDT0 can drive CRU to generate global software reset.

22.2 Block Diagram

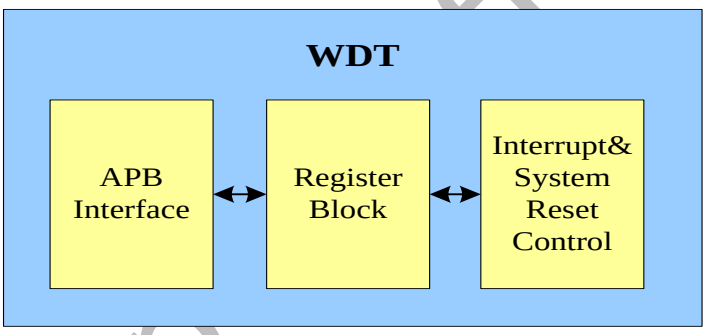


Fig. 22-1 WDT block diagram

Block Descriptions:

- APB Interface

The APB Interface implements the APB slave operation. Its data bus width is 32 bits.

- Register Block

A register block that read coherence for the current count register.

- Interrupt & system reset control

An interrupt/system reset generation block is comprised of a decrementing counter and control logic.

22.3 Function Description

22.3.1 Operation

Counter

The WDT counts from a preset (timeout) value in descending order to zero. When the counter reaches zero, depending on the output response mode selected, either a system reset or an interrupt occurs. When the counter reaches zero, it wraps to the selected timeout value and continues decrementing. The user can restart the counter to its initial value. This is programmed by writing to the restart register at any time. The process of restarting the watchdog counter is sometimes referred as kicking the dog. As a safety feature to prevent accidental restarts, the value 0x76 must be written to the Current Counter Value Register (WDT_CRR).

Interrupts

The WDT can be programmed to generate an interrupt (and then a system reset) when a timeout occurs. When a 1 is written to the response mode field (RMOD, bit 1) of the Watchdog Timer Control Register (WDT_CR), the WDT generates an interrupt. If it is not cleared by the time a second timeout occurs, then it generates a system reset. If a restart occurs at the same time the watchdog counter reaches zero, an interrupt is not generated.

System Resets

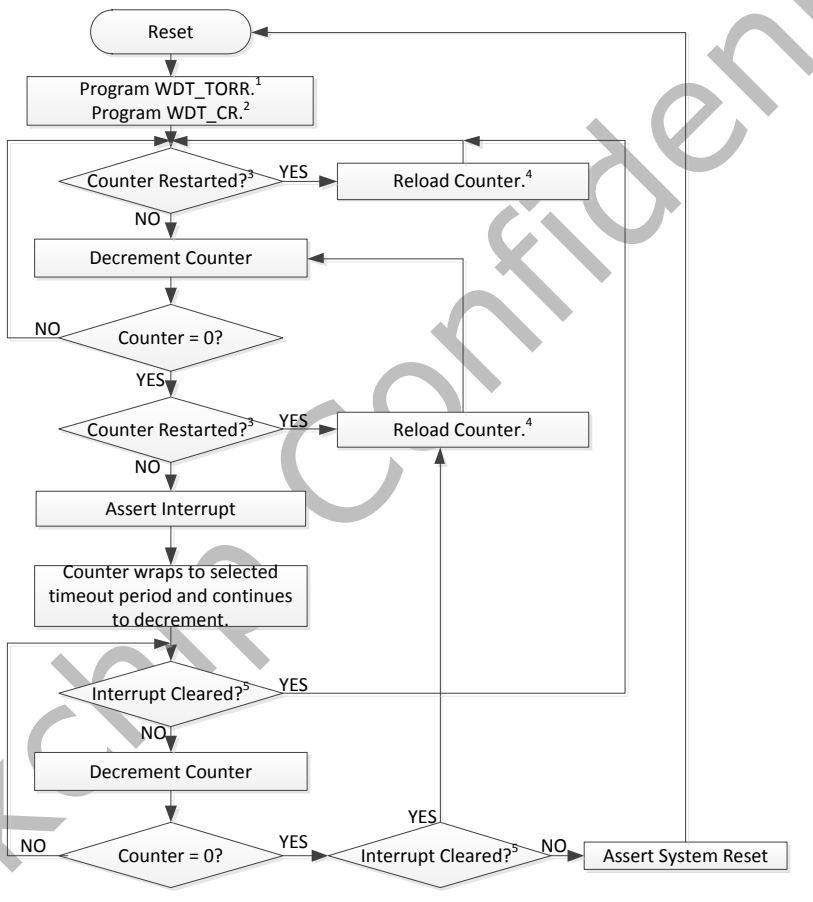
When a 0 is written to the output response mode field (RMOD, bit 1) of the Watchdog Timer Control Register (WDT_CR), the WDT generates a system reset when a timeout occurs.

Reset Pulse Length

The reset pulse length is the number of pclk cycles for which a system reset is asserted. When a system reset is generated, it remains asserted for the number of cycles specified by the reset pulse length or until the system is reset. A counter restart has no effect on the system reset once it has been asserted.

22.3.2 Programming sequence

Operation Flow Chart (Response mode=1)



1. Select required timeout period.
2. Set reset pulse length, response mode, and enable WDT.
3. Write 0x76 to WDT_CRR.
4. Starts back to selected timeout period.
5. Can clear by reading WDT_EOI or restarting (kicking) the counter by writing 0x76 to WDT_CRR.

Fig. 22-2 WDT Operation Flow

22.4 Register Description

This section describes the control/status registers of the design.

22.4.1 Registers Summary

Name	Offset	Size	Reset Value	Description
WDT_CR	0x0000	W	0x0000000a	Control Register

Name	Offset	Size	Reset Value	Description
WDT_TORR	0x0004	W	0x00000000	Timeout range Register
WDT_CCVR	0x0008	W	0x00000000	Current counter value Register
WDT_CRR	0x000c	W	0x00000000	Counter restart Register
WDT_STAT	0x0010	W	0x00000000	Interrupt status Register
WDT_EOI	0x0014	W	0x00000000	Interrupt clear Register

*Notes:Size:**B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access*

22.4.2 Detail Register Description

WDT_CR
Address: Operational Base + offset (0x0000)
Control Register

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:2	RW	0x2	rst_pluse_lenth Reset pulse length. This is used to select the number of pclk cycles for which the system reset stays asserted. 000: 2 pclk cycles 001: 4 pclk cycles 010: 8 pclk cycles 011: 16 pclk cycles 100: 32 pclk cycles 101: 64 pclk cycles 110: 128 pclk cycles 111: 256 pclk cycles
1	RW	0x1	resp_mode Response mode. Selects the output response generated to a timeout. 0: Generate a system reset. 1: First generate an interrupt and if it is not cleared by the time a second timeout occurs then generate a system reset.
0	RW	0x0	wdt_en Writable when the configuration parameter WDT_ALWAYS_EN=0, otherwise, it is readable. This bit is used to enable and disable the watchdog. When disabled, the counter dose not decrement .Thus, no interrupt or system reset is generated. Once this bit has been enabled, it can be cleared only by a system reset. 0: WDT disabled; 1: WDT enabled.

WDT_TORR
Address: Operational Base + offset (0x0004)
Timeout range Register

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved

Bit	Attr	Reset Value	Description
3:0	RW	0x0	timeout_period Timeout period. This field is used to select the timeout period from which the watchdog counter restarts. A change of the timeout period takes effect only after the next counter restart (kick). The range of values available for a 32-bit watchdog counter are: 0000: 0x0000ffff 0001: 0x0001ffff 0010: 0x0003ffff 0011: 0x0007ffff 0100: 0x000fffff 0101: 0x001fffff 0110: 0x003fffff 0111: 0x007fffff 1000: 0x00ffffff 1001: 0x01ffffff 1010: 0x03ffffff 1011: 0x07ffffff 1100: 0x0fffffff 1101: 0x1fffffff 1110: 0x3fffffff 1111: 0x7fffffff

WDT_CCVR
Address: Operational Base + offset (0x0008)
Current counter value Register

Bit	Attr	Reset Value	Description
31:0	RO	0x00000000	cur_cnt Current counter value This register, when read, is the current value of the internal counter. This value is read coherently whenever it is read

WDT_CRR
Address: Operational Base + offset (0x000c)
Counter restart Register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	W1C	0x00	cnt_restart Counter restart This register is used to restart the WDT counter. As a safety feature to prevent accidental restarts, the value 0x76 must be written. A restart also clears the WDT interrupt. Reading this register returns zero.

WDT_STAT

Address: Operational Base + offset (0x0010)
Interrupt status Register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RO	0x0	wdt_status This register shows the interrupt status of the WDT. 1: Interrupt is active regardless of polarity; 0: Interrupt is inactive.

WDT_EOI
Address: Operational Base + offset (0x0014)
Interrupt clear Register

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RC	0x0	wdt_int_clr Clears the watchdog interrupt. This can be used to clear the interrupt without restarting the watchdog counter.